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Rev. 3, Apr-2008

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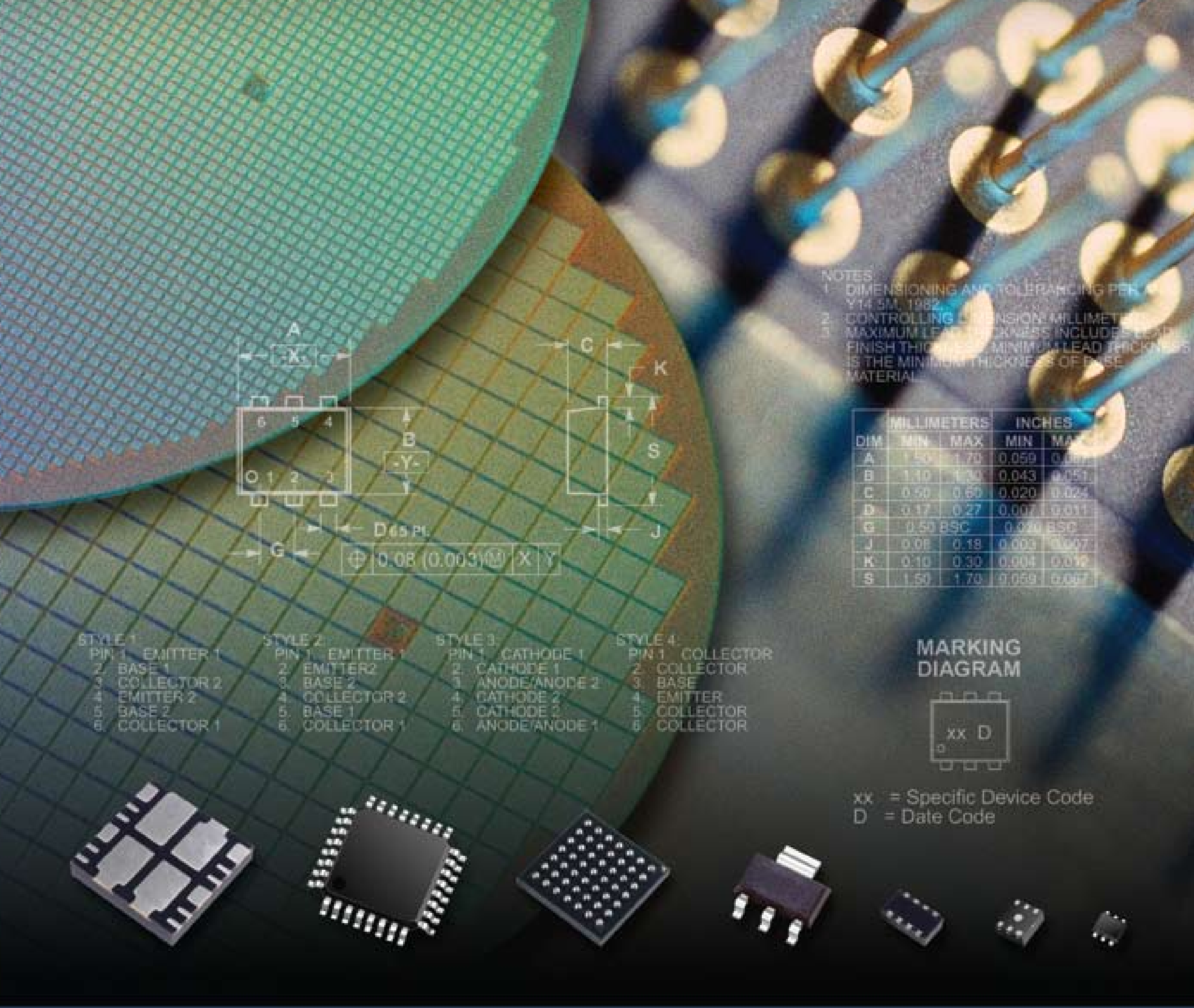
Semiconductor Packages and Case Outlines

Reference Manual



Semiconductor Packages and Case Outlines

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Common Package Reference Table

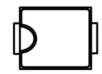
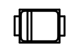
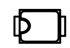
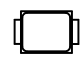
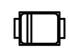
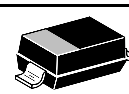
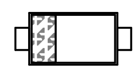
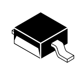
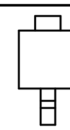
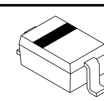
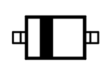
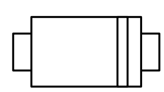
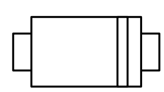
Common Packages

The table is organized by mounting style (surface mount, followed by through−hole), pin count (2, 3, 4, etc., to multi−lead) and case numbers (smallest to largest) to assist in quickly locating the desired information. A detailed index of package designation and case numbers is located in the back of the book.

PACKAGE STYLE CHARACTERISTIC

SURFACE MOUNT

Section 1: 2−Lead Packages

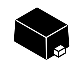
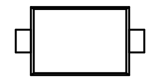
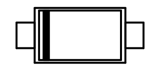
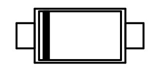
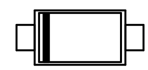
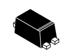
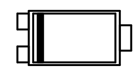
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Surface Mount J−Lead	SO	SMC	CASE NO. 403 (page 77)	 SCALE 1:1	
Surface Mount J−Lead	SO	**SMB** DO−214AA	CASE NO. 403A (page 78)	 SCALE 1:1	
Surface Mount J−Lead	SO	SMA	CASE NO. 403B (page 78)	 SCALE 1:1	
Surface Mount	SO	SMB	CASE NO. 403C (page 79)	 SCALE 1:1	
Surface Mount	SO	SMA	CASE NO. 403D (page 79)	 SCALE 1:1	
Surface Mount Gull Wing	SO	**SOD−123** SC−77	CASE NO. 425 (page 90)	 SCALE 4:1	
Surface Mount Heat Sink	SO	POWERMITE®	CASE NO. 457 (page 91)	 SCALE 2:1	
Surface Mount Gull Wing	SO	**SOD−323** SC−76	CASE NO. 477 (page 95)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOD−123FL	CASE NO. 498 (page 126)	 SCALE 2:1	
Surface Mount Flat Lead	SO	SOD−123F	CASE NO. 498AB (page 127)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

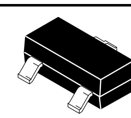
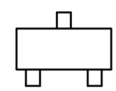
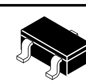
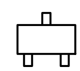
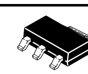
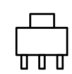
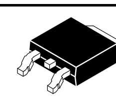
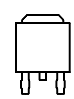
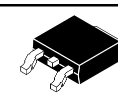
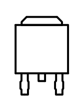
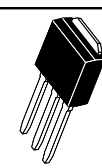
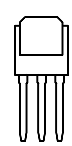
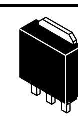
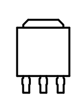
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 1: 2−Lead Packages

Surface Mount Flat Lead	SO	**SOD−523** SC−79	CASE NO. 502 (page 141)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOD−723	CASE NO. 509AA (page 158)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOD−923	CASE NO. 514AA (page 164)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOD−923	CASE NO. 514AB (page 165)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOT−1123	CASE NO. 524AA (page 175)	 SCALE 4:1	

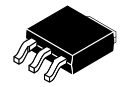
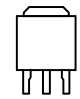
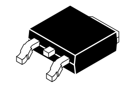
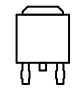
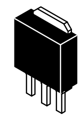
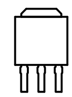
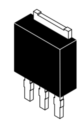
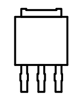
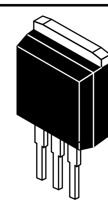
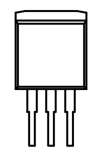
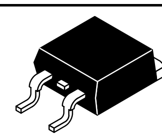
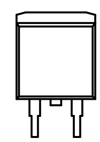
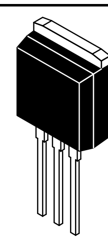
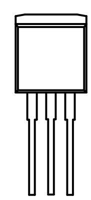
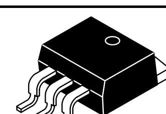
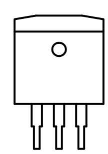
Section 2: 3−Lead Packages

Surface Mount Gull Wing	SO	**SOT−23** TO−236AB	CASE NO. 318 (page 63)	 SCALE 4:1	
Surface Mount Gull Wing	SO	SC−59	CASE NO. 318D (page 64)	 SCALE 2:1	
Surface Mount Gull Wing	SO	SOT−223	CASE NO. 318E (page 65)	 SCALE 1:1	
Surface Mount Heat Sink	SO	DPAK	CASE NO. 369A (page 73)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**DPAK** Single Gauge TO−252	CASE NO. 369C (page 74)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**DPAK** Single Gauge, Straight Lead TO−251	CASE NO. 369D (page 74)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**3 IPAK** Straight Lead	CASE NO. 369F (page 75)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

SURFACE MOUNT

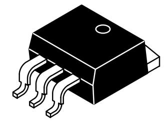
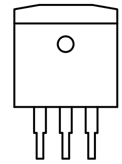
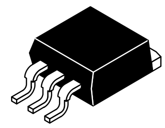
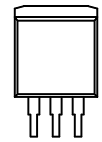
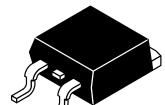
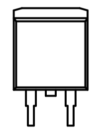
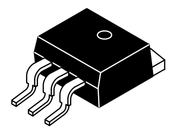
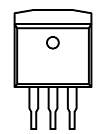
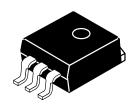
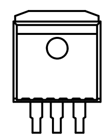
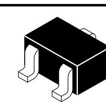
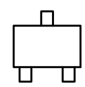
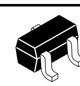
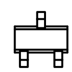
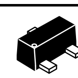
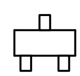
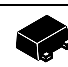
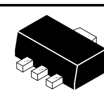
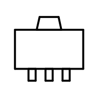
Section 2: 3−Lead Packages

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Surface Mount Heat Sink	SO	**DPAK** Siurface Mount	CASE NO. 369G (page 75)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**DPAK** Single Gauge	CASE NO. 369AA (page 76)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**3 IPAK** Straight Lead	CASE NO. 369AC (page 76)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**3.5MM IPAK** Straight Lead	CASE NO. 369AD (page 77)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**D²PAK** Straight Lead	CASE NO. 418 (page 80)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**D²PAK**	CASE NO. 418B (page 81)	 SCALE 1:1	
Surface Mount Heat Sink	SO	**I²PAK** TO−262	CASE NO. 418D (page 82)	 SCALE 1:1	
Surface Mount	SO	**D²PAK** Long Lead	CASE NO. 418E (page 82)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

SURFACE MOUNT

Section 2: 3−Lead Packages

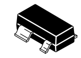
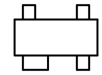
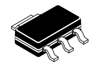
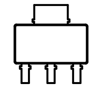
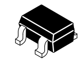
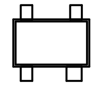
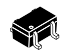
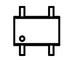
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Surface Mount	SO	**D²PAK** Short Lead	CASE NO. 418F (page 83)	 SCALE 1:1	
Surface Mount	SO	**D²PAK**	CASE NO. 418G (page 83)	 SCALE 1:1	
Surface Mount	SO	**D²PAK**	CASE NO. 418AA (page 84)	 SCALE 1:1	
Surface Mount	SO	**D²PAK**	CASE NO. 418AB (page 85)	 SCALE 1:1	
Surface Mount	SO	**D²PAK**	CASE NO. 418AF (page 85)	 SCALE 1:1	
Surface Mount Gull Wing	SO	**SC−70** SOT−323	CASE NO. 419 (page 86)	 SCALE 4:1	
Surface Mount Gull Wing	SO	**SC−75** SOT−416	CASE NO. 463 (page 92)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SC−89	CASE NO. 463C (page 95)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOT−723	CASE NO. 631AA (page 185)	 SCALE 4:1	
Surface Mount Heat Sink	SO	SOT−89	CASE NO. 1213 (page 254)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

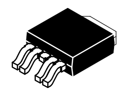
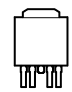
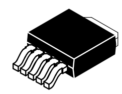
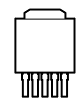
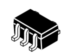
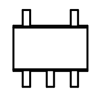
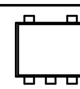
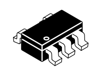
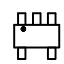
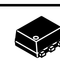
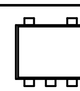
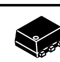
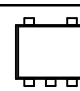
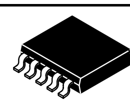
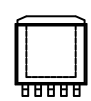
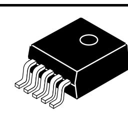
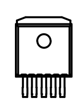
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 3: 4−Lead Packages

Surface Mount Gull Wing	SO	SOT−143	CASE NO. 318A (page 64)	 SCALE 2:1	
Surface Mount Gull Wing	SO	SOT−223, 4 Lead	CASE NO. 318H (page 68)	 SCALE 1:1	
Surface Mount Gull Wing	SO	**SC−82AB** SC70−4, SOT−343	CASE NO. 419C (page 89)	 SCALE 2:1	
Surface Mount Gull Wing	SO	SC−82	CASE NO. 900AA (page 231)	 SCALE 2:1	

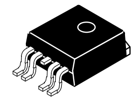
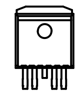
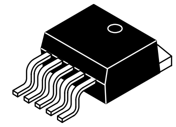
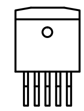
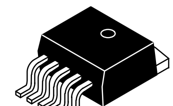
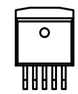
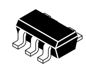
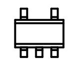
Section 4: 5−Lead Packages

Surface Mount	SO	DPAK 5 Center Lead Crop	CASE NO. 175AA (page 48)	 SCALE 1:1	
Surface Mount	SO	DPAK 5	CASE NO. 271AA (page 57)	 SCALE 1:1	
Surface Mount Gull Wing	SO	**SC−88A** SOT−353, SC70−5	CASE NO. 419A (page 87)	 SCALE 2:1	
Surface Mount Flat Lead	SO	SOT−553	CASE NO. 463B (page 94)	 SCALE 2:1	
Surface Mount Gull Wing	SO	**TSOP−5** SOT23−5, SC59−5, SC−74A	CASE NO. 483 (page 96)	 SCALE 2:1	
Surface Mount Flat Lead	SO	SOT−953	CASE NO. 527AB (page 178)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOT−953	CASE NO. 527AE (page 178)	 SCALE 4:1	
Surface Mount	SO	SPAK, 5 Lead	CASE NO. 553AB (page 179)	 SCALE 1:1	
Surface Mount	SO	D^2PAK 5−PIN	CASE NO. 936A (page 236)	 SCALE 1:1	

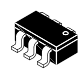
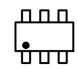
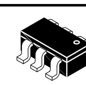
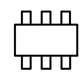
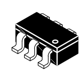
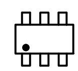
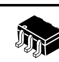
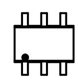
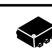
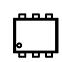
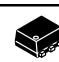
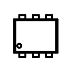
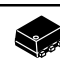
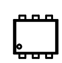
† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

SURFACE MOUNT

Section 4: 5–Lead Packages

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Surface Mount	SO	D^2PAK Center Lead Cropped	CASE NO. 936D (page 237)	 SCALE 1:1	
Surface Mount	SO	D^2PAK Long Lead	CASE NO. 936F (page 237)	 SCALE 1:1	
Surface Mount	SO	D^2PAK 5–LEAD	CASE NO. 936AA (page 239)	 SCALE 1:1	
Surface Mount Gull Wing	SO	SOT23–5	CASE NO. 1212 (page 254)	 SCALE 2:1	

Section 5: 6–Lead Packages

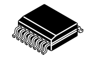
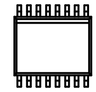
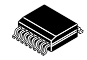
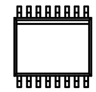
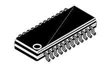
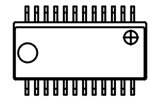
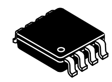
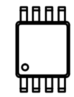
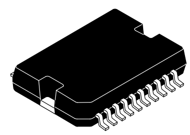
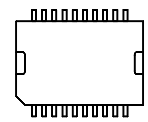
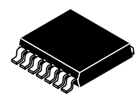
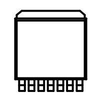
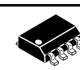
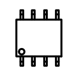
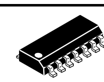
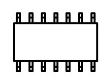
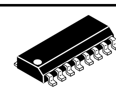
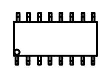
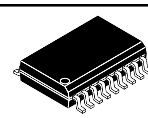
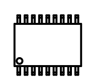
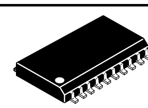
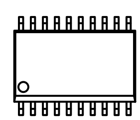
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Surface Mount Gull Wing	SO	SC–74	CASE NO. 318F (page 66)	 SCALE 2:1	
Surface Mount Gull Wing	SO	**TSOP–6** SOT23–6, SC59–6	CASE NO. 318G (page 67)	 SCALE 2:1	
Surface Mount Gull Wing	SO	SC–74R	CASE NO. 318AA (page 68)	 SCALE 2:1	
Surface Mount Gull Wing	SO	**SC–88** SOT–363, SC70–6	CASE NO. 419B (page 88)	 SCALE 2:1	
Surface Mount Flat Lead	SO	SOT–563	CASE NO. 463A (page 93)	 SCALE 2:1	
Surface Mount Flat Lead	SO	SOT–963	CASE NO. 527AA (page 177)	 SCALE 4:1	
Surface Mount Flat Lead	SO	SOT–963	CASE NO. 527AD (page 178)	 SCALE 4:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 6: Multi‐Leaded Packages

Flat Pack	FP	SOP−16	CASE NO. 484 (page 96)	 SCALE 1:1	
Flat Pack	FP	QSOP−16	CASE NO. 492 (page 123)	 SCALE 1:1	
Flat Pack	FP	QSOP−24	CASE NO. 492B (page 124)	 SCALE 1:1	
Surface Mount	SO	US8	CASE NO. 493 (page 124)	 SCALE 4 :1	
Flat Pack	FP	PSOP−20	CASE NO. 525AA (page 176)	 SCALE 1:1	
Surface Mount	SO	SPAK 7−Lead	CASE NO. 553AA (page 179)	 SCALE 1:1	
Surface Mount	SO	SO−8	CASE NO. 751 (page 194)	 SCALE 1:1	
Surface Mount	SO	SO−14	CASE NO. 751A (page 195)	 SCALE 1:1	
Surface Mount	SO	SO−16	CASE NO. 751B (page 196)	 SCALE 1:1	
Surface Mount	SO	SO−18, WIDE BODY	CASE NO. 751C (page 197)	 SCALE 1:1	
Surface Mount	SO	SO−20L	CASE NO. 751D (page 197)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

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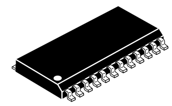
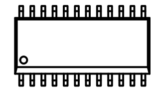
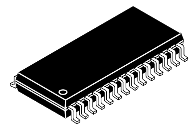
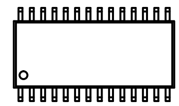
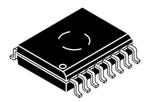
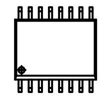
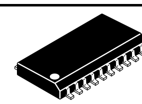
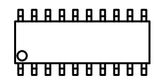
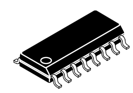
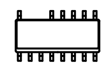
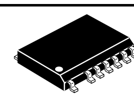
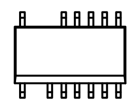
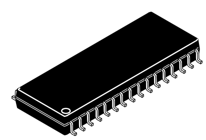
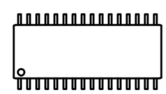
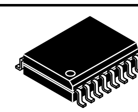
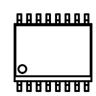
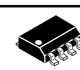
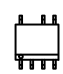
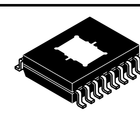
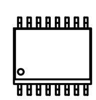
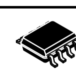
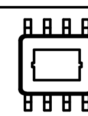
Surface Mount	SO	SO−24L	CASE NO. 751E (page 198)	 SCALE 1:1	
Surface Mount	SO	SO−28L	CASE NO. 751F (page 198)	 SCALE 1:1	
Surface Mount	SO	SOP−16L	CASE NO. 751G (page 199)	 SCALE 1:1	
Surface Mount	SO	SO−20 EIAJ	CASE NO. 751J (page 199)	 SCALE 1:1	
Surface Mount	SO	SO−16 Missing Leads	CASE NO. 751K (page 200)	 SCALE 1:1	
Surface Mount	SO	SO−16 Wide Body Missing Leads	CASE NO. 751N (page 200)	 SCALE 1:1	
Surface Mount	SO	SO−32 Wide	CASE NO. 751P (page 201)	 SCALE 1:1	
Surface Mount	SO	SO−16L Wide Body Exposed Pad	CASE NO. 751R (page 201)	 SCALE 1:1	
Surface Mount	SO	SO−7	CASE NO. 751U (page 202)	 SCALE 1:1	
Surface Mount	SO	SO−16 Wide Body Exposed Pad	CASE NO. 751AB (page 203)	 SCALE 1:1	
Surface Mount	SO	SO−8 Exposed Pad	CASE NO. 751AC (page 203)	 SCALE 1:1	

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SURFACE MOUNT

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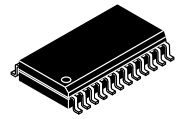
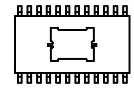
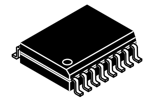
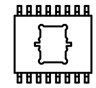
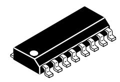
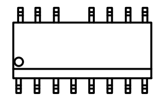
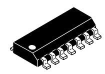
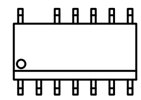
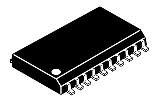
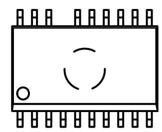
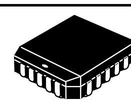
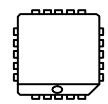
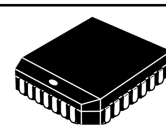
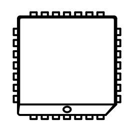
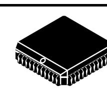
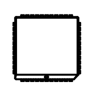
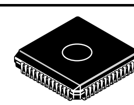
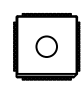
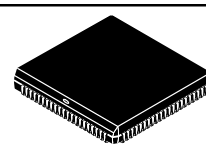
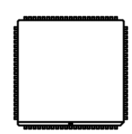
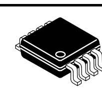
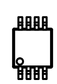
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Surface Mount	SO	SO−24 Wide Body Exposed Pad	CASE NO. 751AE (page 204)	 SCALE 1:1	
Surface Mount	SO	SO−16 Wide Body Exposed Pad	CASE NO. 751AG (page 204)	 SCALE 1:1	
Surface Mount	SO	SO−16 Less Pin 13	CASE NO. 751AM (page 205)	 SCALE 1:1	
Surface Mount	SO	SO−14 Less Pin 13	CASE NO. 751AN (page 205)	 SCALE 1:1	
Surface Mount	SO	SO−20 Less Pin 17	CASE NO. 752AA (page 206)	 SCALE 1:1	
Chip Carrier	CC	PLCC−20	CASE NO. 775 (page 210)	 SCALE 1:1	
Chip Carrier	CC	PLCC−28	CASE NO. 776 (page 211)	 SCALE 1:1	
Chip Carrier	CC	PLCC−44	CASE NO. 777 (page 212)	 SCALE 1:2	
Chip Carrier	CC	PLCC−52	CASE NO. 778B (page 213)	 SCALE 1:2	
Chip Carrier	CC	PLCC−84	CASE NO. 780 (page 214)	 SCALE 1:2	
Surface Mount	SO	**Micro8**™ MSOP−8	CASE NO. 846A (page 217)	 SCALE 2:1	

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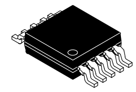
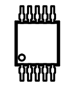
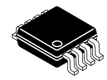
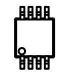
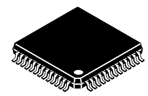
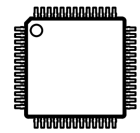
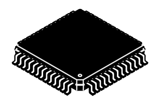
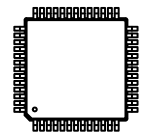
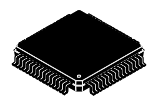
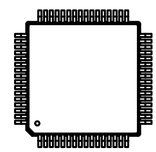
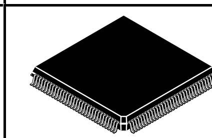
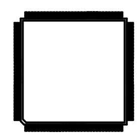
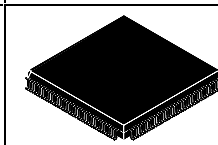
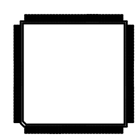
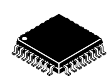
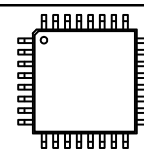
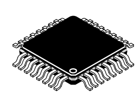
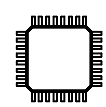
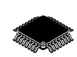
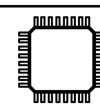
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 6: Multi–Leaded Packages

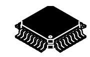
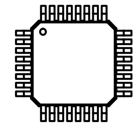
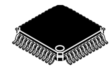
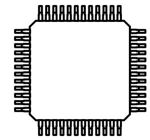
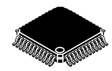
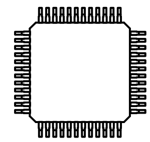
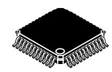
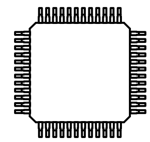
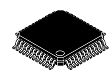
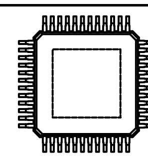
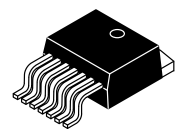
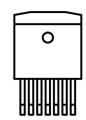
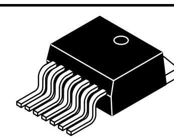
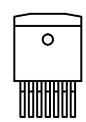
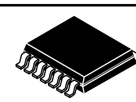
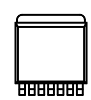
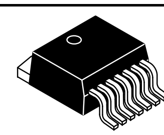
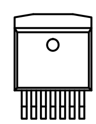
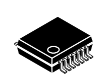
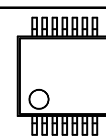
Surface Mount	SO	**Micro10** MSOP–10	CASE NO. 846B (page 218)	 SCALE 2:1	
Surface Mount	SO	**Micro8**™ TSSOP–8, 3x3	CASE NO. 846AA (page 220)	 SCALE 2:1	
Flat Pack	FP	LQFP–52	CASE NO. 848D (page 221)	 SCALE 1:1	
Flat Pack	FP	LQFP–52 Exposed Pad	CASE NO. 848H (page 222)	 SCALE 1:1	
Flat Pack	FP	LQFP–64 Exposed Pad	CASE NO. 848G (page 223)	 SCALE 1:1	
Flat Pack	FP	QFP–128	CASE NO. 862A (page 225)	 SCALE 1:2	
Flat Pack	FP	QFP–160	CASE NO. 864A (page 226)	 SCALE 1:2	
Flat Pack	FP	TQFP–32	CASE NO. 873 (page 227)	 SCALE 1:1	
Flat Pack	FP	LQFP–32	CASE NO. 873A (page 228)	 SCALE 1:1	
Flat Pack	FP	TQFP–32	CASE NO. 873B (page 229)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 6: Multi−Leaded Packages

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Flat Pack	FP	TQFP−32	CASE NO. 873F (page 230)	 SCALE 1:1	
Flat Pack	FP	TQFP−48	CASE NO. 932 (page 232)	 SCALE 1:1	
Flat Pack	FP	TQFP−48	CASE NO. 932F (page 233)	 SCALE 1:1	
Flat Pack	FP	LQFP−48	CASE NO. 932AA (page 234)	 SCALE 1:1	
Flat Pack	FP	TQFP−48 EP, 7x7	CASE NO. 932AB (page 235)	 SCALE 1:1	
Surface Mount	SO	D^{2}PAK Short 7−Lead (DSP7)	CASE NO. 936H (page 238)	 SCALE 1:1	
Surface Mount	SO	D^{2}PAK 7−Lead (DSP7)	CASE NO. 936G (page 238)	 SCALE 1:1	
Surface Mount	SO	D^{2}PAK 7−Lead PowerFLEX	CASE NO. 936J (page 239)	 SCALE 1:1	
Surface Mount	SO	D^{2}PAK Short Lead	CASE NO. 936AB (page 240)	 SCALE 1:1	
Surface Mount	SO	SSOP−14	CASE NO. 940A (page 241)	 SCALE 1:1	

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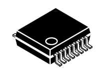
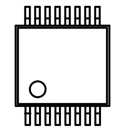
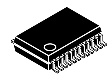
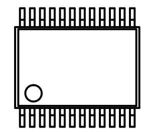
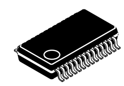
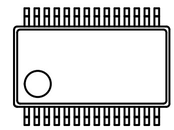
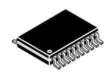
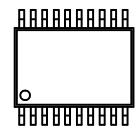
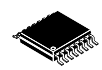
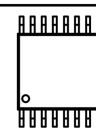
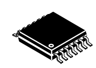
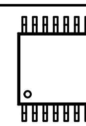
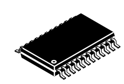
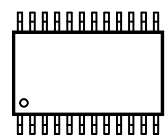
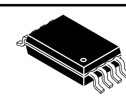
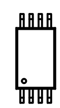
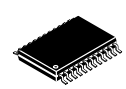
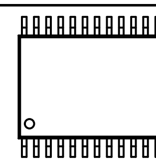
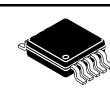
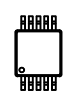
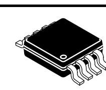
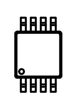
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 6: Multi−Leaded Packages

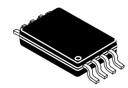
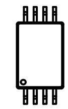
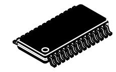
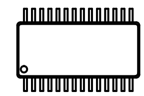
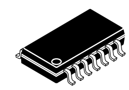
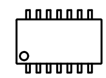
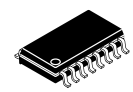
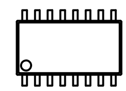
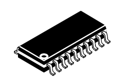
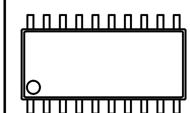
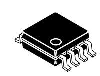
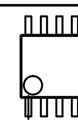
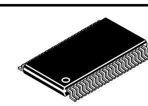
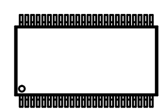
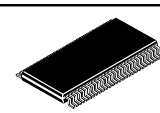
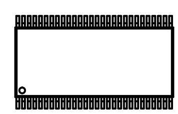
Surface Mount	SO	SSOP−16	CASE NO. 940B (page 241)	 SCALE 1:1	
Surface Mount	SO	SSOP−24	CASE NO. 940D (page 242)	 SCALE 1:1	
Surface Mount	SO	SSOP−28	CASE NO. 940J (page 243)	 SCALE 1:1	
Surface Mount	SO	TSSOP−20	CASE NO. 948E (page 244)	 SCALE 1:1	
Surface Mount	SO	TSSOP−16	CASE NO. 948F (page 245)	 SCALE 1:1	
Surface Mount	SO	TSSOP−14	CASE NO. 948G (page 246)	 SCALE 1:1	
Surface Mount	SO	TSSOP−24	CASE NO. 948H (page 247)	 SCALE 1:1	
Surface Mount	SO	**TSSOP−8**	CASE NO. 948J (page 248)	 SCALE 2:1	
Surface Mount	SO	TSSOP−24 Wide Body	CASE NO. 948K (page 248)	 SCALE 1:1	
Surface Mount	SO	TSSOP−10	CASE NO. 948P (page 249)	 SCALE 2:1	
Surface Mount	SO	**TSSOP−8** Micro8	CASE NO. 948R (page 249)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 6: Multi−Leaded Packages

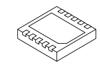
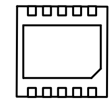
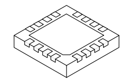
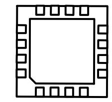
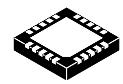
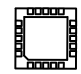
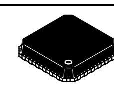
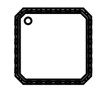
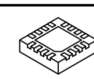
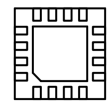
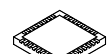
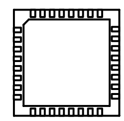
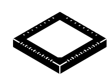
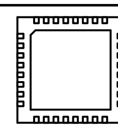
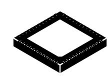
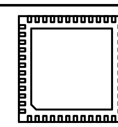
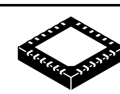
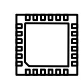
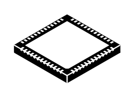
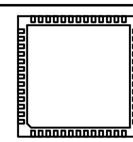
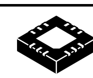
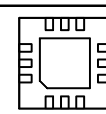
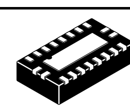
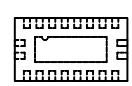
Surface Mount	SO	TSSOP−8 0.65mm Pitch	CASE NO. 948S (page 250)	 SCALE 2:1	
Surface Mount	SO	TSSOP−28	CASE NO. 948AA (page 247)	 SCALE 1:1	
Surface Mount	SO	EIAJ−14	CASE NO. 965 (page 251)	 SCALE 1:1	
Surface Mount	SO	EIAJ−16	CASE NO. 966 (page 252)	 SCALE 1:1	
Surface Mount	SO	EIAJ−20	CASE NO. 967 (page 252)	 SCALE 1:1	
Surface Mount	SO	EIAJ−8	CASE NO. 968 (page 253)	 SCALE 1:1	
Surface Mount	SO	TSSOP−48	CASE NO. 1201 (page 247)	 SCALE 1:1	
Surface Mount	SO	TSSOP−56	CASE NO. 1202 (page 247)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 7: Leadless/QFN/DFN Packages

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
MicroLeadless	HP	DFN10 3x3	CASE NO. 485C (page 97)	 SCALE 2:1	
MicroLeadless	HP	QFN16 4x4	CASE NO. 485D (page 98)	 SCALE 2:1	
MicroLeadless	HP	QFN20 4x4	CASE NO. 485E (page 98)	 SCALE 2:1	
MicroLeadless	HP	24−PIN MLF 4x4	CASE NO. 485F (page 99)	 SCALE 2:1	
MicroLeadless	HP	QFN16 3x3	CASE NO. 485G (page 100)	 SCALE 2:1	
MicroLeadless	HP	QFN32 7x7	CASE NO. 485H (page 100)	 SCALE 1:1	
MicroLeadless	HP	QFN32 7x7	CASE NO. 485J (page 101)	 SCALE 1:1	
MicroLeadless	HP	QFN48 7x7	CASE NO. 485K (page 101)	 SCALE 1:1	
MicroLeadless	HP	QFN24 4x4	CASE NO. 485L (page 102)	 SCALE 2:1	
MicroLeadless	HP	QFN52 8x8	CASE NO. 485M (page 102)	 SCALE 1:1	
MicroLeadless	HP	QFN12 3x3	CASE NO. 485N (page 103)	 SCALE 2:1	
MicroLeadless	HP	QFN20 2.5x4.5	CASE NO. 485AA (page 103)	 SCALE 2:1	

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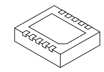
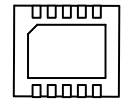
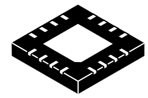
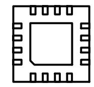
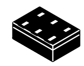
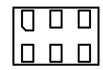
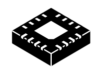
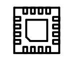
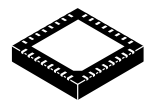
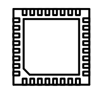
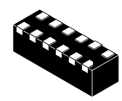
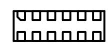
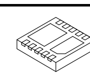
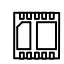
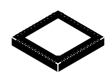
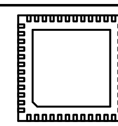
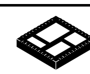
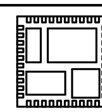
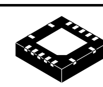
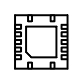
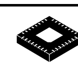
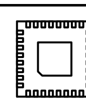
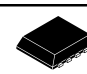
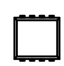
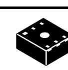
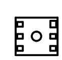
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 7: Leadless/QFN/DFN Packages

MicroLeadless	HP	DFN10 3.5x3	CASE NO. 485AB (page 104)	 SCALE 2:1	
MicroLeadless	HP	QFN16 5x5	CASE NO. 485AC (page 104)	 SCALE 2:1	
MicroLeadless	HP	6−PIN BT QFN 1.5x1	CASE NO. 485AD (page 105)	 SCALE 4:1	
MicroLeadless	HP	QFN16 3x3	CASE NO. 485AE (page 105)	 SCALE 2:1	
MicroLeadless	HP	QFN32 5x5	CASE NO. 485AF (page 106)	 SCALE 2:1	
MicroLeadless	HP	WDFN12 3x1	CASE NO. 485AG (page 106)	 SCALE 4:1	
MicroLeadless	HP	DFN10 3x3	CASE NO. 485AH (page 107)	 SCALE 2:1	
MicroLeadless	HP	QFN48 7x7	CASE NO. 485AJ (page 107)	 SCALE 1:1	
MicroLeadless	HP	QFN40 6x6	CASE NO. 485AK (page 108)	 SCALE 1:1	
MicroLeadless	HP	QFN14 3.5x3.5	CASE NO. 485AL (page 109)	 SCALE 2:1	
MicroLeadless	HP	QFN32 5x5	CASE NO. 485AM (page 110)	 SCALE 2:1	
MicroLeadless	HP	SON−8	CASE NO. 486 (page 110)	 SCALE 2:1	
MicroLeadless	HP	**DFN6 2x2.2** SC70−LLS	CASE NO. 488 (page 111)	 SCALE 2:1	

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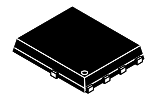
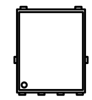
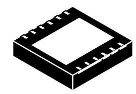
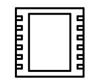
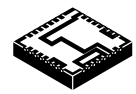
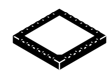
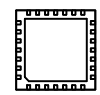
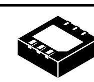
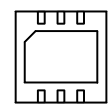
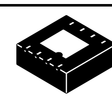
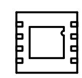
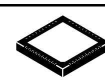
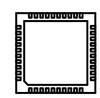
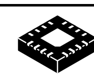
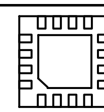
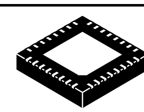
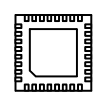
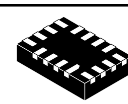
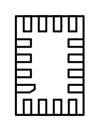
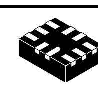
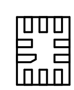
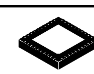
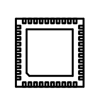
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

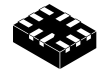
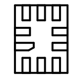
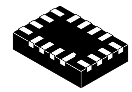
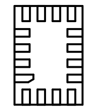
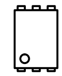
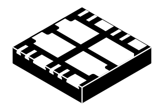
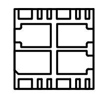
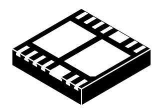
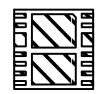
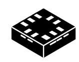
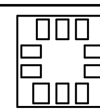
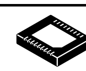
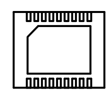
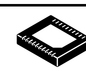
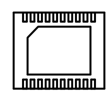
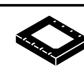
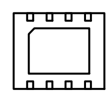
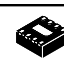
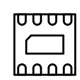
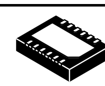
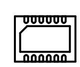
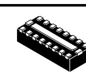
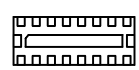
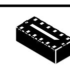
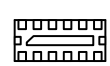
Section 7: Leadless/QFN/DFN Packages

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
MicroLeadless	HP	**DFN6 5x6** SO8 FL	CASE NO. 488AA (page 112)	 SCALE 2:1	
MicroLeadless	HP	12−PIN PLLP 9x9	CASE NO. 488AB (page 113)	 SCALE 1:1	
MicroLeadless	HP	32−PIN PLLP 9x9	CASE NO. 488AC (page 114)	 SCALE 1:1	
MicroLeadless	HP	QFN28 7x7	CASE NO. 488AD (page 115)	 SCALE 1:1	
MicroLeadless	HP	DFN6 3x3	CASE NO. 488AE (page 115)	 SCALE 2:1	
MicroLeadless	HP	DFN8 4x4	CASE NO. 488AF (page 116)	 SCALE 2:1	
MicroLeadless	HP	QFN40 7x7	CASE NO. 488AG (page 116)	 SCALE 1:1	
MicroLeadless	HP	QFN16 3x3	CASE NO. 488AK (page 117)	 SCALE 2:1	
MicroLeadless	HP	QFN32 5x5	CASE NO. 488AM (page 117)	 SCALE 2:1	
MicroLeadless	HP	WQFN16 1.8x2.6	CASE NO. 488AP (page 118)	 SCALE 4:1	
MicroLeadless	HP	WQFN10 1.4x1.8	CASE NO. 488AQ (page 118)	 SCALE 4:1	
MicroLeadless	HP	QFN40 6x6	CASE NO. 488AR (page 119)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

SURFACE MOUNT

Section 7: Leadless/QFN/DFN Packages

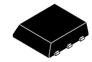
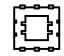
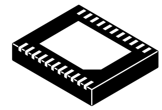
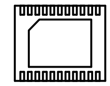
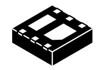
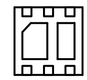
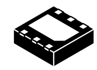
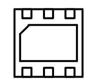
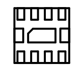
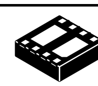
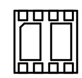
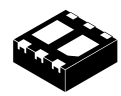
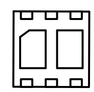
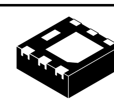
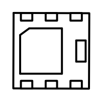
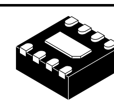
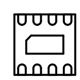
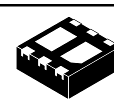
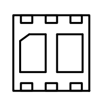
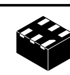
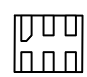
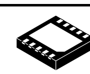
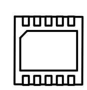
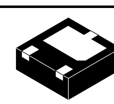
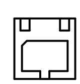
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
MicroLeadless	HP	UQFN10 1.4x1.8	CASE NO. 488AT (page 120)	 SCALE 4:1	
MicroLeadless	HP	UQFN16 1.8x2.6	CASE NO. 488AU (page 121)	 SCALE 4:1	
MicroLeadless	HP	SON−6	CASE NO. 494 (page 125)	 SCALE 2:1	
MicroLeadless	HE	FBIP (Full Bridge Integrated Package)	CASE NO. 495 (page 125)	 SCALE 1:1	
MicroLeadless	HE	QFN14 10.5x10.5	CASE NO. 495A (page 126)	 SCALE 1:1	
MicroLeadless	HP	QFN10 3x3	CASE NO. 501 (page 140)	 SCALE 2:1	
MicroLeadless	HP	DFN18 6x5	CASE NO. 505 (page 142)	 SCALE 1:1	
MicroLeadless	HP	DFN20 6x5	CASE NO. 505AB (page 142)	 SCALE 1:1	
MicroLeadless	HP	DFN8 6x5	CASE NO. 505AC (page 143)	 SCALE 1:1	
MicroLeadless	HP	DFN8 2x2	CASE NO. 506AA (page 143)	 SCALE 2:1	
MicroLeadless	HP	DFN12 4x3	CASE NO. 506AB (page 144)	 SCALE 2:1	
MicroLeadless	HP	DFN16 4x1.6	CASE NO. 506AC (page 144)	 SCALE 2:1	
MicroLeadless	HP	DFN12 3x1.35	CASE NO. 506AD (page 145)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

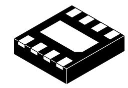
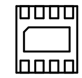
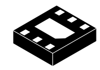
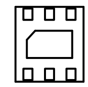
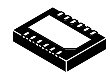
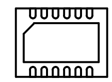
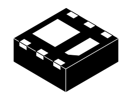
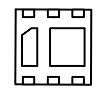
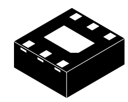
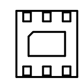
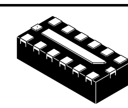
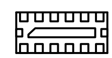
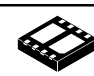
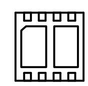
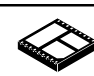
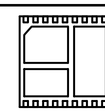
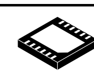
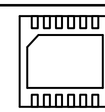
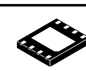
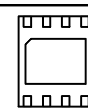
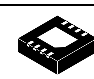
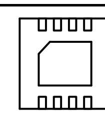
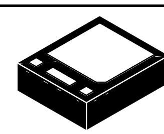
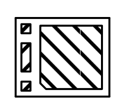
Section 7: Leadless/QFN/DFN Packages

MicroLeadless	HP	HSON−6	CASE NO. 506AE (page 145)	 SCALE 2:1	
MicroLeadless	HP	DFN22 6x5	CASE NO. 506AF (page 146)	 SCALE 2:1	
MicroLeadless	HP	DFN6 3x3	CASE NO. 506AG (page 146)	 SCALE 2:1	
MicroLeadless	HP	DFN6 3x3	CASE NO. 506AH (page 147)	 SCALE 2:1	
MicroLeadless	HP	DFN8 1.6x1.6	CASE NO. 506AK (page 147)	 SCALE 2:1	
MicroLeadless	HP	DFN8 3.3x3.3	CASE NO. 506AL (page 148)	 SCALE 2:1	
MicroLeadless	HP	WDFN6 2x2	CASE NO. 506AN (page 148)	 SCALE 4:1	
MicroLeadless	HP	WDFN6 2x2	CASE NO. 506AP (page 149)	 SCALE 4:1	
MicroLeadless	HP	DFN8 2x2	CASE NO. 506AQ (page 149)	 SCALE 2:1	
MicroLeadless	HP	DFN6 3x3	CASE NO. 506AR (page 150)	 SCALE 2:1	
MicroLeadless	HP	WDFN6 1.2x1	CASE NO. 506AS (page 150)	 SCALE 4:1	
MicroLeadless	HP	UDFN10 3x3	CASE NO. 506AT (page 151)	 SCALE 2:1	
MicroLeadless	HP	WDFN3 2x2	CASE NO. 506AU (page 151)	 SCALE 4:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

SURFACE MOUNT

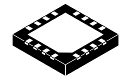
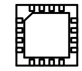
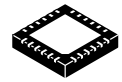
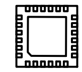
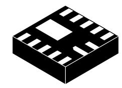
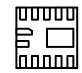
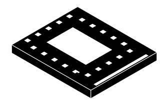
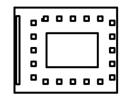
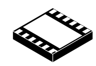
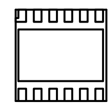
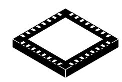
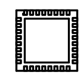
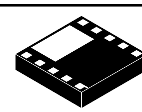
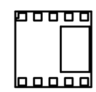
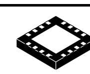
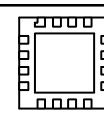
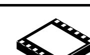
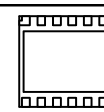
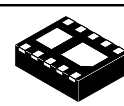
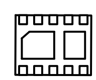
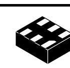
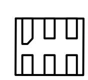
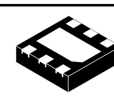
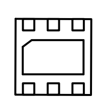
Section 7: Leadless/QFN/DFN Packages

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
MicroLeadless	HP	UDFN8 2x2.2	CASE NO. 506AV (page 152)	 SCALE 4:1	
MicroLeadless	HP	DFN6 3x3.3	CASE NO. 506AX (page 152)	 SCALE 2:1	
MicroLeadless	HP	WDFN12 3x4	CASE NO. 506AY (page 153)	 SCALE 2:1	
MicroLeadless	HP	WDFN6 2x2	CASE NO. 506AZ (page 153)	 SCALE 4:1	
MicroLeadless	HP	DFN6 2x2.2	CASE NO. 506BA (page 154)	 SCALE 2:1	
MicroLeadless	HP	WDFN12 3x1.35	CASE NO. 506BB (page 154)	 SCALE 4:1	
MicroLeadless	HP	DFN8 3x3	CASE NO. 506BC (page 155)	 SCALE 2:1	
MicroLeadless	HP	DFN18 6x6	CASE NO. 506BD (page 155)	 SCALE 1:1	
MicroLeadless	HP	DFN12 3x3	CASE NO. 506BE (page 156)	 SCALE 2:1	
MicroLeadless	HP	DFN8 5x6	CASE NO. 506BG (page 156)	 SCALE 1:1	
MicroLeadless	HP	DFN8 3x3	CASE NO. 506BJ (page 157)	 SCALE 2:1	
MicroLeadless	HP	PLLP4	CASE NO. 508AA (page 158)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

SURFACE MOUNT

Section 7: Leadless/QFN/DFN Packages

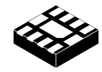
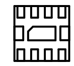
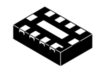
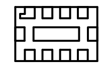
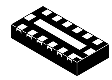
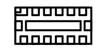
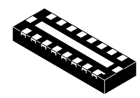
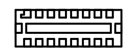
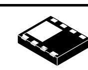
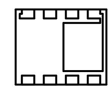
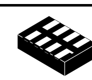
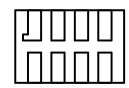
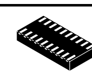
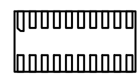
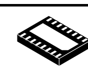
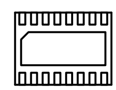
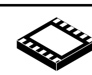
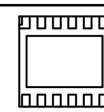
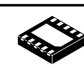
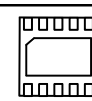
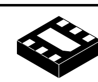
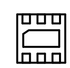
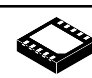
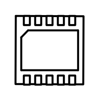
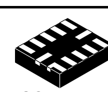
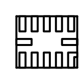
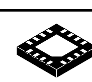
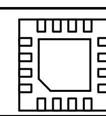
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
MicroLeadless	HP	QFN16 4x4	CASE NO. 510AB (page 159)	 SCALE 2:1	
MicroLeadless	HP	QFN24 4x4	CASE NO. 511AA (page 159)	 SCALE 2:1	
MicroLeadless	HP	LLGA12, 2x2	CASE NO. 513AA (page 160)	 SCALE 4:1	
MicroLeadless	HP	TLLGA20, 6x5	CASE NO. 513AC (page 161)	 SCALE 2:1	
MicroLeadless	HP	LLGA12, 3x3	CASE NO. 513AD (page 162)	 SCALE 2:1	
MicroLeadless	HP	TLLGA32, 4x4	CASE NO. 513AE (page 162)	 SCALE 2:1	
MicroLeadless	HP	LLGA10, 2.5x2.5	CASE NO. 513AG (page 163)	 SCALE 4:1	
MicroLeadless	HP	LLGA16, 3x3	CASE NO. 513AJ (page 163)	 SCALE 2:1	
MicroLeadless	HP	LLGA12, 3x3	CASE NO. 513AK (page 164)	 SCALE 2:1	
MicroLeadless	HP	WDFN10 2.5x2	CASE NO. 516AA (page 165)	 SCALE 4:1	
MicroLeadless	HP	UDFN6 1.2x1	CASE NO. 517AA (page 166)	 SCALE 4:1	
MicroLeadless	HP	UDFN6 2x2	CASE NO. 517AB (page 166)	 SCALE 4:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 7: Leadless/QFN/DFN Packages

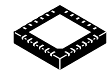
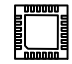
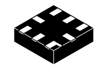
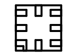
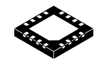
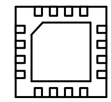
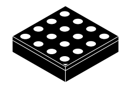
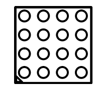
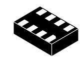
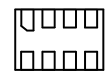
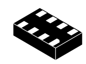
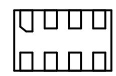
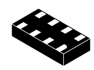
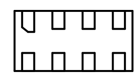
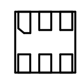
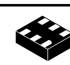
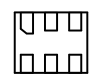
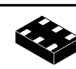
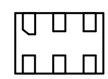
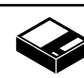
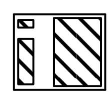
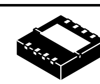
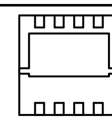
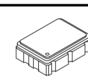
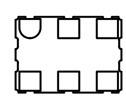
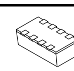
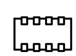
MicroLeadless	HP	UDFN8 1.6x1.6	CASE NO. 517AC (page 167)	 SCALE 4:1	
MicroLeadless	HP	UDFN8 1.8x1.2	CASE NO. 517AD (page 167)	 SCALE 2:1	
MicroLeadless	HP	UDFN12 2.5x1.2	CASE NO. 517AE (page 168)	 SCALE 4:1	
MicroLeadless	HP	UDFN16 3.5x1.2	CASE NO. 517AF (page 168)	 SCALE 4:1	
MicroLeadless	HP	LLGA8 3x2.5	CASE NO. 517AH (page 169)	 SCALE 2:1	
MicroLeadless	HP	UDFN8 1.8x1.2	CASE NO. 517AJ (page 169)	 SCALE 4:1	
MicroLeadless	HP	UDFN20 4x2	CASE NO. 517AK (page 170)	 SCALE 2:1	
MicroLeadless	HP	UDFN16 3.2x2.4	CASE NO. 517AL (page 170)	 SCALE 2:1	
MicroLeadless	HP	UDFN12 3x3	CASE NO. 517AM (page 171)	 SCALE 2:1	
MicroLeadless	HP	UDFN10 2.6x2.6	CASE NO. 517AN (page 171)	 SCALE 2:1	
MicroLeadless	HP	UDFN6 1.6x1.6	CASE NO. 517AP (page 172)	 SCALE 4:1	
MicroLeadless	HP	WDFN10 3x3	CASE NO. 522AA (page 172)	 SCALE 2:1	
MicroLeadless	HP	UQFN12 1.7x2	CASE NO. 523AE (page 173)	 SCALE 4:1	
MicroLeadless	HP	UQFN16 3x3	CASE NO. 523AF (page 173)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 7: Leadless/QFN/DFN Packages

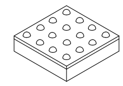
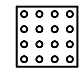
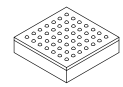
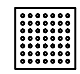
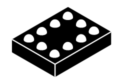
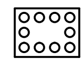
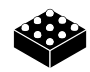
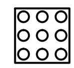
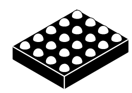
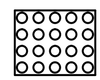
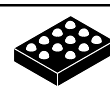
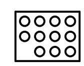
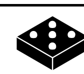
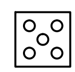
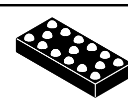
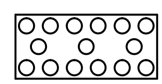
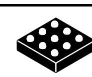
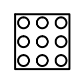
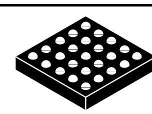
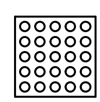
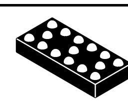
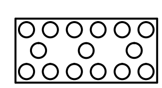
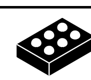
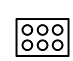
MicroLeadless	HP	UQFN24 3.5x3.5	CASE NO. 523AG (page 174)	 SCALE 2:1	
MicroLeadless	HP	UQFN8 1.5x1.5	CASE NO. 523AH (page 174)	 SCALE 4:1	
MicroLeadless	HP	UQFN16 3x3	CASE NO. 523AJ (page 175)	 SCALE 2:1	
MicroLeadless	HP	16 Pin LGA 4x4	CASE NO. 526AB (page 177)	 SCALE 2:1	
MicroLeadless	HP	ULLGA8 1.45x1	CASE NO. 613AA (page 180)	 SCALE 4:1	
MicroLeadless	HP	ULLGA8 1.6x1	CASE NO. 613AB (page 180)	 SCALE 4:1	
MicroLeadless	HP	ULLGA8 1.95x1	CASE NO. 613AC (page 181)	 SCALE 4:1	
MicroLeadless	HP	ULLGA6 1x1	CASE NO. 613AD (page 181)	 SCALE 4:1	
MicroLeadless	HP	ULLGA6 1.2x1	CASE NO. 613AE (page 182)	 SCALE 4:1	
MicroLeadless	HP	ULLGA6 1.45x1	CASE NO. 613AF (page 182)	 SCALE 4:1	
MicroLeadless	HE	SO−8 Leadless	CASE NO. 751S (page 202)	 SCALE 1:1	
MicroLeadless	HP	Micro8 Leadless	CASE NO. 846C (page 219)	 SCALE 2:1	
MicroLeadless	HP	Micro8 Leadless	CASE NO. 848AB (page 224)	 SCALE 1:1	
MicroLeadless™	HP	ChipFET™ Leadless	CASE NO. 1206A (page 253)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 8: Flip–Chip/BGA Packages

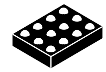
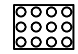
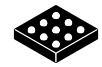
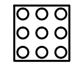
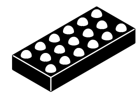
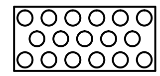
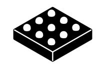
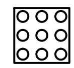
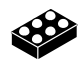
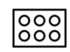
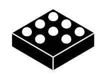
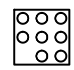
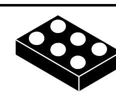
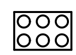
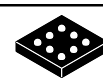
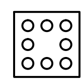
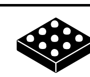
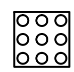
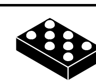
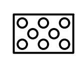
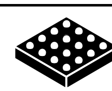
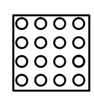
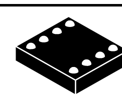
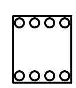
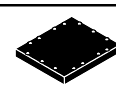
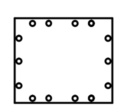
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
BGA	NA	16–Pin BGA	CASE NO. 489 (page 122)	 SCALE 2:1	
BGA	NA	49–Pin BGA	CASE NO. 489A (page 122)	 SCALE 1:1	
Flip–Chip	NA	10–Pin Flip–Chip	CASE NO. 489AA (page 123)	 SCALE 4:1	
Flip–Chip	NA	9–Pin Flip–Chip	CASE NO. 499 (page 127)	 SCALE 4:1	
Flip–Chip	NA	20–Pin Flip–Chip	CASE NO. 499A (page 128)	 SCALE 4:1	
Flip–Chip	NA	11–Pin Flip–Chip	CASE NO. 499B (page 128)	 SCALE 4:1	
Flip–Chip	NA	5–Pin Flip–Chip	CASE NO. 499C (page 129)	 SCALE 4:1	
Flip–Chip	NA	15–Pin Flip–Chip	CASE NO. 499D (page 129)	 SCALE 4:1	
Flip–Chip	NA	9–Pin Flip–Chip	CASE NO. 499E (page 130)	 SCALE 4:1	
Flip–Chip	NA	25–Pin Flip–Chip	CASE NO. 499G (page 130)	 SCALE 4:1	
Flip–Chip	NA	15–Pin Flip–Chip	CASE NO. 499H (page 131)	 SCALE 4:1	
Flip–Chip	NA	6–Pin Flip–Chip	CASE NO. 499J (page 131)	 SCALE 4:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

Section 8: Flip−Chip/BGA Packages

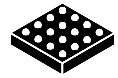
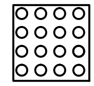
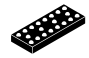
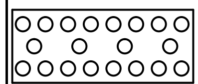
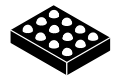
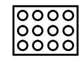
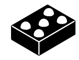
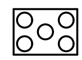
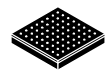
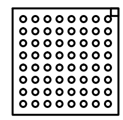
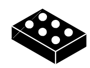
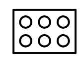
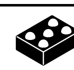
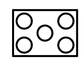
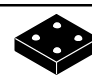
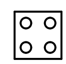
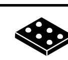
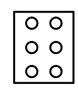
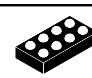
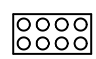
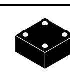
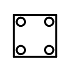
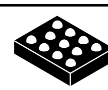
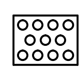
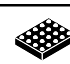
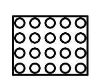
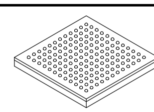
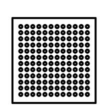
Flip−Chip	NA	12−Pin Flip−Chip	CASE NO. 499AB (page 132)	 SCALE 4:1	
Flip−Chip	NA	9−Pin Flip−Chip	CASE NO. 499AC (page 132)	 SCALE 4:1	
Flip−Chip	NA	17−Pin Flip−Chip	CASE NO. 499AD (page 133)	 SCALE 4:1	
Flip−Chip	NA	9−Pin Flip−Chip	CASE NO. 499AE (page 133)	 SCALE 4:1	
Flip−Chip	NA	6−Pin Flip−Chip	CASE NO. 499AF (page 134)	 SCALE 4:1	
Flip−Chip	NA	8−Pin Flip−Chip	CASE NO. 499AG (page 134)	 SCALE 4:1	
Flip−Chip	NA	6−Pin Flip−Chip	CASE NO. 499AH (page 135)	 SCALE 4:1	
Flip−Chip	NA	8−Pin Flip−Chip	CASE NO. 499AJ (page 135)	 SCALE 4:1	
Flip−Chip	NA	9−Pin Flip−Chip	CASE NO. 499AL (page 136)	 SCALE 4:1	
Flip−Chip	NA	8−Pin Flip−Chip	CASE NO. 499AM (page 136)	 SCALE 4:1	
Flip−Chip	NA	16−Pin Flip−Chip	CASE NO. 499AN (page 137)	 SCALE 4:1	
Flip−Chip	NA	8−Pin Flip−Chip	CASE NO. 499AP (page 137)	 SCALE 4:1	
Flip−Chip	NA	14−Pin Flip−Chip	CASE NO. 499AQ (page 138)	 SCALE 2:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

SURFACE MOUNT

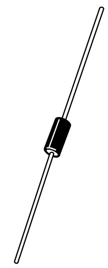
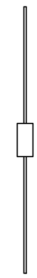
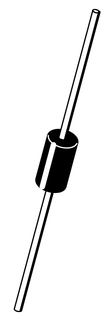
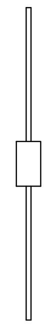
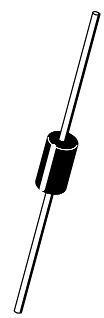
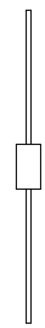
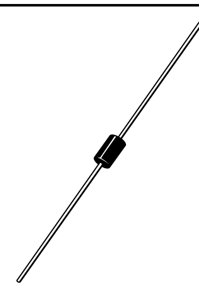
Section 8: Flip−Chip/BGA Packages

Flip−Chip	NA	16−Pin Flip−Chip	CASE NO. 499AR (page 138)	 SCALE 4:1	
Flip−Chip	NA	20−Pin Flip−Chip	CASE NO. 499AS (page 139)	 SCALE 2:1	
Flip−Chip	NA	12−Pin Flip−Chip	CASE NO. 499AU (page 139)	 SCALE 4:1	
Flip−Chip	NA	5−Pin Flip−Chip	CASE NO. 499AY (page 140)	 SCALE 4:1	
BGA	NA	64−Pin LFBGA	CASE NO. 504 (page 141)	 SCALE 1:2	
Flip−Chip	NA	6−Pin Flip−Chip	CASE NO. 766AA (page 206)	 SCALE 4:1	
Flip−Chip	NA	5−Pin Flip−Chip	CASE NO. 766AB (page 207)	 SCALE 4:1	
Flip−Chip	NA	4−Pin Flip−Chip	CASE NO. 766AC (page 207)	 SCALE 4:1	
Flip−Chip	NA	6−Pin Flip−Chip	CASE NO. 766AD (page 208)	 SCALE 4:1	
Flip−Chip	NA	8−Pin Flip−Chip	CASE NO. 766AE (page 208)	 SCALE 4:1	
Flip−Chip	NA	4−Pin Flip−Chip	CASE NO. 766AF (page 208)	 SCALE 4:1	
Flip−Chip	NA	11−Pin Flip−Chip	CASE NO. 766AJ (page 209)	 SCALE 4:1	
Flip−Chip	NA	20−Pin Flip−Chip	CASE NO. 766AK (page 209)	 SCALE 2:1	
BGA	NA	144−BGA	CASE NO. 1242 (page 255)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

THROUGH−HOLE

Section 1: Axial Leaded and Cans

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Molded Axial	LF	SURMETIC™ 40	CASE NO. 017AA (page 44)	 SCALE 1:1	
Molded Axial	LF	MOSORB™	CASE NO. 41 (page 47)	 SCALE 1:1	
Molded Axial	LF	MOSORB™	CASE NO. 41A (page 47)	 SCALE 1:1	
Molded Axial	LF	DO−41	CASE NO. 59A (page 47)	 SCALE 1:1	

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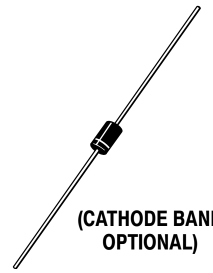
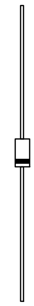
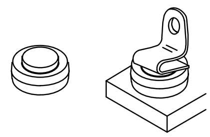
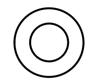
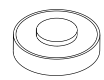
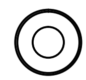
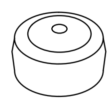
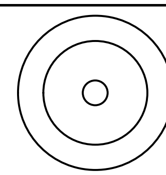
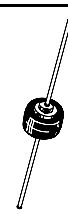
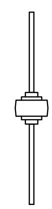
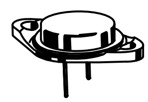
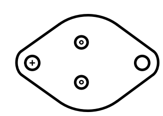
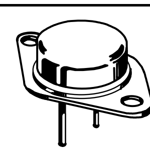
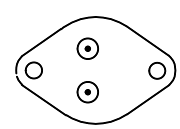
THROUGH−HOLE

Section 1: Axial Leaded and Cans

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Molded Axial	LF	MiniMOSORB™, 1A SURMETIC	CASE NO. 59AA (page 48)	 (CATHODE BAND OPTIONAL) SCALE 1:1	
Disk/Button	DB	MICRODE BUTTON	CASE NO. 193 (page 49)	 SCALE 1:1	
Disk/Button	DB	BUTTON CAN	CASE NO. 193A (page 49)	 SCALE 1:1	
Disk/Button	DB	JUMBO CAN	CASE NO. 193AA (page 50)	 SCALE 1:1	
Disk/Button	DB	AXIAL LEAD BUTTON	CASE NO. 194 (page 50)	 SCALE 1:1	
Disk/Button	DB	**TO−3** TO−204	CASE NO. 197 (page 51)	 SCALE 1:2	
Disk/Button	DB	**TO−3** TO−204	CASE NO. 197A (page 50)	 SCALE 1:2	

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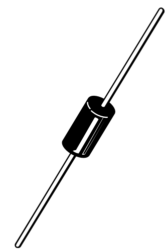
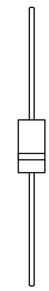
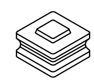
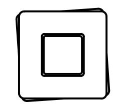
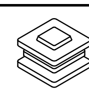
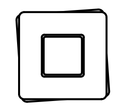
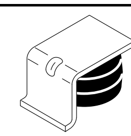
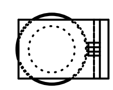
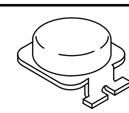
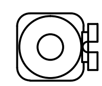
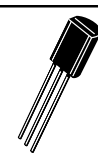
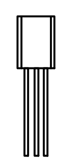
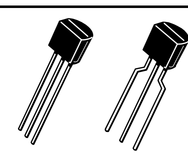
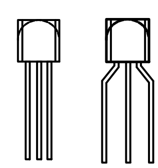
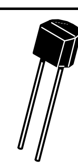
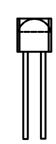
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

THROUGH−HOLE

Section 1: Axial Leaded and Cans

Molded Axial	LF	3A SURMETIC	CASE NO. 267 (page 56)	 SCALE 1:1	
Disk/Button	DB	BUTTON	CASE NO. 416 (page 80)	 SCALE 2:1	
Disk/Button	DB	SSOVP BUTTON	CASE NO. 416A (page 80)	 SCALE 2:1	
Disk/Button	DB	TAB MOUNT BUTTON	CASE NO. 421A (page 90)	 SCALE 1:1	
Disk/Button	DB	TOPCAN	CASE NO. 460 (page 91)	 SCALE 1:1	

Section 2: Non−Axial Cylinder

Non−Axial Cylinder	CY	**TO−92 1−Watt** TO−226AE	CASE NO. 29−10 (page 45)	 SCALE 1:1.5	
Non−Axial Cylinder	CY	**TO−92** TO−226AA	CASE NO. 29−11 (page 46)	 SCALE 1:1.5	
Non−Axial Cylinder	CY	**TO−92 Two Lead** TO−226AC	CASE NO. 182 (page 49)	 SCALE 1:1.5	

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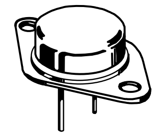
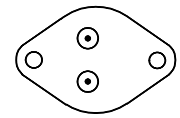
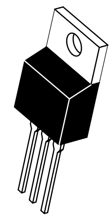
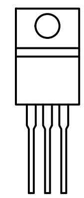
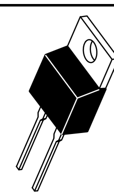
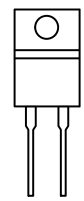
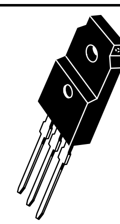
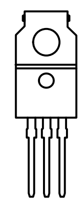
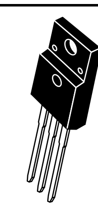
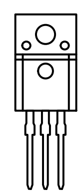
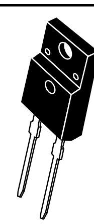
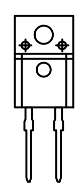
THROUGH−HOLE

Section 3: Flange Mount

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Flange Mounted	FM	**TO−3** **40 mil Pins** TO−204AA	CASE NO. 1−07 (page 44)	 SCALE 1:2	
Flange Mounted	FM	TO−220	CASE NO. 221A (pages 52 & 53)	 SCALE 1:1	
Flange Mounted	FM	TO−220 Two Lead	CASE NO. 221B (page 53)	 SCALE 1:1	
Flange Mounted	FM	TO−220 FULLPACK™ Thyristor	CASE NO. 221C (page 54)	 SCALE 1:1	
Flange Mounted	FM	TO−220 FULLPACK Transistor	CASE NO. 221D (page 54)	 SCALE 1:1	
Flange Mounted	FM	TO−220 FULLPACK Two Lead	CASE NO. 221E (page 55)	 SCALE 1:1	

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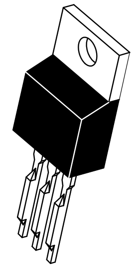
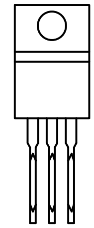
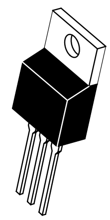
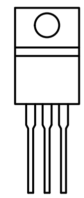
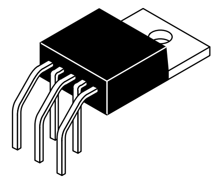
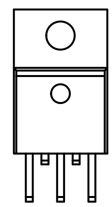
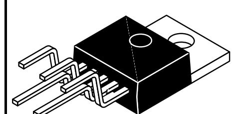
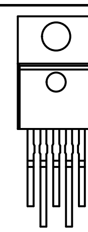
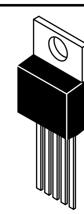
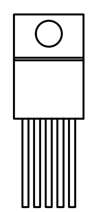
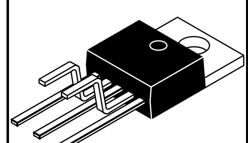
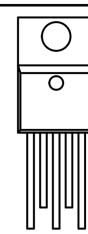
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

THROUGH−HOLE

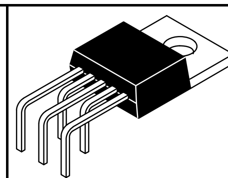
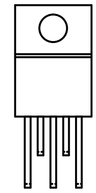
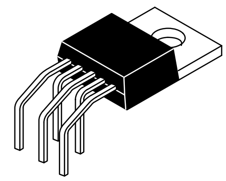
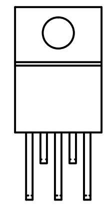
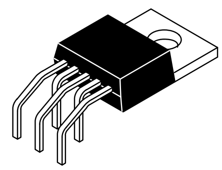
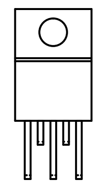
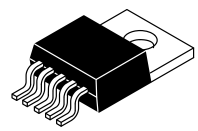
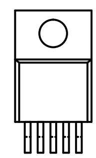
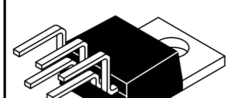
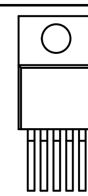
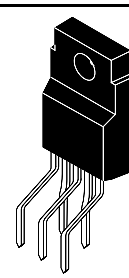
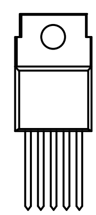
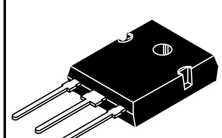
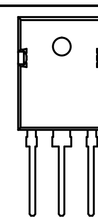
Section 3: Flange Mount

Flange Mounted	FM	**TO−220** TO−220AB	CASE NO. 221K (page 55)	 SCALE 1:1	
Flange Mounted	FM	TO−220 Single Gauge	CASE NO. 221AB (page 56)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (THA5)	CASE NO. 314A (page 57)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (Offset Leads)	CASE NO. 314B (page 58)	 SCALE 1:1	
Flange Mounted	FM	TO−220 Five Lead	CASE NO. 314D (page 58)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (VHVIC)	CASE NO. 314E (page 59)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

THROUGH−HOLE

Section 3: Flange Mount

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Flange Mounted	FM	TO−220 (THB5)	CASE NO. 314F (page 59)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (THC5)	CASE NO. 314G (page 60)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (THD5)	CASE NO. 314H (page 60)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (THE5)	CASE NO. 314J (page 61)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (Bent Leads)	CASE NO. 314K (page 61)	 SCALE 1:1	
Flange Mounted	FM	TO−220 (TFVA5)	CASE NO. 314N (page 62)	 SCALE 1:1	
Flange Mounted	FM	TO−247	CASE NO. 340F (page 69)	 SCALE 1:1	

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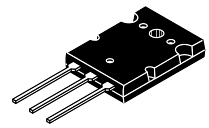
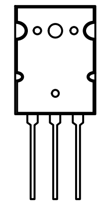
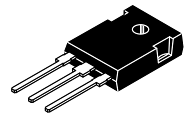
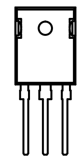
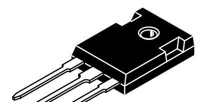
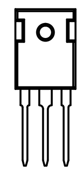
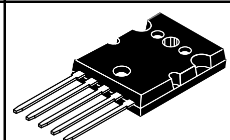
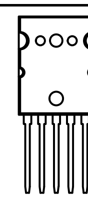
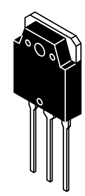
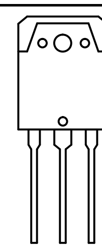
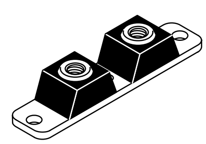
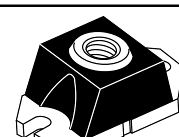
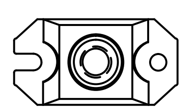
THROUGH−HOLE

Section 3: Flange Mount

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
Flange Mounted	FM	**TO−264** TO−3PBL	CASE NO. 340G (page 69)	 SCALE 1:2	
Flange Mounted	FM	TO−247	CASE NO. 340K (page 70)	 SCALE 1:1	
Flange Mounted	FM	TO−247	CASE NO. 340L (page 70)	 SCALE 1:2	
Flange Mounted	FM	TO−264	CASE NO. 340AA (page 71)	 SCALE 1:2	
Flange Mounted	FM	TO−3P−3LD	CASE NO. 340AB (page 71)	 SCALE 1:2	
Flange Mounted	FM	POWERTAP™ II	CASE NO. 357C (page 72)	 SCALE 1:2	
Flange Mounted	FM	POWERTAP III	CASE NO. 357D (page 72)	 SCALE 1:1	

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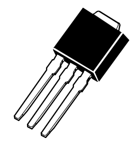
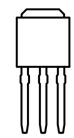
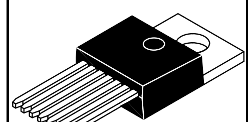
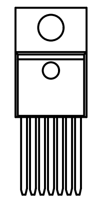
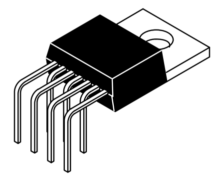
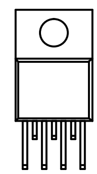
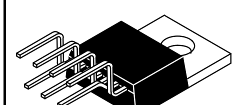
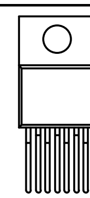
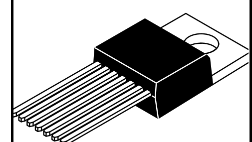
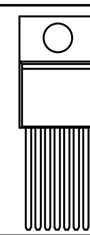
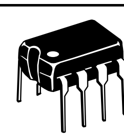
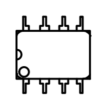
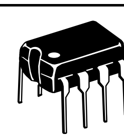
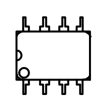
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

THROUGH−HOLE

Section 3: Flange Mount

Flange Mounted	FM	DPAK Straight Leads	CASE NO. 369 (page 73)	 SCALE 1:1	
Flange Mounted	FM	TO−220 Seven Lead	CASE NO. 821E (page 215)	 SCALE 1:1	
Flange Mounted	FM	TO−220, 7−LEAD (THA7)	CASE NO. 821H (page 216)	 SCALE 1:1	
Flange Mounted	FM	TO−220, 7−LEAD (TVA7)	CASE NO. 821J (page 216)	 SCALE 1:1	
Flange Mounted	FM	TO−220 Seven Lead	CASE NO. 821P (page 217)	 SCALE 1:1	

Section 4: Dual In−Line PIn

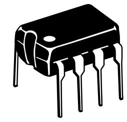
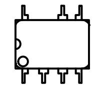
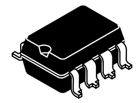
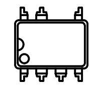
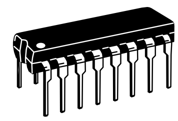
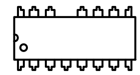
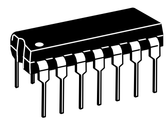
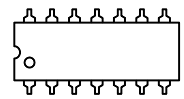
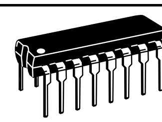
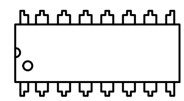
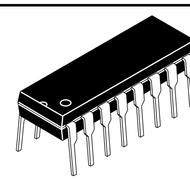
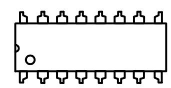
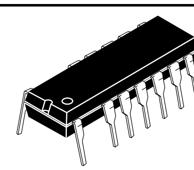
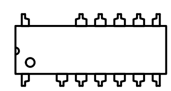
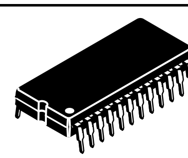
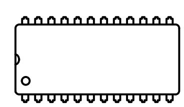
In−Line Pin	IP	DIP−8	CASE NO. 626 (page 183)	 SCALE 1:1	
In−Line Pin	IP	PDIP−8	CASE NO. 626A (page 183)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)

THROUGH−HOLE

Section 4: Dual In−Line PIn

In−Line Pin	IP	PDIP−7	CASE NO. 626B (page 184)	 SCALE 1:1	
In−Line Pin	IP	PDIP−7, GULL WING	CASE NO. 626AA (page 184)	 SCALE 1:1	
In−Line Pin	IP	PDIP−16 Less Pin 13	CASE NO. 626AB (page 185)	 SCALE 1:1	
In−Line Pin	IP	DIP−14	CASE NO. 646 (page 186)	 SCALE 1:1	
In−Line Pin	IP	DIP−16	CASE NO. 648 (page 187)	 SCALE 1:1	
In−Line Pin	IP	PDIP−16	CASE NO. 648C (page 187)	 SCALE 1:1	
In−Line Pin	IP	PDIP−16 Missing Lead	CASE NO. 648E (page 188)	 SCALE 1:1	
In−Line Pin	IP	DIP−24 Wide Body	CASE NO. 649 (page 189)	 SCALE 1:1	

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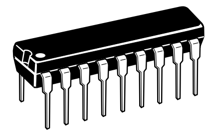
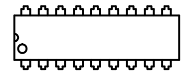
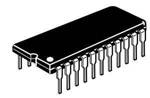
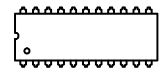
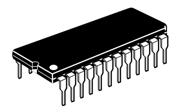
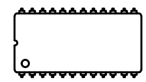
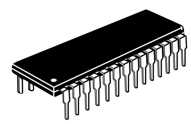
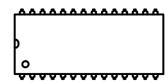
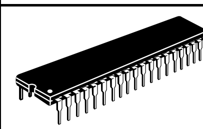
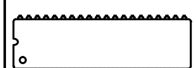
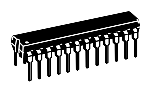
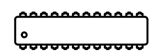
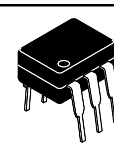
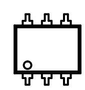
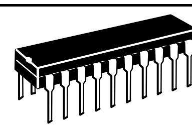
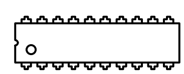
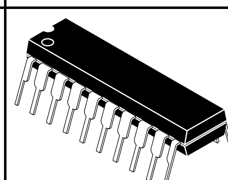
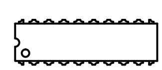
THROUGH−HOLE

Section 4: Dual In−Line PIn

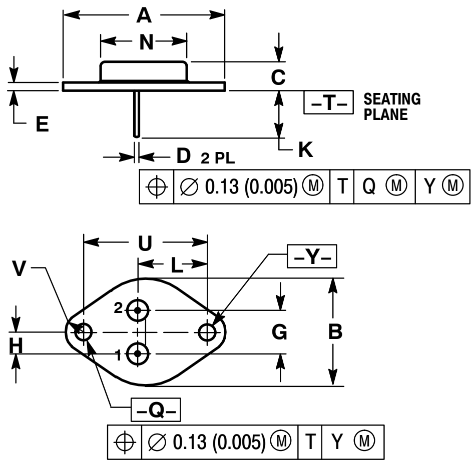
PACKAGE STYLE	JEDEC STYLE CODE	PACKAGE DESIGNATION†	ON SEMICONDUCTOR CASE OUTLINE NO.	ISOMETRIC	CASE OUTLINE (Not to Scale)
In−Line Pin	IP	DIP−18	CASE NO. 707 (page 189)	 SCALE 1:1	
In−Line Pin	IP	PDIP−22	CASE NO. 708 (page 190)	 SCALE 1:2	
In−Line Pin	IP	PDIP−24 Wide Body	CASE NO. 709 (page 190)	 SCALE 1:2	
In−Line Pin	IP	DIP−28 Wide Body	CASE NO. 710 (page 191)	 SCALE 1:2	
In−Line Pin	IP	DIP−40 Wide Body	CASE NO. 711 (page 191)	 SCALE 1:1	
In−Line Pin	IP	DIP−24	CASE NO. 724 (page 192)	 SCALE 1:2	
In−Line Pin	IP	PDIP−6	CASE NO. 730N (page 192)	 SCALE 1:1	
In−Line Pin	IP	DIP−20	CASE NO. 738 (page 193)	 SCALE 1:1	
In−Line Pin	IP	PDIP−20	CASE NO. 804 (page 215)	 SCALE 1:1	

† **Bold** indicates the ON Semiconductor package designation. Items listed in plain text represent other common package designations.

Section 2

Case Outlines

TO−3 40 MIL PINS
TO−204AA
CASE 1−07
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO−204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

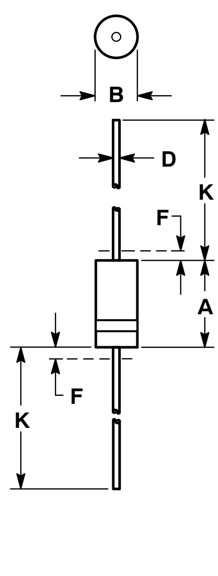
STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

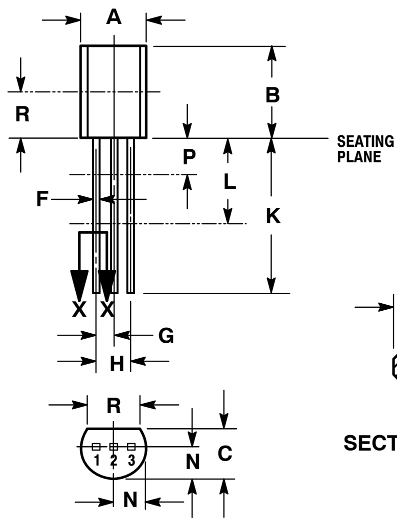
SURMETIC 40, AXIAL LEAD
CASE 017AA−01
ISSUE O

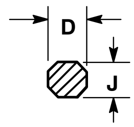


NOTES:
1. CONTROLLING DIMENSION: INCH
2. LEAD DIAMETER AND FINISH NOT CONTROLLED WITHIN DIMENSION F.
3. CATHODE BAND INDICATES POLARITY

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.330	0.350	8.38	8.89
B	0.130	0.145	3.30	3.68
D	0.037	0.043	0.94	1.09
F	---	0.050	---	1.27
K	1.000	1.250	25.40	31.75

TO−92 1−WATT
TO−226AE
CASE 29−10
ISSUE AL





SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MIMIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.457	0.533
F	0.016	0.019	0.407	0.482
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

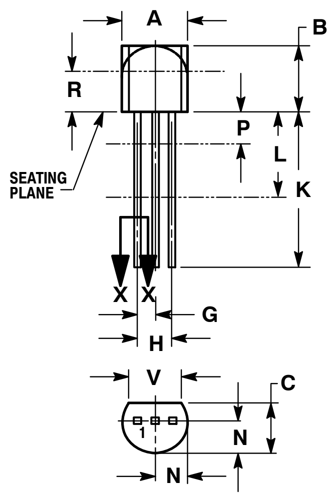
STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

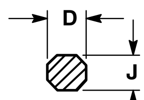
STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

TO−92 (TO−226AA)
CASE 29−11
ISSUE AM



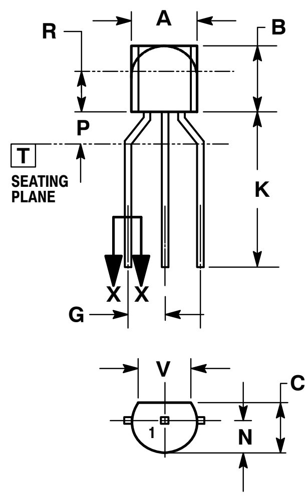
STRAIGHT LEAD
BULK PACK



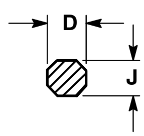
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS	
DIM	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

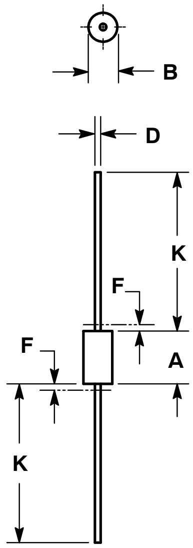
STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

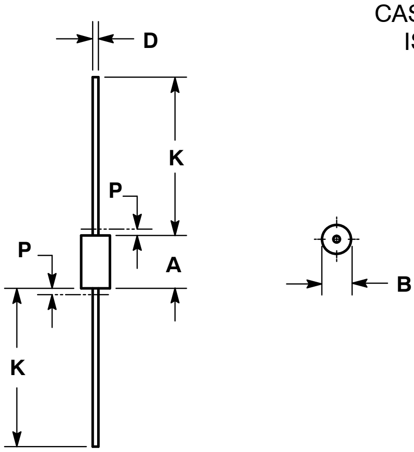
MOSORB
CASE 41−13
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD FINISH AND DIAMETER UNCONTROLLED IN DIMENSION F.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.360	0.375	9.14	9.52
B	0.190	0.205	4.83	5.21
D	0.028	0.032	0.71	0.81
F	---	0.050	---	1.27
K	1.000	---	25.40	---

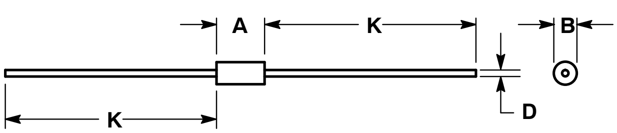
MOSORB
CASE 41A−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD FINISH AND DIAMETER UNCONTROLLED IN DIMENSION P.
4. 041A−01 THRU 041A−03 OBSOLETE, NEW STANDARD 041A−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.335	0.374	8.50	9.50
B	0.189	0.209	4.80	5.30
D	0.038	0.042	0.96	1.06
K	1.000	---	25.40	---
P	---	0.050	---	1.27

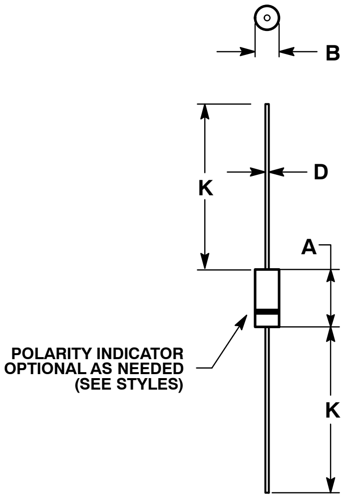
DO−41
CASE 59A−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.260	5.97	6.60
B	0.110	0.120	2.79	3.05
D	0.030	0.034	0.76	0.86
K	1.100	---	27.94	---

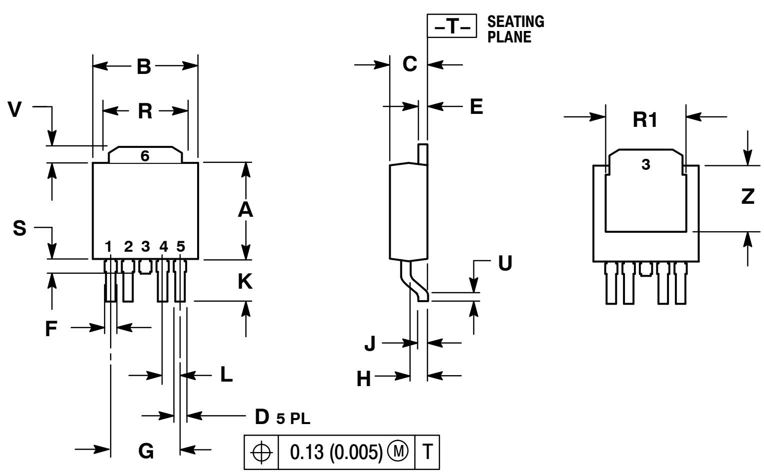
AXIAL LEAD
CASE 59AA−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO−41 OUTLINE SHALL APPLY.
4. POLARITY DENOTED BY CATHODE BAND.
5. LEAD DIAMETER NOT CONTROLLED WITHIN F DIMENSION.
6. REPLACES CASE 59−09.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.228	0.299	5.80	7.60
B	0.102	0.142	2.60	3.60
D	0.028	0.034	0.71	0.86
K	1.000	−−−	25.44	−−−

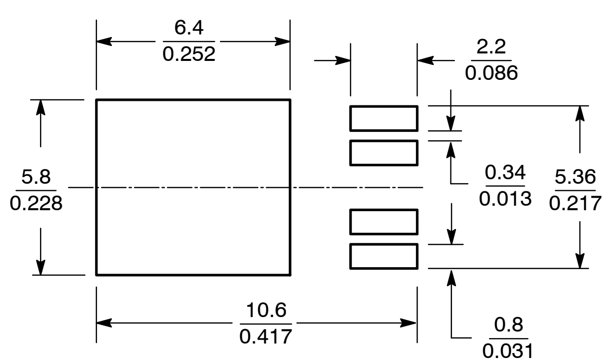
DPAK 5 CENTER LEAD CROP
CASE 175AA−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

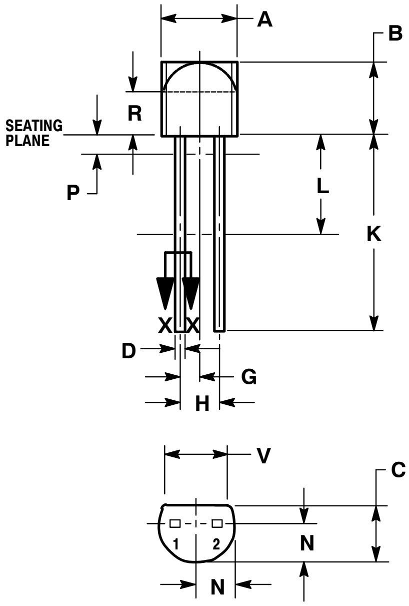
SOLDERING FOOTPRINT

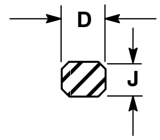


SCALE 4:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

TO−92 TWO LEAD

TO−226AC
CASE 182−06
ISSUE L





SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND ZONE R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.21
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.050 BSC		1.27 BSC	
H	0.100 BSC		2.54 BSC	
J	0.014	0.016	0.36	0.41
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.03	2.66
P	---	0.050	---	1.27
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 1:
PIN 1. ANODE
2. CATHODE

STYLE 2:
PIN 1. CATHODE
2. ANODE

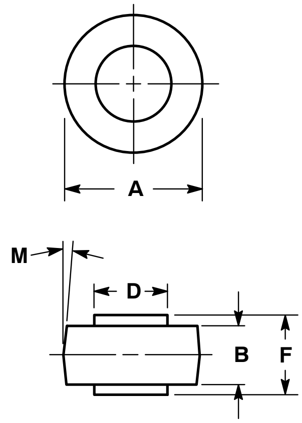
STYLE 3:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2

STYLE 4:
CANCELLED

STYLE 5:
PIN 1. INPUT
2. OUTPUT

MICRODE BUTTON

CASE 193−04
ISSUE L

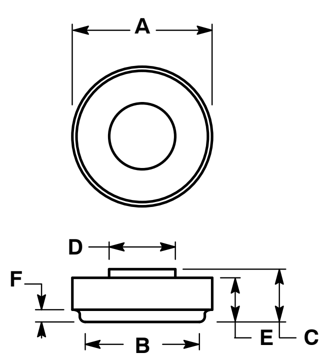


NOTES:
1. CASE 193−03 OBSOLETE, NEW STANDARD 193−04.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.43	8.69	0.332	0.342
B	4.19	4.45	0.165	0.175
D	5.54	5.64	0.218	0.222
F	5.94	6.25	0.234	0.246
M	5 °NOM		5 °NOM	

BUTTON CAN

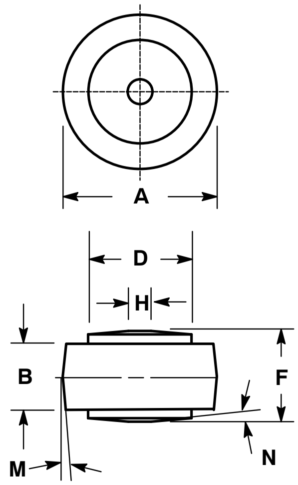
CASE 193A−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.4	11.6	0.449	0.457
B	9.3	9.7	0.366	0.382
C	4.3	4.9	0.169	0.193
D	5.4	5.6	0.213	0.220
E	3.6	4.2	0.142	0.165
F	1.0	2.0	0.039	0.079

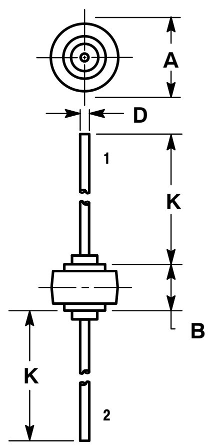
JUMBO CAN
CASE 193AA−01
ISSUE O



NOTES:
1. CASE 193−05 AND 193−07 OBSOLETE, NEW STANDARD 193−06.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.03	10.29	0.395	0.405
B	4.19	4.45	0.165	0.175
D	6.81	6.91	0.268	0.272
F	5.94	6.25	0.234	0.246
H	1.40	1.65	0.055	0.065
M	5 °NOM		5 °NOM	
N	6 °NOM		6 °NOM	

AXIAL LEAD BUTTON
CASE 194−04
ISSUE H



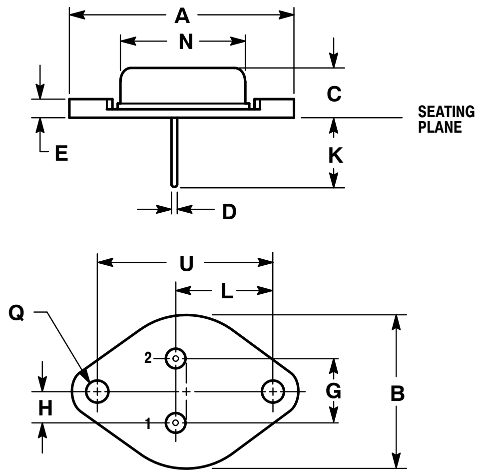
NOTES:
1. CATHODE SYMBOL ON PACKAGE.
2. 194−01 OBSOLETE, 194−04 NEW STANDARD.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.43	8.69	0.332	0.342
B	5.94	6.25	0.234	0.246
D	1.27	1.35	0.050	0.053
K	25.15	25.65	0.990	1.010

STYLE 1:
PIN 1. CATHODE
2. ANODE

TO−3

TO−204
CASE 197−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	1.573	---	39.95
B	0.980	1.050	24.89	26.67
C	0.250	0.450	6.35	11.43
D	0.057	0.063	1.45	1.60
E	---	0.135	---	3.43
G	0.420	0.440	10.67	11.18
H	0.205	0.225	5.21	5.72
K	0.440	0.480	11.18	12.19
L	0.655	0.675	16.64	17.15
N	---	0.875	---	22.23
Q	0.151	0.165	3.84	4.19
U	1.177	1.197	29.90	30.40

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

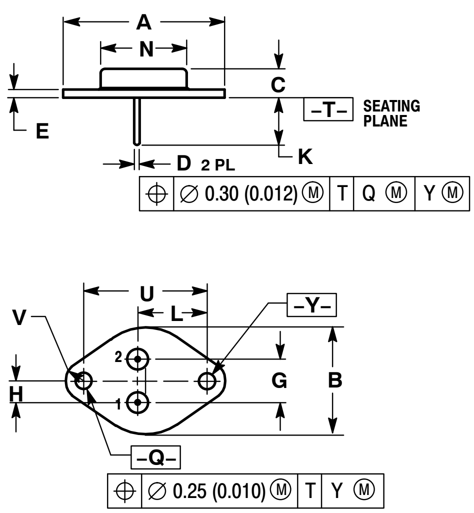
STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. ANODE = 1
2. ANODE = 2
CASE: CATHODES

TO−3

TO−204
CASE 197A−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

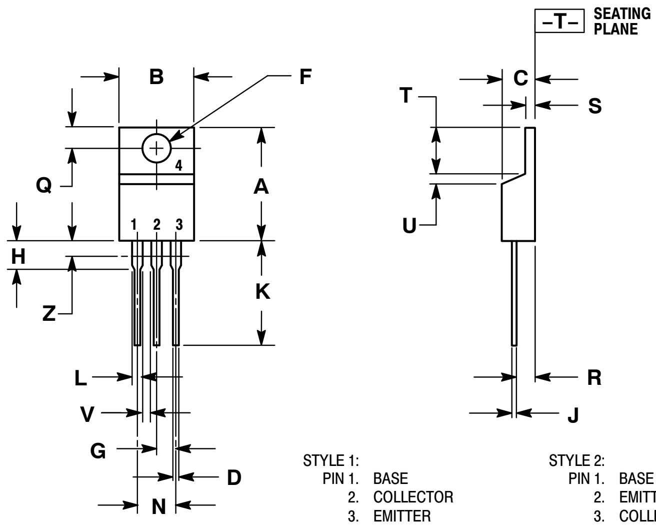
STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. EMITTER
2. BASE
CASE: COLLECTOR

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. ANODE = 1
2. ANODE = 2
CASE: CATHODES

TO−220
CASE 221A−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

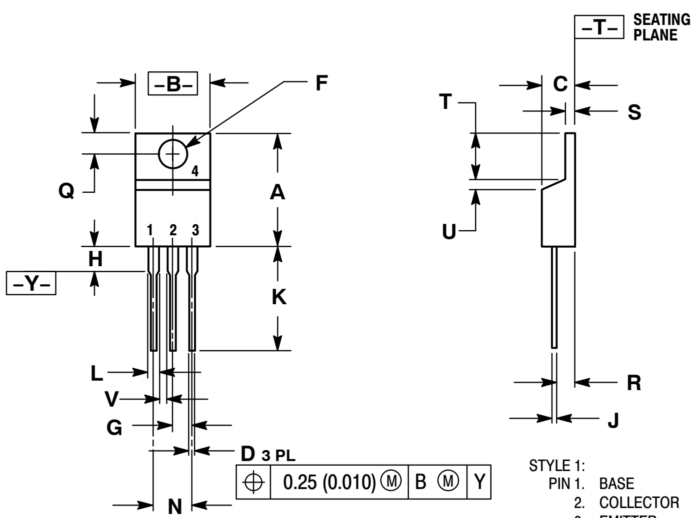
STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

TO−220
CASE 221A−08
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.025	0.035	0.64	0.89
F	0.139	0.155	3.53	3.93
G	0.100 BSC		2.54 BSC	
H	---	0.280	---	7.11
J	0.012	0.045	0.31	1.14
K	0.500	0.580	12.70	14.73
L	0.045	0.060	1.15	1.52
N	0.200 BSC		5.08 BSC	
Q	0.100	0.135	2.54	3.42
R	0.080	0.115	2.04	2.92
S	0.020	0.055	0.51	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

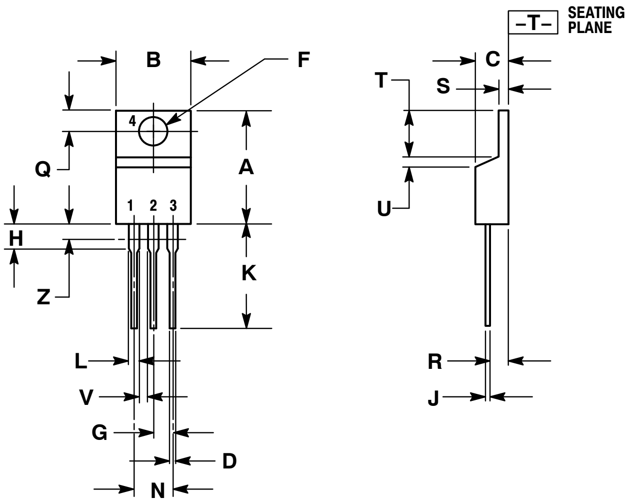
STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

TO−220
CASE 221A−09
ISSUE AF



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

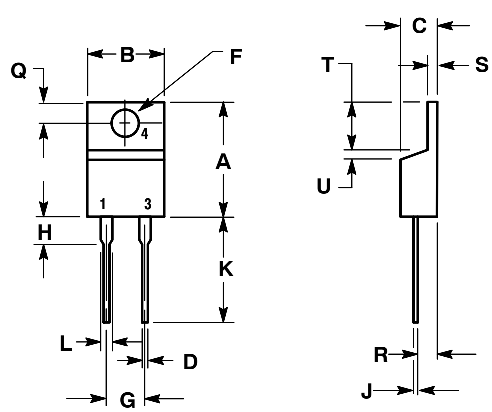
STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

TO−220 TWO−LEAD
CASE 221B−04
ISSUE E



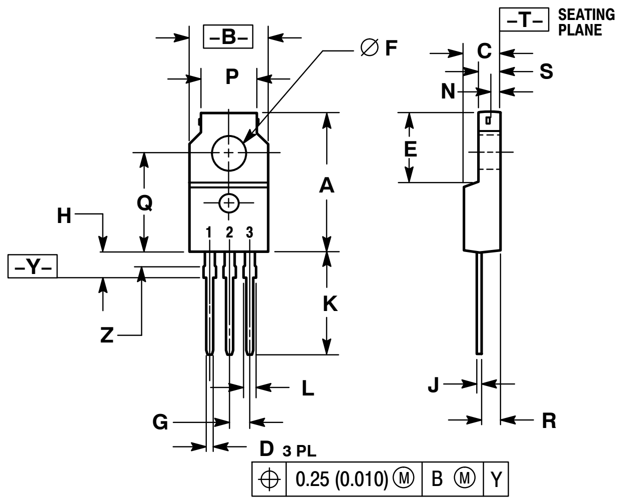
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.595	0.620	15.11	15.75
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.82
D	0.025	0.035	0.64	0.89
F	0.142	0.161	3.61	4.09
G	0.190	0.210	4.83	5.33
H	0.110	0.130	2.79	3.30
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.14	1.39
T	0.235	0.255	5.97	6.48
U	0.000	0.050	0.000	1.27

STYLE 1:
PIN 1. CATHODE
2. N/A
3. ANODE
4. CATHODE

STYLE 2:
PIN 1. ANODE
2. N/A
3. CATHODE
4. ANODE

TO−220 FULLPACK THYRISTOR
CASE 221C−02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. LEAD DIMENSIONS UNCONTROLLED WITHIN DIMENSION Z.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.680	0.700	17.28	17.78
B	0.388	0.408	9.86	10.36
C	0.175	0.195	4.45	4.95
D	0.025	0.040	0.64	1.01
E	0.340	0.355	8.64	9.01
F	0.140	0.150	3.56	3.81
G	0.100 BSC		2.54 BSC	
H	0.110	0.155	2.80	3.93
J	0.018	0.028	0.46	0.71
K	0.500	0.550	12.70	13.97
L	0.045	0.070	1.15	1.77
N	0.049	---	1.25	---
P	0.270	0.290	6.86	7.36
Q	0.480	0.500	12.20	12.70
R	0.090	0.120	2.29	3.04
S	0.105	0.115	2.67	2.92
Z	0.070	0.090	1.78	2.28

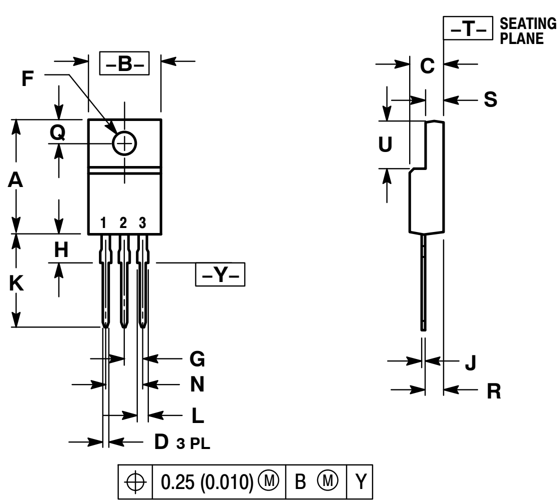
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 3:
PIN 1. MT 1
2. MT 2
3. GATE

STYLE 4:
PIN 1. GATE
2. DRAIN
3. SOURCE

TO−220 FULLPACK TRANSISTOR
CASE 221D−03
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

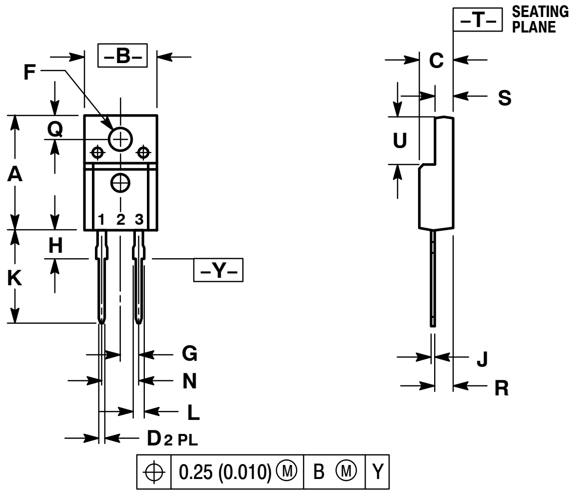
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. CATHODE

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 6:
PIN 1. MT 1
2. MT 2
3. GATE

TO−220 FULLPACK, 2−LEAD
CASE 221E−01
ISSUE A

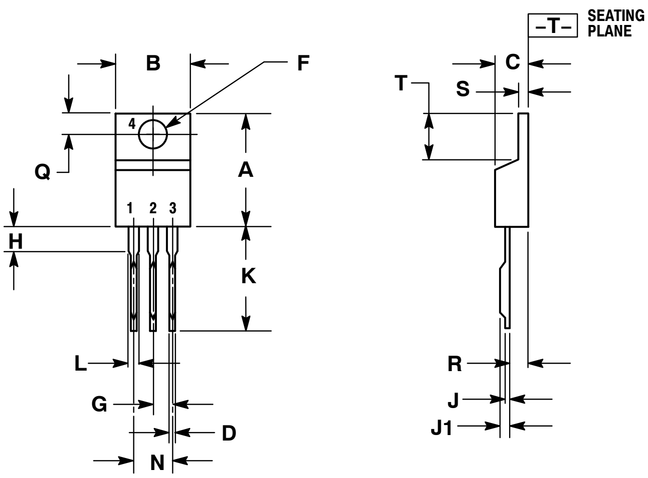


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.633	15.67	16.07
B	0.392	0.408	9.96	10.36
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.121	0.129	3.08	3.28
G	0.100 BSC		2.54 BSC	
H	0.117	0.133	2.98	3.38
J	0.018	0.025	0.45	0.64
K	0.499	0.562	12.68	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.101	0.117	2.56	2.96
S	0.092	0.108	2.34	2.74
U	0.255	0.271	6.48	6.88

STYLE 1:
PIN 1. CATHODE
2. N/A
3. ANODE

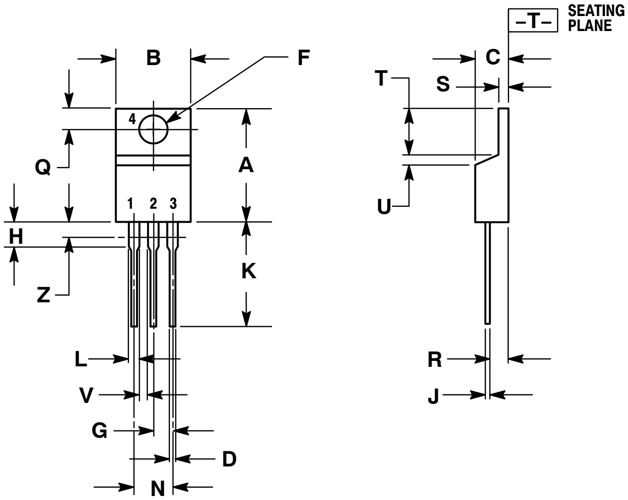
TO−220AB
CASE 221K−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 INCH PER SIDE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.650	14.22	16.51
B	0.380	0.420	9.65	10.67
C	0.140	0.190	3.56	4.83
D	0.015	0.040	0.38	1.02
F	0.139	0.161	3.53	4.09
G	0.100 BSC		2.54 BSC	
H	---	0.250	---	6.35
J	0.014	0.024	0.36	0.61
J1	0.018	0.026	0.46	0.66
K	0.500	0.580	12.70	14.73
L	0.045	0.070	1.14	1.78
N	0.200 BSC		5.08 BSC	
Q	0.100	0.135	2.54	3.43
R	0.080	0.115	2.03	2.92
S	0.020	0.055	0.51	1.40
T	0.230	0.270	5.84	6.86

TO−220, SINGLE GAUGE
CASE 221AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.055	0.508	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

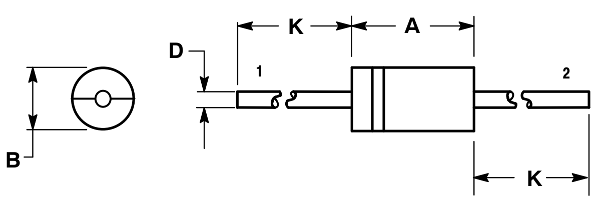
STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

3A SURMETIC
CASE 267−03
ISSUE G



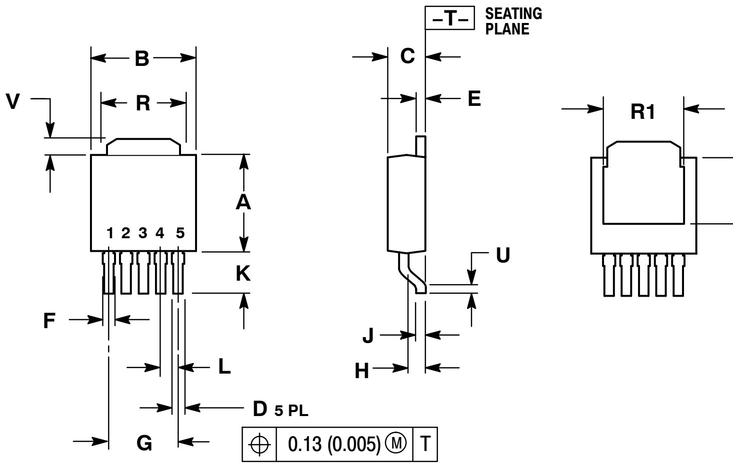
NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 267−01 AND 267−02 OBSOLETE, NEW STANDARD 267−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.370	0.380	9.40	9.65
B	0.190	0.210	4.83	5.33
D	0.048	0.052	1.22	1.32
K	1.000	---	25.40	---

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

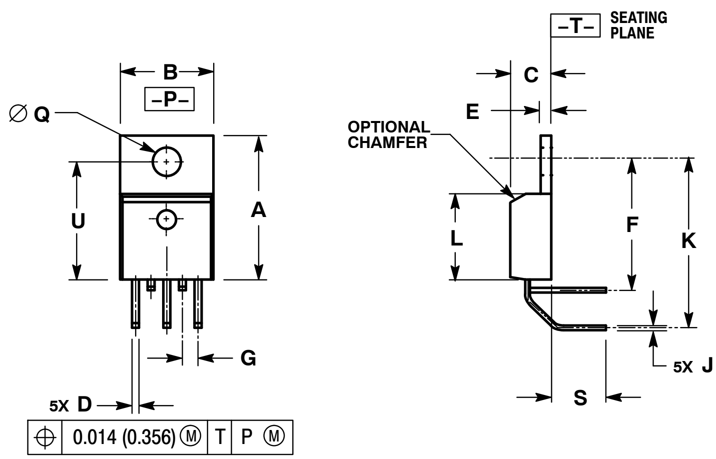
DPAK−5
CASE 271AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.50	0.70
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

5−LEAD TO−220 (THA5)
CASE 314A−03
ISSUE E

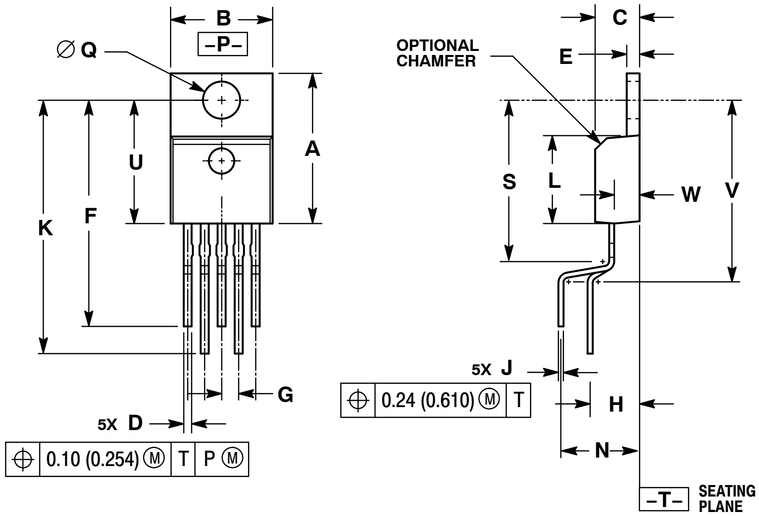


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
U	0.468	0.505	11.888	12.827

5−LEAD TO−220 (OFFSET LEADS)

CASE 314B−05
ISSUE L



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

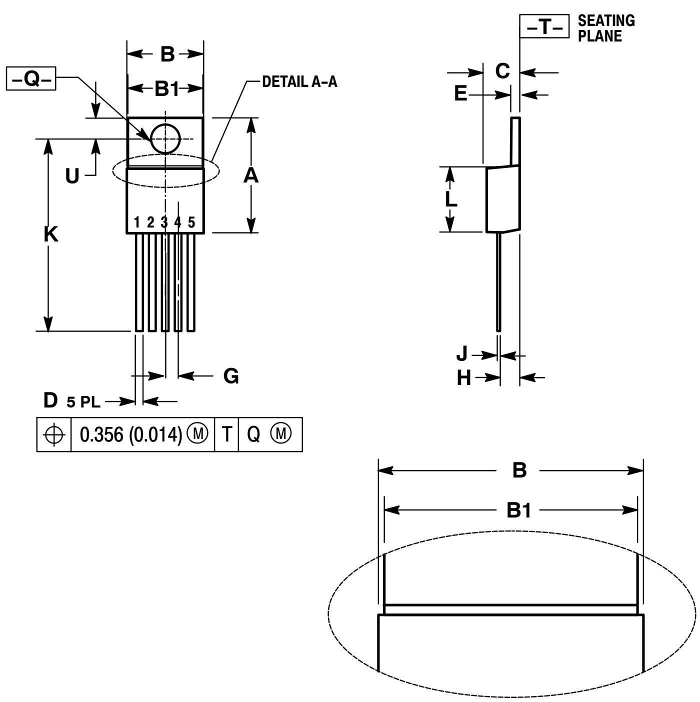
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	---	0.620	---	15.748
U	0.468	0.505	11.888	12.827
V	---	0.735	---	18.669
W	0.090	0.110	2.286	2.794

STYLE 1 THRU 4:
CANCELLED

STYLE 5:
PIN 1. GATE
2. MIRROR
3. DRAIN
4. KELVIN
5. SOURCE

TO−220 FIVE−LEAD

CASE 314D−04
ISSUE F

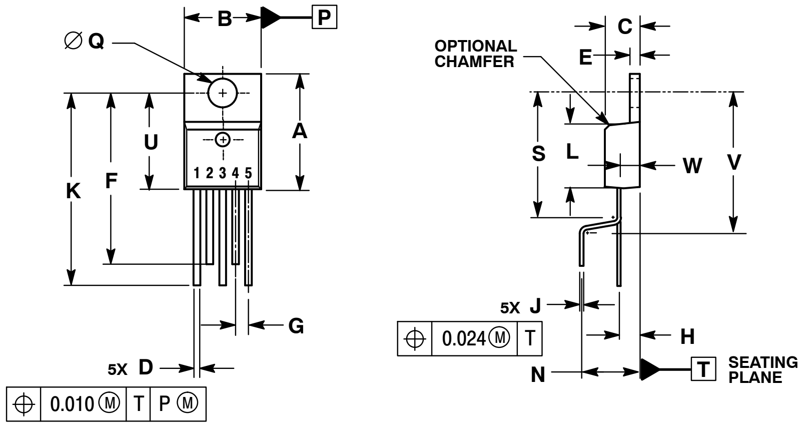


DETAIL A−A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
B1	0.375	0.415	9.525	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.977	1.045	24.810	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

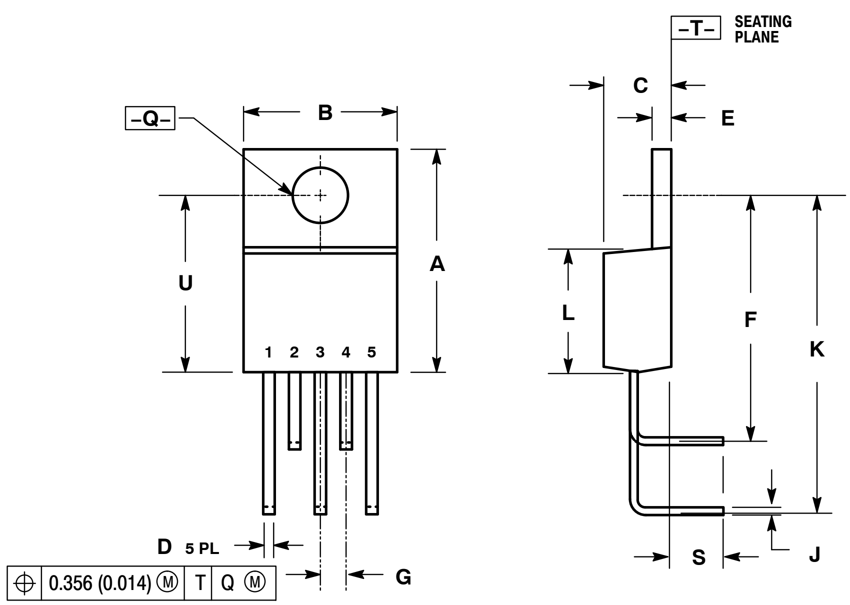
TO−220, 5−LEAD (VHVIC)
CASE 314E−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.005 TOTAL IN EXCESS OF THE “D” DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. 314E−01 THRU −02 OBSOLETE, NEW STANDARD IS 314E−03.

	INCHES	
DIM	MIN	MAX
A	0.572	0.613
B	0.390	0.415
C	0.165	0.187
D	0.025	0.038
E	0.045	0.055
F	0.890	0.930
G	0.067 BSC	
H	0.105 BSC	
J	0.015	0.025
K	0.900	1.045
L	0.320	0.365
N	0.259 BSC	
Q	0.140	0.156
S	---	0.620
U	0.468	0.505
V	---	0.718
W	0.090	0.100

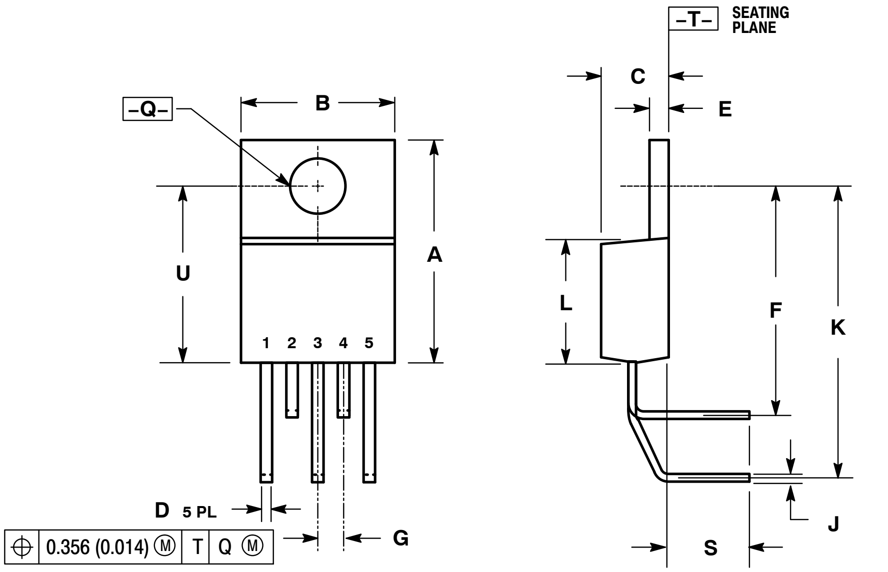
TO−220, 5−LEAD (THB5)
CASE 314F−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. FORMED LEADS ARE PERPENDICULAR TO THE PLANE OF THE HEAT SINK TAB. LEAD TIPS MUST BE WITHIN 0.015 OF NOMINAL POSITION.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.568	0.583	14.43	14.81
B	0.390	0.410	9.91	10.41
C	0.170	0.180	4.32	4.57
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.653	0.668	16.59	16.97
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.803	0.818	20.40	20.78
L	0.322	0.337	8.18	8.56
Q	0.146	0.156	3.71	3.96
S	0.097	0.147	2.46	3.73
U	0.460	0.475	11.68	12.07

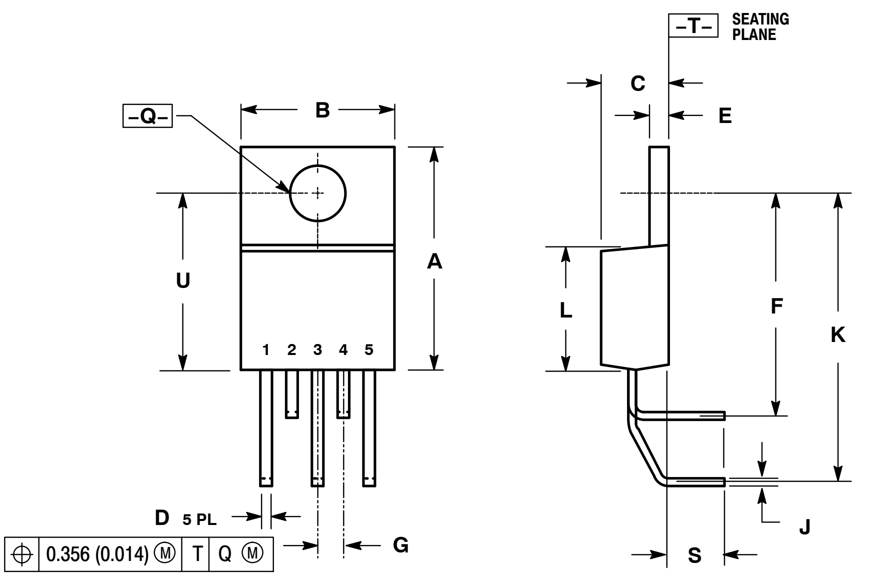
TO−220, 5−LEAD (THC5)
CASE 314G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITHIN ± 15 MILS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.568	0.583	14.43	14.81
B	0.390	0.410	9.91	10.41
C	0.170	0.180	4.32	4.57
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.593	0.608	15.06	15.44
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.753	0.768	19.13	19.51
L	0.322	0.337	8.18	8.56
Q	0.146	0.156	3.71	3.96
S	0.220	0.270	5.59	6.86
U	0.460	0.475	11.68	12.07

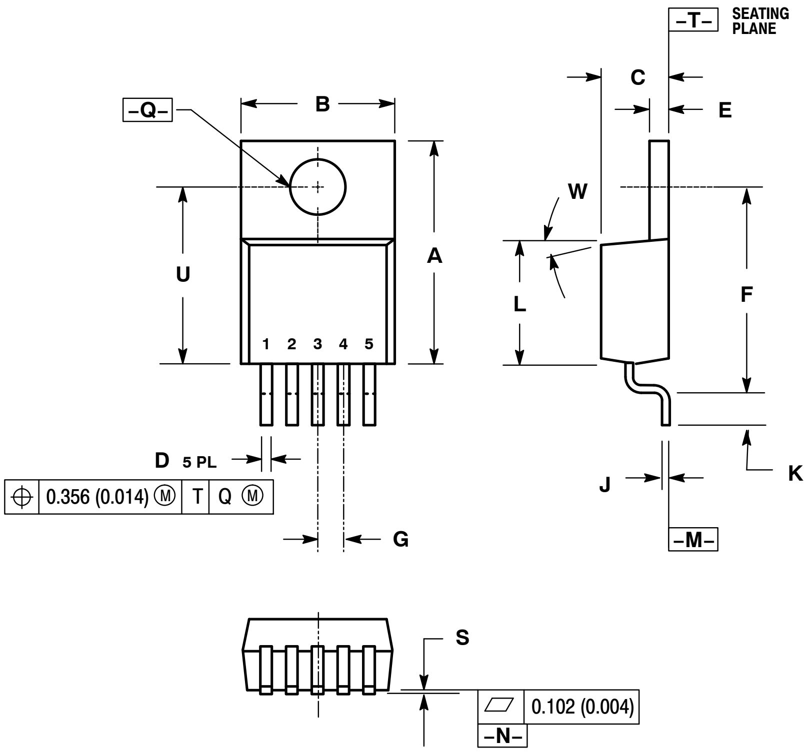
TO−220, 5−LEAD (THD5)
CASE 314H−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITHIN ± 15 MILS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.568	0.583	14.43	14.81
B	0.390	0.410	9.91	10.41
C	0.170	0.180	4.32	4.57
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.593	0.608	15.06	15.44
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.753	0.768	19.13	19.51
L	0.322	0.337	8.18	8.56
Q	0.146	0.156	3.71	3.96
S	0.220	0.270	5.59	6.86
U	0.460	0.475	11.68	12.07

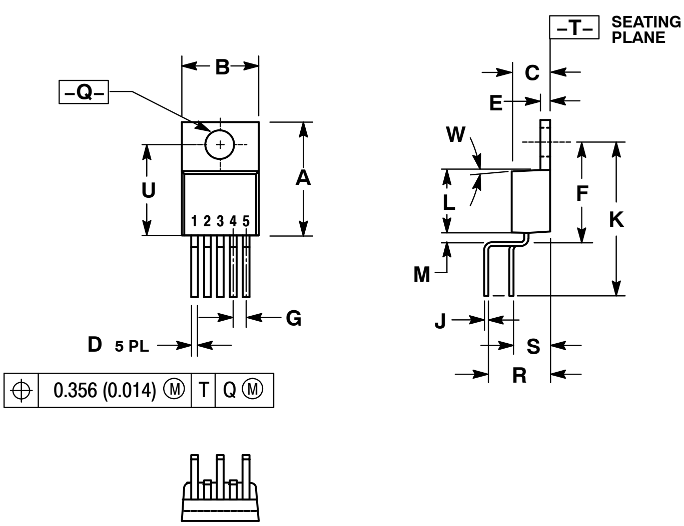
TO−220, 5−LEAD (THE5)
CASE 314J−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. DIMENSIONS EXCLUSIVE OF MOLD FLASH AND METAL BURRS.
5. FOOTPAD LENGTH MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM −M−.
6. COPLANARITY 0.004” MAX. REFERENCE TO DATUM −N− STANDOFF HEIGHT 0.00 − 0.010”.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.568	0.583	14.43	14.81
B	0.395	0.405	10.03	10.29
C	0.170	0.180	4.32	4.57
D	0.028	0.036	0.71	0.91
E	0.045	0.055	1.14	1.40
F	0.543	0.558	13.79	14.17
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.073	0.088	1.85	2.24
L	0.324	0.339	8.23	8.61
Q	0.146	0.156	3.71	3.96
S	0.000	0.010	0.00	0.25
U	0.460	0.475	11.68	12.07
W	5 °		5 °	

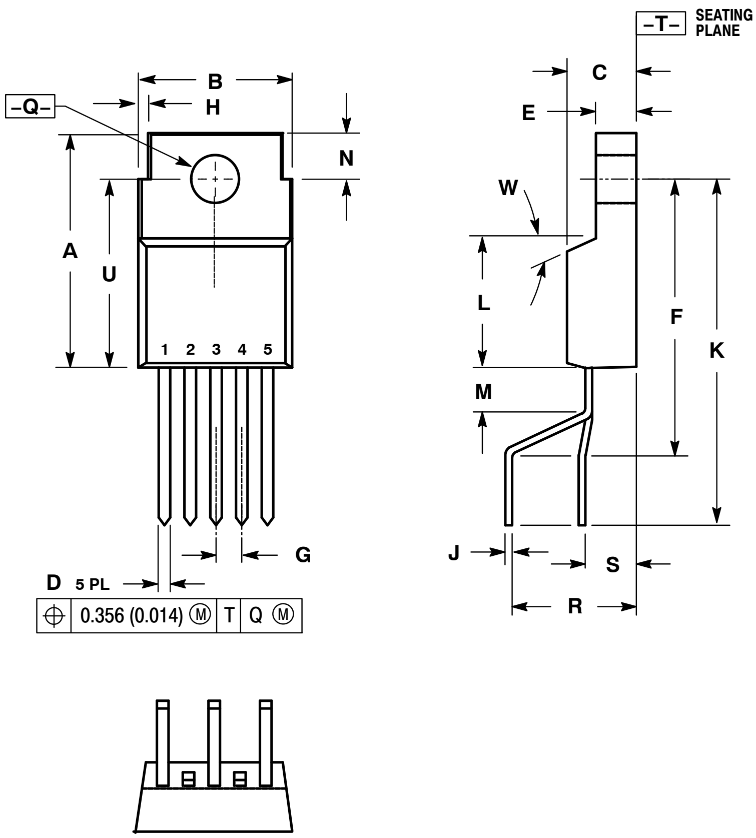
TO−220, 5−LEAD (TVA5)
CASE 314K−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D, INCLUDING PROTRUSION, SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.78	10.54
C	0.160	0.190	4.06	4.83
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.530	0.545	13.46	13.84
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.321	0.337	8.15	8.56
M	0.063	0.078	1.60	1.98
Q	0.146	0.156	3.71	3.96
R	0.271	0.321	6.88	8.15
S	0.146	0.196	3.71	4.98
U	0.460	0.475	11.68	12.07
W	5 °		5 °	

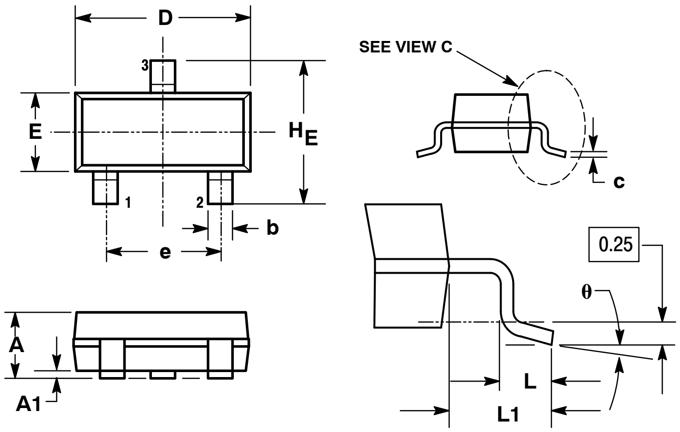
TO−220, 5−LEAD (TFVA5)
CASE 314N−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
4. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITHIN ± 0.015 ".

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.604	0.614	15.34	15.60
B	0.395	0.405	10.03	10.29
C	0.175	0.185	4.44	4.70
D	0.027	0.037	0.69	0.94
E	0.100	0.110	2.54	2.79
F	0.712	0.727	18.08	18.47
G	0.067 BSC		1.70 BSC	
H	0.020	0.030	0.51	0.76
J	0.014	0.022	0.36	0.56
K	0.889	0.904	22.58	22.96
L	0.324	0.339	8.23	8.61
M	0.115	0.130	2.92	3.30
N	0.115	0.125	2.92	3.17
Q	0.120	0.130	3.05	3.30
R	0.292	0.342	7.42	8.69
S	0.133	0.183	3.38	4.65
U	0.480	0.495	12.19	12.57
W	5 °		5 °	

SOT−23
TO−236AB
CASE 318−08
ISSUE AN



VIEW C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

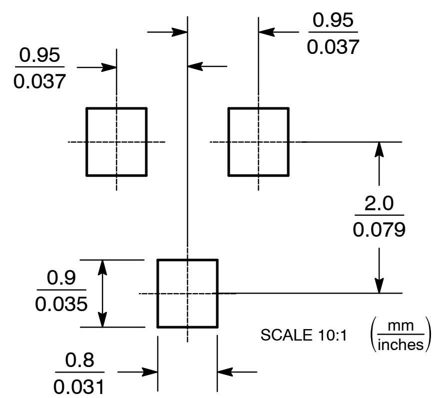
STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

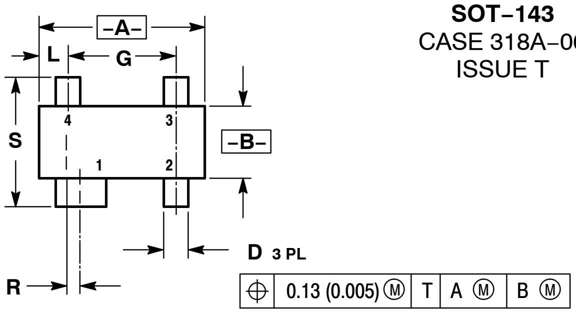
STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

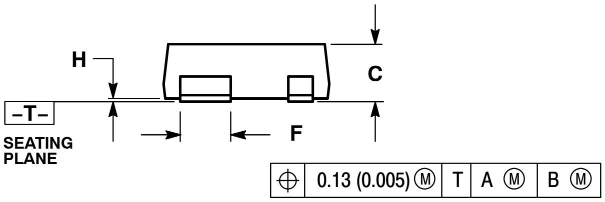
STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

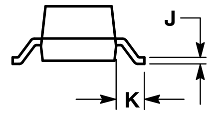
SOLDERING FOOTPRINT



SOT−143
CASE 318A−06
ISSUE T







NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS ARE INCLUSIVE OF PLATING.
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
5. 318A−01 THRU −05 OBSOLETE, NEW STANDARD 318A−06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.800	3.040	0.110	0.120
B	1.200	1.400	0.047	0.055
C	0.890	1.120	0.035	0.044
D	0.370	0.510	0.015	0.020
F	0.760	0.940	0.030	0.037
G	1.920 BSC		0.076 BSC	
H	0.013	0.100	0.001	0.004
J	0.085	0.180	0.003	0.007
K	0.55 REF		0.022 REF	
L	0.525 BSC		0.021 BSC	
R	0.200 BSC		0.008 BSC	
S	2.100	2.640	0.083	0.0104

STYLE 1:
PIN 1. COLLECTOR
2. EMITTER
3. EMITTER
4. BASE

STYLE 2:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. GATE 2

STYLE 3:
PIN 1. GROUND
2. SOURCE
3. INPUT
4. OUTPUT

STYLE 4:
PIN 1. OUTPUT
2. GROUND
3. GROUND
4. INPUT

STYLE 5:
PIN 1. SOURCE
2. DRAIN
3. GATE 1
4. SOURCE

STYLE 6:
PIN 1. GND
2. RF IN
3. VREG
4. RF OUT

STYLE 7:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE

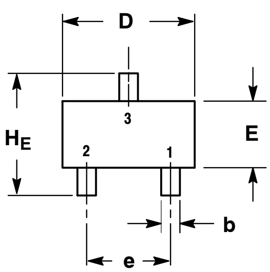
STYLE 8:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. N/C

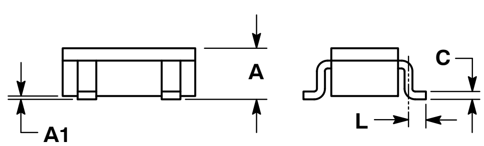
STYLE 9:
PIN 1. GND
2. IOUT
3. VCC
4. VREF

STYLE 10:
PIN 1. DRAIN
2. N/C
3. SOURCE
4. GATE

STYLE 11:
PIN 1. SOURCE
2. GATE 1
3. GATE 2
4. DRAIN

SC−59
CASE 318D−04
ISSUE G





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.15	1.30	0.039	0.045	0.051
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.35	0.43	0.50	0.014	0.017	0.020
c	0.09	0.14	0.18	0.003	0.005	0.007
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	1.70	1.90	2.10	0.067	0.075	0.083
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.80	3.00	0.099	0.110	0.118

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. N.C.
2. ANODE
3. CATHODE

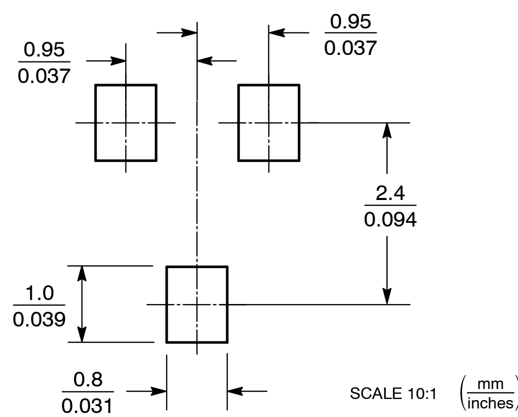
STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. N.C.
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE

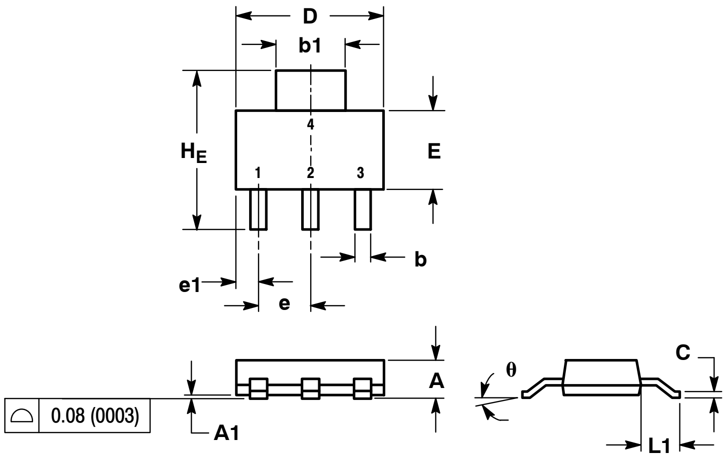
STYLE 6:
PIN 1. CATHODE
2. ANODE
3. ANODE/CATHODE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOT−223
CASE 318E−04
ISSUE M



NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

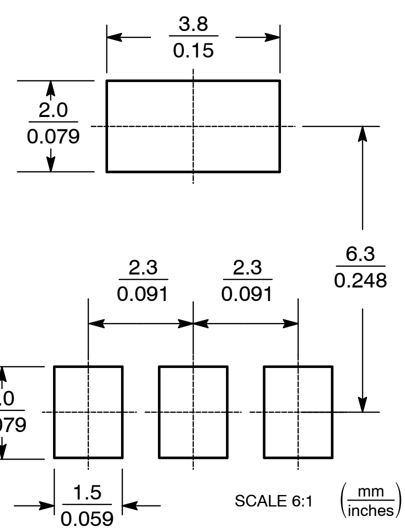
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

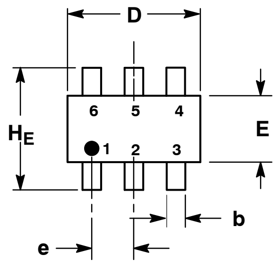
STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

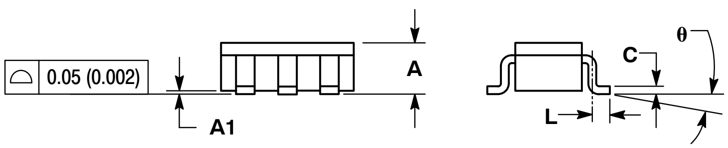
STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT



SC−74
CASE 318F−05
ISSUE M





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

STYLE 1:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 2:
PIN 1. NO CONNECTION
2. COLLECTOR
3. EMITTER
4. NO CONNECTION
5. COLLECTOR
6. BASE

STYLE 3:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 4:
PIN 1. COLLECTOR 2
2. EMITTER 1/EMITTER 2
3. COLLECTOR 1
4. EMITTER 3
5. BASE 1/BASE 2/COLLECTOR 3
6. BASE 3

STYLE 5:
PIN 1. CHANNEL 1
2. ANODE
3. CHANNEL 2
4. CHANNEL 3
5. CATHODE
6. CHANNEL 4

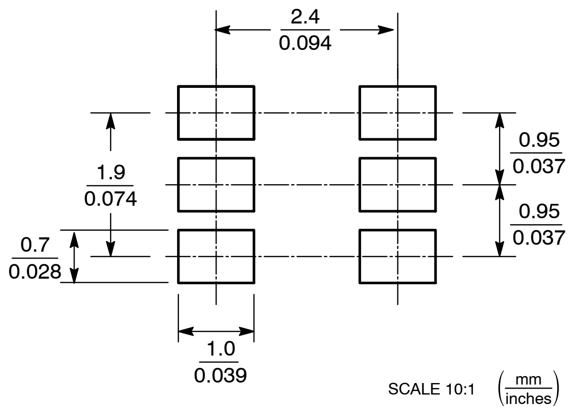
STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 8:
PIN 1. EMITTER 1
2. BASE 2
3. COLLECTOR 2
4. EMITTER 2
5. BASE 1
6. COLLECTOR 1

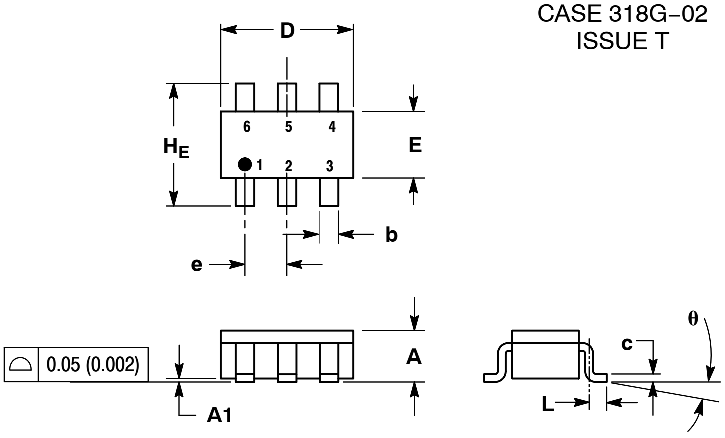
STYLE 9:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TSOP−6
SOT23−6, SC59−6
CASE 318G−02
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

STYLE 1:
PIN 7. DRAIN
8. DRAIN
9. GATE
10. SOURCE
11. DRAIN
12. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

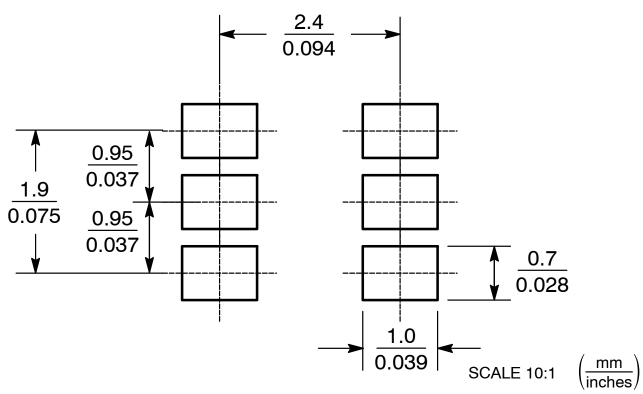
STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

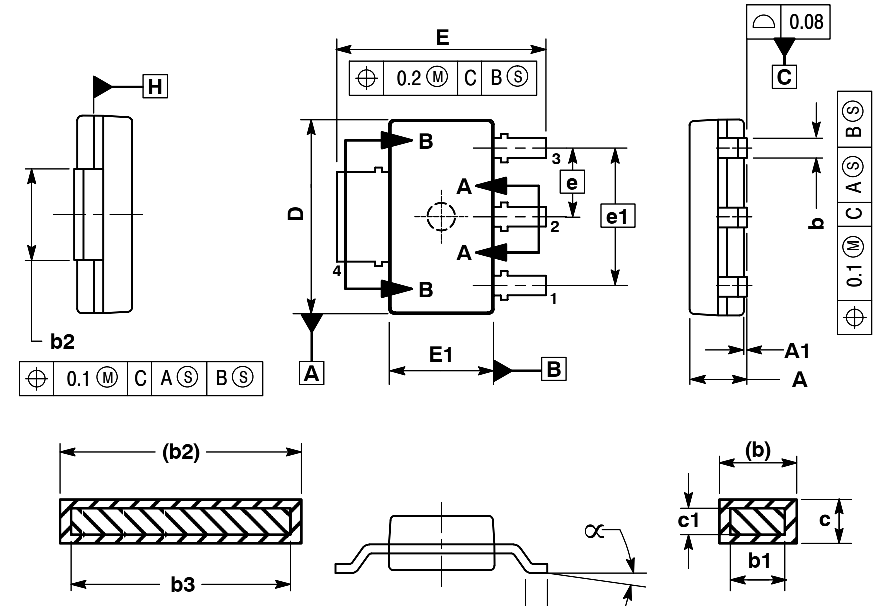
STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOT−223
CASE 318H−01
ISSUE O



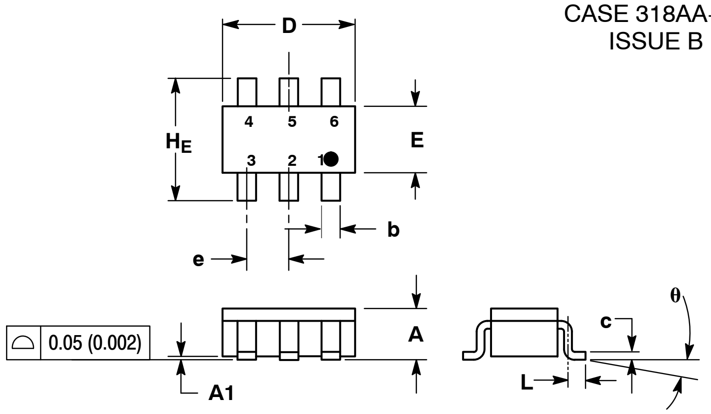
SECTION B−B

SECTION A−A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.23 PER SIDE.
4. DIMENSIONS b AND b2 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE b AND b2 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.80
A1	0.02	0.11
b	0.60	0.88
b1	0.60	0.80
b2	2.90	3.10
b3	2.90	3.05
c	0.24	0.35
c1	0.24	0.30
D	6.30	6.70
E	6.70	7.30
E1	3.30	3.70
e	2.30	
e1	4.60	
L	0.25	---
∝	0°	10°

SC−74R
CASE 318AA−01
ISSUE B



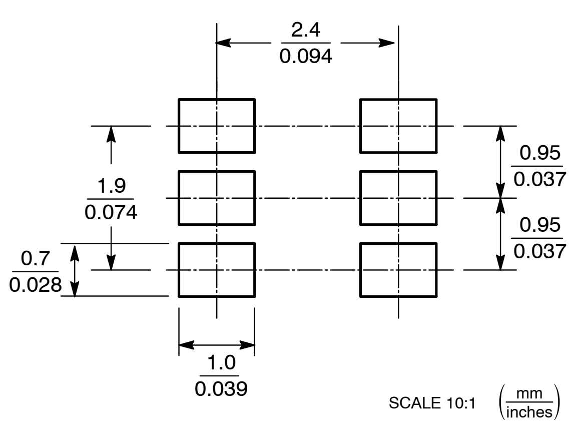
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	–	10°	0°	–	10°

STYLE 20:
PIN 1. COLLECTOR 1
2. BASE 2
3. EMITTER 2
4. COLLECTOR 2
5. BASE 1
6. EMITTER 1

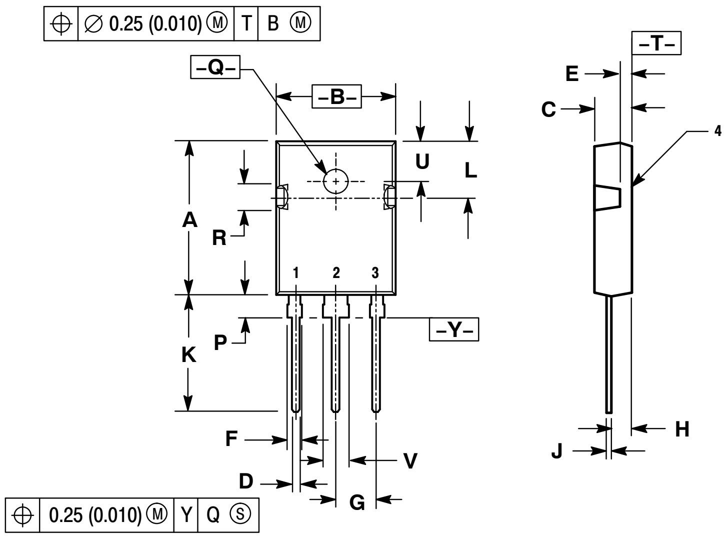
STYLE 21:
PIN 1. COLLECTOR 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. EMITTER 1
6. BASE 1

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TO−247
CASE 340F−03
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

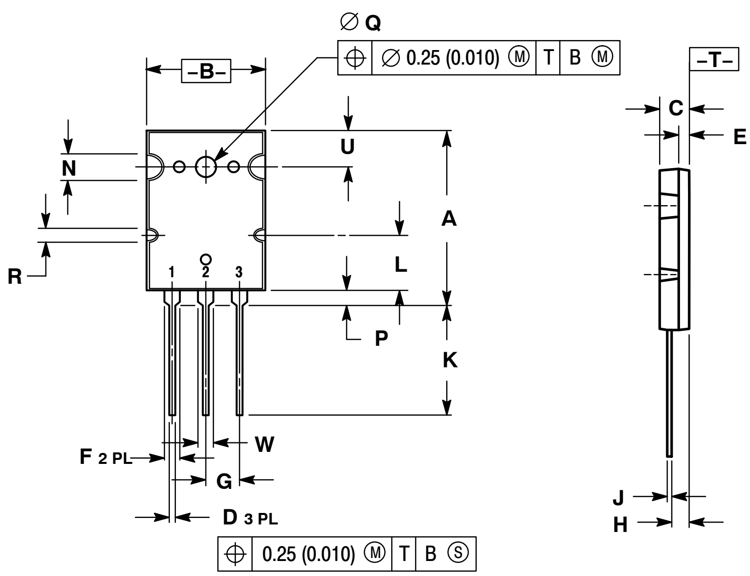
STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE 1
2. CATHODE (S)
3. ANODE 2
4. CATHODE (S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

TO−264
TO−3PBL
CASE 340G−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.2 REF		0.411 REF	
N	4.35 REF		0.172 REF	
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.25 REF		0.089 REF	
U	6.3 REF		0.248 REF	
W	2.8	3.2	0.110	0.125

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

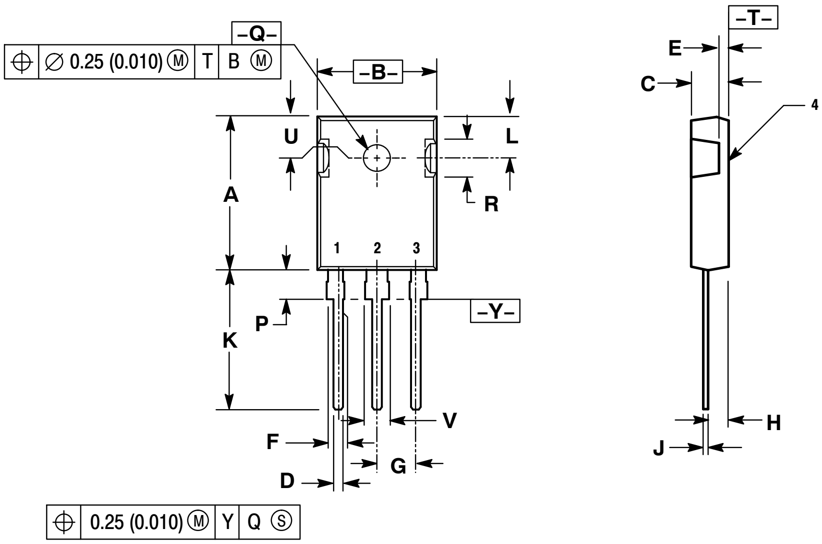
STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

TO−247
CASE 340K−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.7	20.3	0.776	0.799
B	15.3	15.9	0.602	0.626
C	4.7	5.3	0.185	0.209
D	1.0	1.4	0.039	0.055
E	1.27 REF		0.050 REF	
F	2.0	2.4	0.079	0.094
G	5.5 BSC		0.216 BSC	
H	2.2	2.6	0.087	0.102
J	0.4	0.8	0.016	0.031
K	14.2	14.8	0.559	0.583
L	5.5 NOM		0.217 NOM	
P	3.7	4.3	0.146	0.169
Q	3.55	3.65	0.140	0.144
R	5.0 NOM		0.197 NOM	
U	5.5 BSC		0.217 BSC	
V	3.0	3.4	0.118	0.134

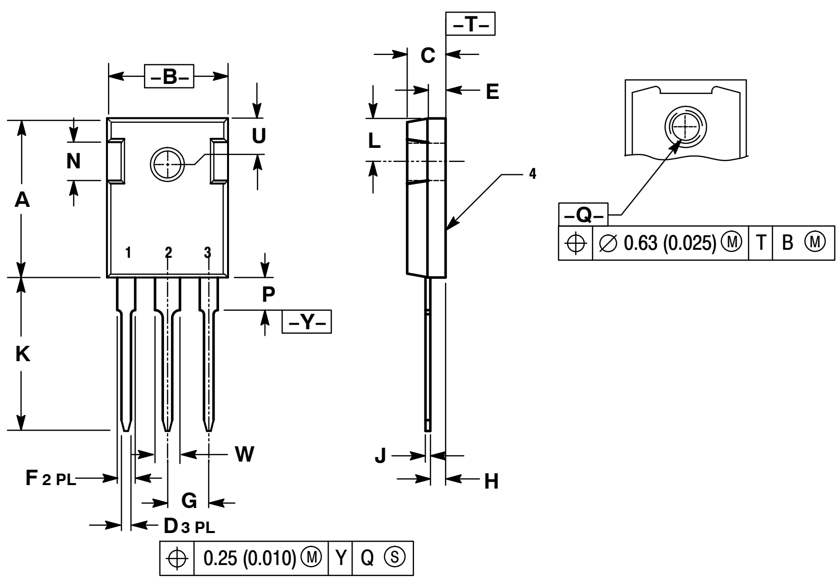
STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE 1
2. CATHODE(S)
3. ANODE 2
4. CATHODE(S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

TO−247
CASE 340L−02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	2.20	2.60	0.087	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	20.06	20.83	0.790	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

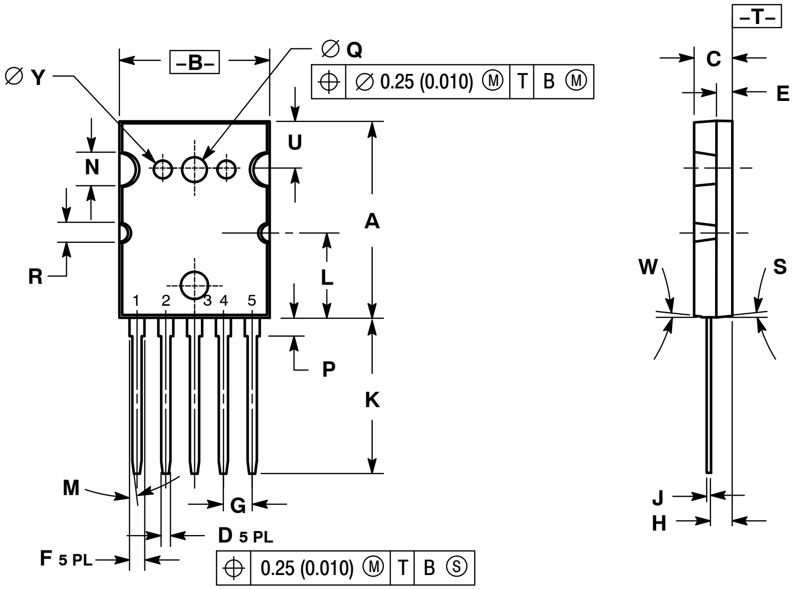
STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

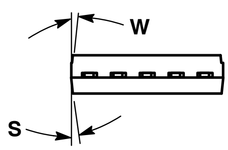
STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

TO−264, 5−LEAD
CASE 340AA−01
ISSUE O



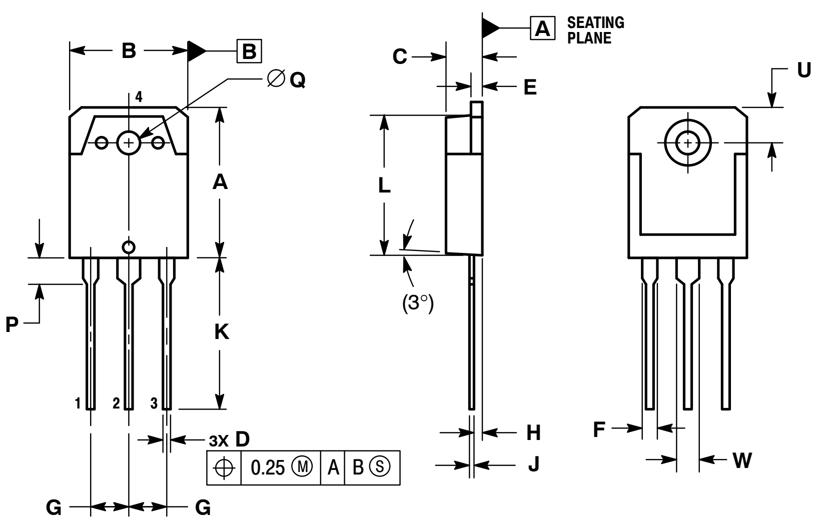


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	25.857	25.984	26.111	1.018	1.023	1.028
B	19.761	19.888	20.015	0.778	0.783	0.788
C	4.699	4.890	5.182	0.185	0.199	0.204
D		1.219 BSC			0.0480 BSC	
E	1.890	2.042	2.184	0.0748	0.0804	0.0860
F		1.981 BSC			0.0780 BSC	
G		3.81 BSC			0.150 BSC	
H	2.667	2.718	2.769	0.1050	0.1070	0.1090
J		0.584 BSC			0.0230 BSC	
K	20.422	20.549	20.676	0.804	0.809	0.814
L		11.28 REF			0.444 REF	
M	0 °	---	7 °	0 °	---	7 °
N		4.57 REF			0.180 REF	
P	2.259	2.386	2.513	0.0889	0.0939	0.0989
Q		3.480 BSC			0.1370 BSC	
R		2.54 REF			0.100 REF	
S	0 °	---	8 °	0 °	---	8 °
U		6.17 REF			0.243 REF	
W	0 °	---	6 °	0 °	---	6 °
Y		2.388 BSC			0.0940 BSC	

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. ANODE
5. CATHODE

TO−3P−3LD
CASE 340AB−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. DIMENSION A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

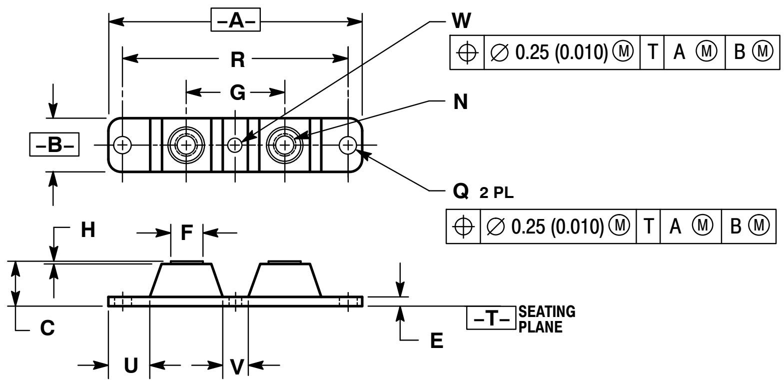
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	19.70	19.90	20.10
B	15.40	15.60	15.80
C	4.60	4.80	5.00
D	0.80	1.00	1.20
E	1.45	1.50	1.65
F	1.80	2.00	2.20
G		5.45 BSC	
H	1.20	1.40	1.60
J	0.55	0.60	0.75
K	19.80	20.00	20.20
L	18.50	18.70	18.90
P	3.30	3.50	3.70
Q	3.10	3.20	3.50
U		5.00 REF	
W	2.80	3.00	3.20

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

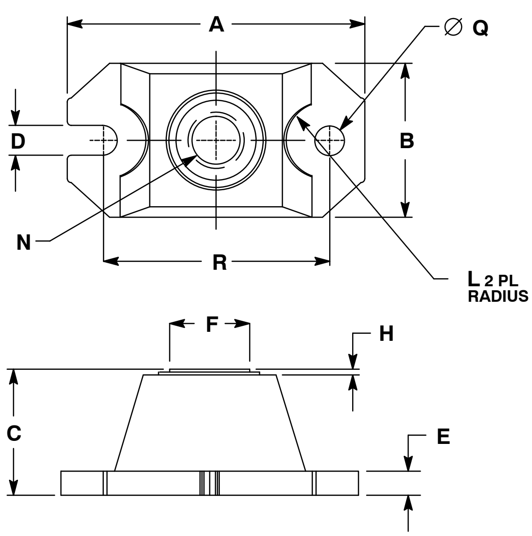
POWERTAP™ II
CASE 357C−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TERMINAL PENETRATION: 5.97 (0.235) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	3.450	3.635	87.63	92.33
B	0.700	0.810	17.78	20.57
C	0.615	0.640	15.63	16.26
E	0.120	0.130	3.05	3.30
F	0.435	0.445	11.05	11.30
G	1.370	1.380	34.80	35.05
H	0.007	0.030	0.18	0.76
N	1/4−20UNC−2B		1/4−20UNC−2B	
Q	0.270	0.285	6.86	7.23
R	31.50 BSC		80.01 BSC	
U	0.600	0.630	15.24	16.00
V	0.330	0.375	8.39	9.52
W	0.170	0.190	4.32	4.82

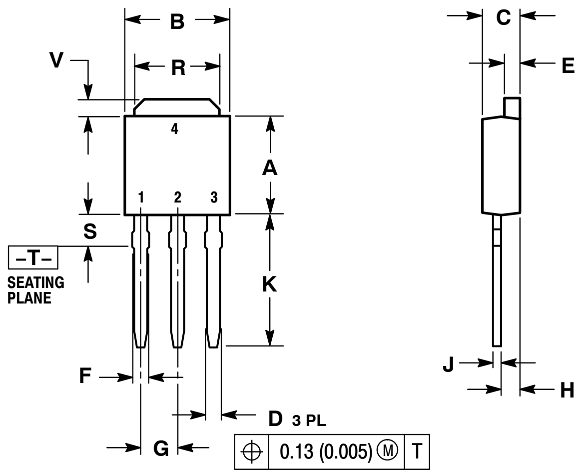
POWERTAP III
CASE 357D−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TERMINAL PENETRATION: 5.97 (0.235) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.520	1.560	38.61	39.62
B	0.783	0.813	19.89	20.65
C	0.615	0.635	15.62	16.13
D	0.152	0.162	3.86	4.11
E	0.120	0.130	3.05	3.30
F	0.435	0.445	11.05	11.30
H	0.007	0.030	0.18	0.76
L	0.210	0.230	5.33	5.84
N	1/4−20UNC−2B		1/4−20UNC−2B	
Q	0.152	0.162	3.86	4.11
R	1.175	1.195	29.85	30.35

DPAK STRAIGHT LEADS
CASE 369–07
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

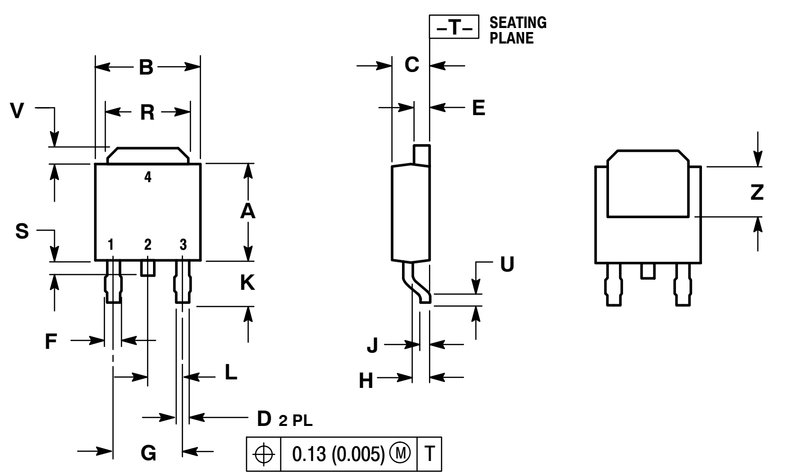
STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

DPAK
CASE 369A–13
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

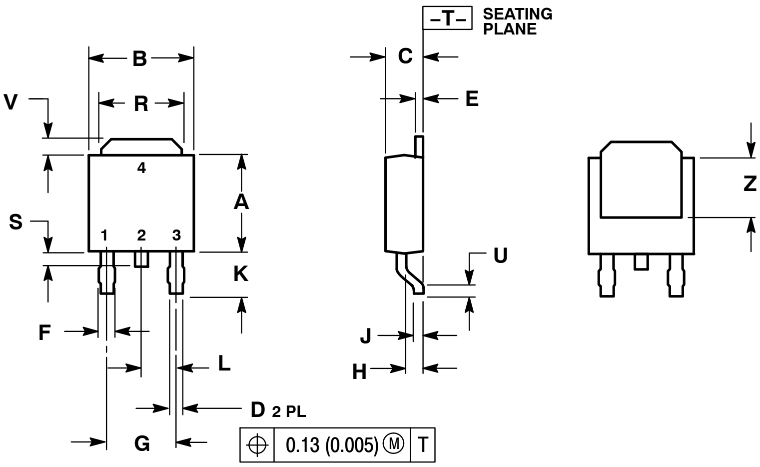
STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DPAK SINGLE GAUGE

CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

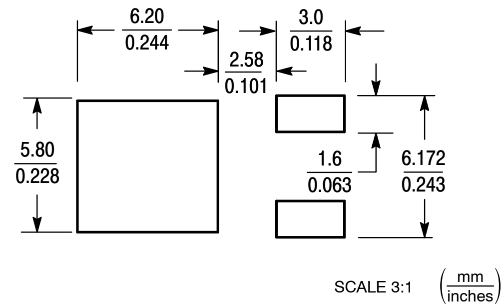
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

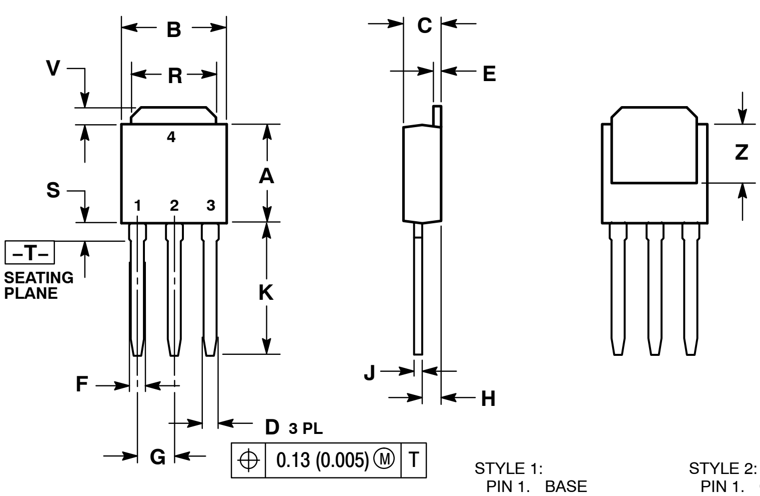
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

RECOMMENDED FOOTPRINT



DPAK SINGLE GAUGE STRAIGHT LEAD

CASE 369D−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

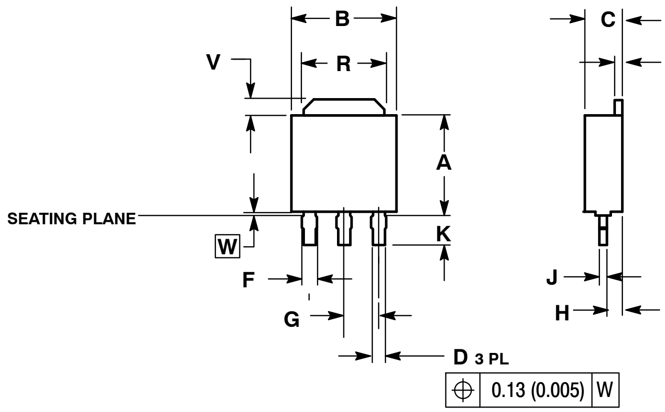
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

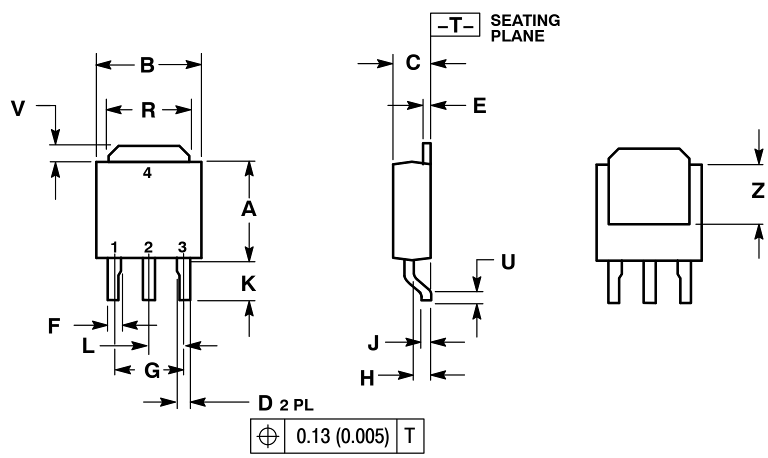
3 IPAK, STRAIGHT LEAD
CASE 369F−01
ISSUE O



NOTES:
1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.083	0.095	2.10	2.41
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

DPAK−3, SURFACE MOUNT
CASE 369G−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

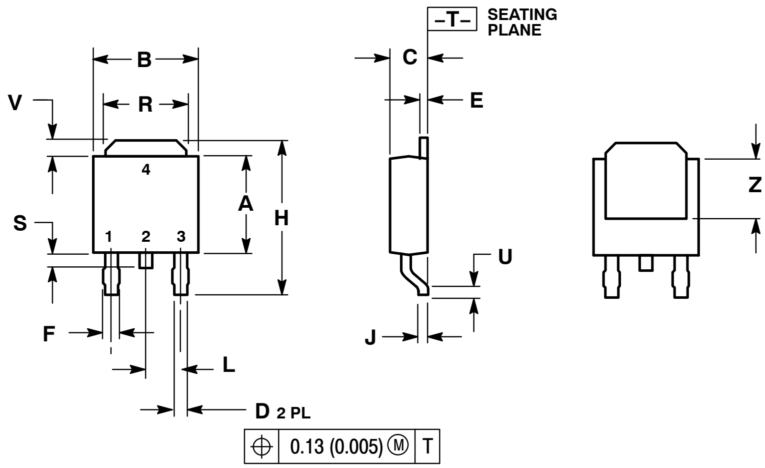
STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DPAK (SINGLE GAUGE)

CASE 369AA−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
H	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

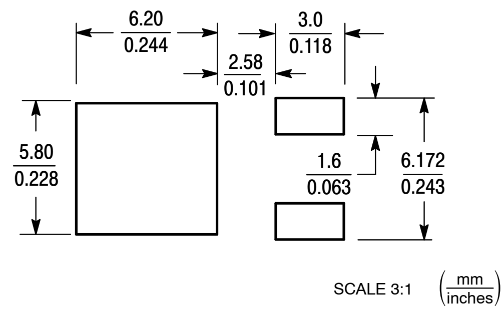
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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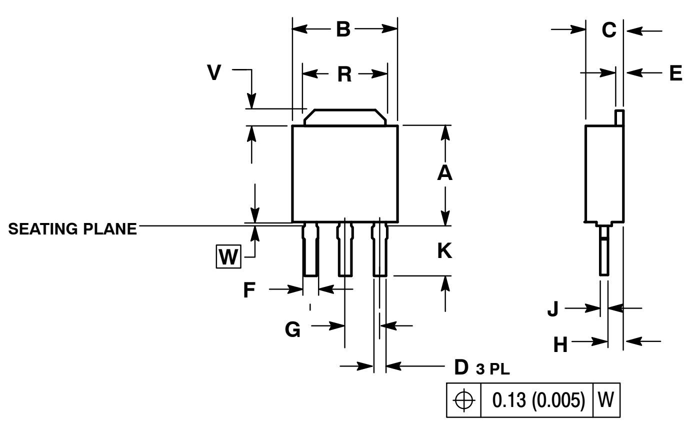
3 IPAK, STRAIGHT LEAD

CASE 369AC−01
ISSUE O

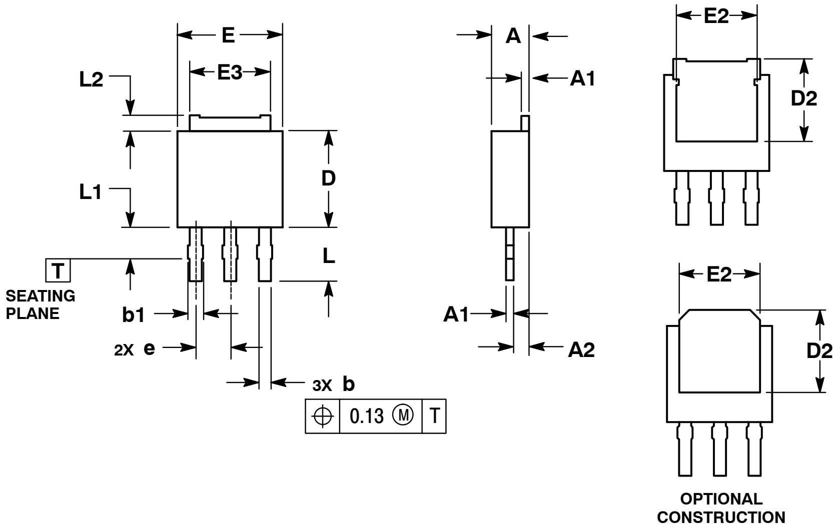


NOTES:
1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

3.5MM IPAK, STRAIGHT LEAD

CASE 369AD−01
ISSUE O

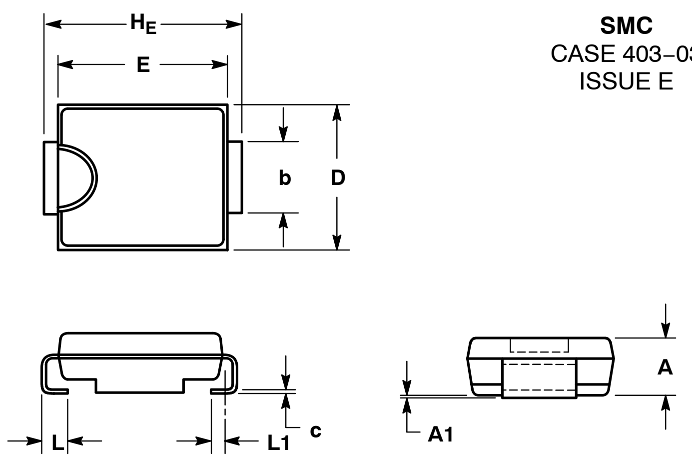


NOTES:
1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	−−−
E	6.35	6.73
E2	4.70	−−−
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	−−−	2.10
L2	0.89	1.27

SMC

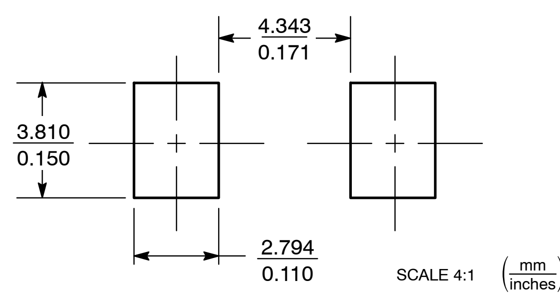
CASE 403−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.
4. 403−01 THRU −02 OBSOLETE, NEW STANDARD 403−03.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.90	2.13	2.41	0.075	0.084	0.095
A1	0.05	0.10	0.15	0.002	0.004	0.006
b	2.92	3.00	3.07	0.115	0.118	0.121
c	0.15	0.23	0.30	0.006	0.009	0.012
D	5.59	5.84	6.10	0.220	0.230	0.240
E	6.60	6.86	7.11	0.260	0.270	0.280
H_E	7.75	7.94	8.13	0.305	0.313	0.320
L	0.76	1.02	1.27	0.030	0.040	0.050
L1	0.51 REF			0.020 REF		

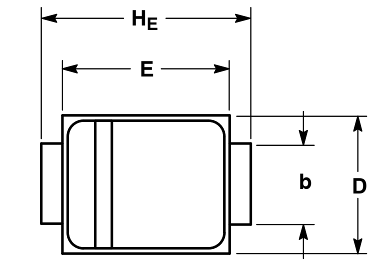
SOLDERING FOOTPRINT*

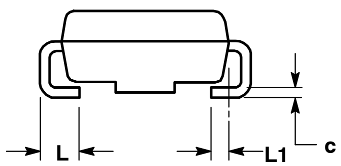


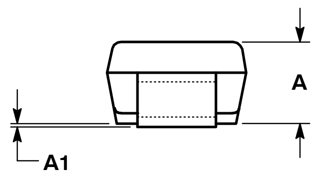
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SMB

DO−214AA
CASE 403A−03
ISSUE F



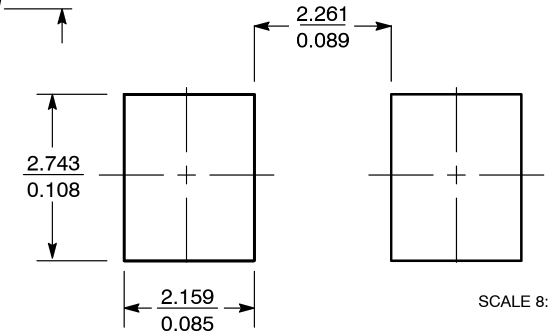




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.90	2.13	2.45	0.075	0.084	0.096
A1	0.05	0.10	0.20	0.002	0.004	0.008
b	1.96	2.03	2.20	0.077	0.080	0.087
c	0.15	0.23	0.31	0.006	0.009	0.012
D	3.30	3.56	3.95	0.130	0.140	0.156
E	4.06	4.32	4.60	0.160	0.170	0.181
H_E	5.21	5.44	5.60	0.205	0.214	0.220
L	0.76	1.02	1.60	0.030	0.040	0.063
L1	0.51 REF			0.020 REF		

SOLDERING FOOTPRINT*

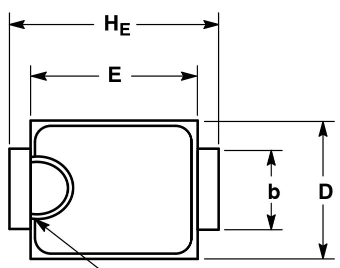


SCALE 8:1 $\left(\frac{mm}{inches}\right)$

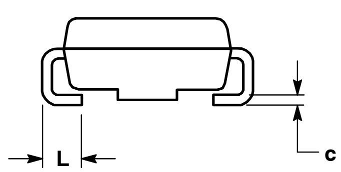
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

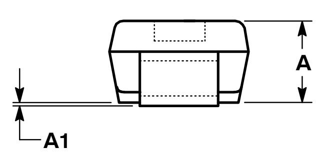
SMA

CASE 403B−02
ISSUE D



POLARITY INDICATOR OPTIONAL AS NEEDED

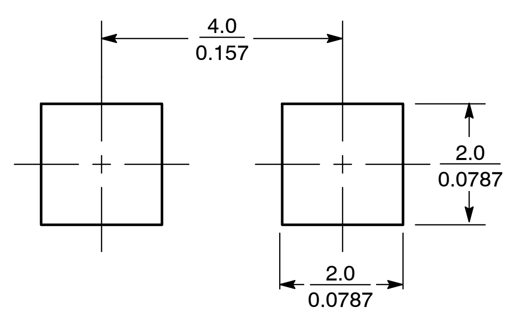




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 403B−01 OBSOLETE, NEW STANDARD 403B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.91	2.16	2.41	0.075	0.085	0.095
A1	0.05	0.10	0.15	0.002	0.004	0.006
b	1.27	1.45	1.63	0.050	0.057	0.064
c	0.15	0.28	0.41	0.006	0.011	0.016
D	2.29	2.60	2.92	0.090	0.103	0.115
E	4.06	4.32	4.57	0.160	0.170	0.180
H_E	4.83	5.21	5.59	0.190	0.205	0.220
L	0.76	1.14	1.52	0.030	0.045	0.060

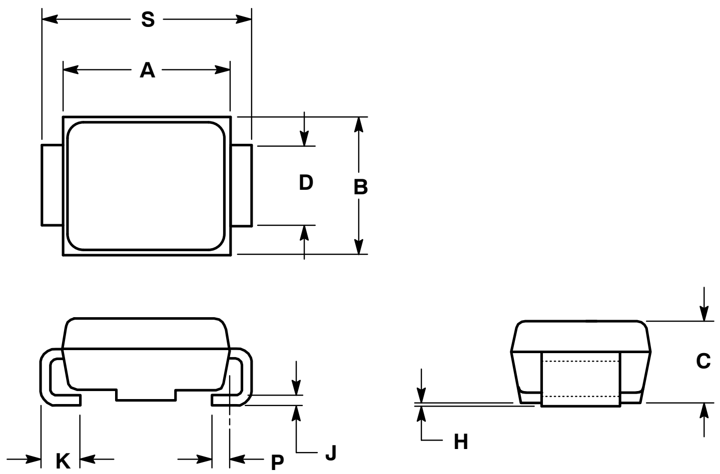
SOLDERING FOOTPRINT*



SCALE 8:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

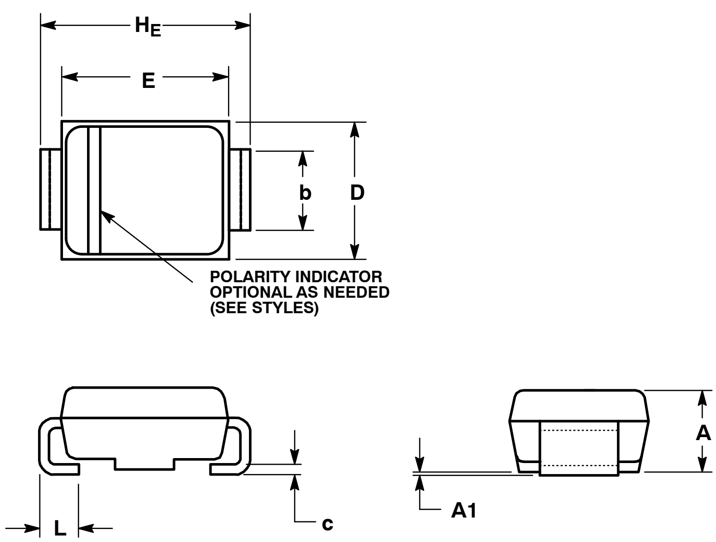
SMB
CASE 403C−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.160	0.180	4.06	4.57
B	0.130	0.150	3.30	3.81
C	0.075	0.095	1.90	2.41
D	0.077	0.083	1.96	2.11
H	0.0020	0.0060	0.051	0.152
J	0.006	0.012	0.15	0.30
K	0.030	0.050	0.76	1.27
P	0.020 REF		0.51 REF	
S	0.205	0.220	5.21	5.59

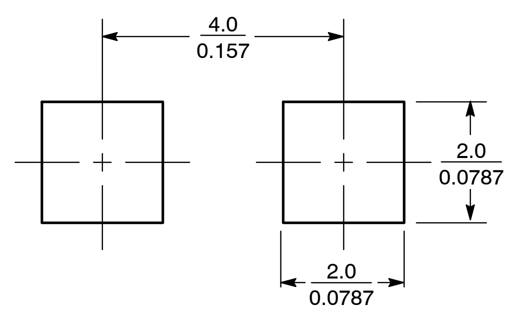
SMA
CASE 403D−02
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 403D−01 OBSOLETE, NEW STANDARD IS 403D−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.92	2.17	2.27	0.076	0.085	0.089
A1	0.05	0.10	0.15	0.002	0.004	0.006
b	1.27	1.45	1.63	0.050	0.057	0.064
c	0.15	0.28	0.41	0.006	0.011	0.016
D	2.29	2.60	2.92	0.090	0.103	0.115
E	4.06	4.32	4.57	0.160	0.170	0.180
H_E	4.83	5.21	5.59	0.190	0.205	0.220
L	0.76	1.14	1.52	0.030	0.045	0.060

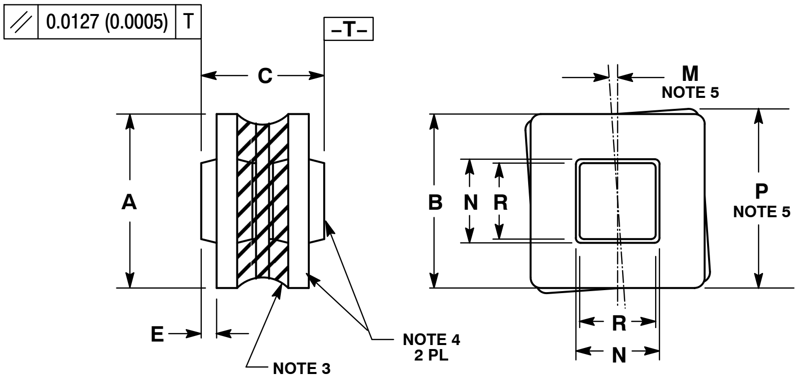
SOLDERING FOOTPRINT*



SCALE 8:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

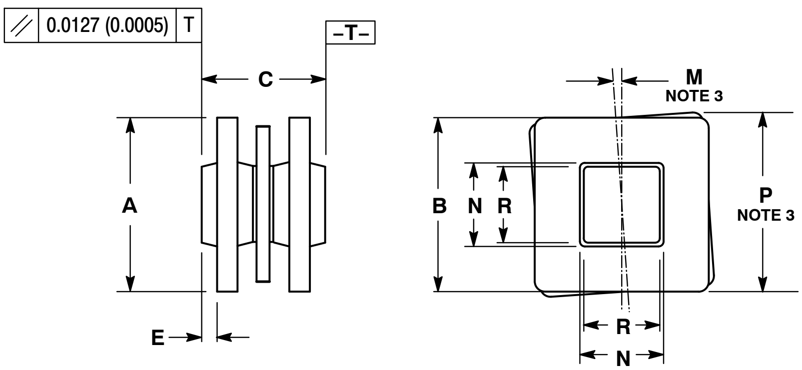
BUTTON
CASE 416–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. SEAL RING SEALANT SHALL NOT PROTRUDE OVER MAXIMUM DIMENSION NOTED.
4. THESE SURFACES SHALL BE COMPLETELY FREE OF SEALANT.
5. DIMENSION M AND P MAXIMUM MISALIGNMENT OF HALFS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.110	0.120	2.79	3.05
B	0.110	0.120	2.79	3.05
C	0.072	0.080	1.83	2.03
E	0.006	0.010	0.15	0.25
M	---	4°	---	4°
N	0.073	0.077	1.85	1.96
P	---	0.130	---	3.30
R	0.065	0.070	1.65	1.78

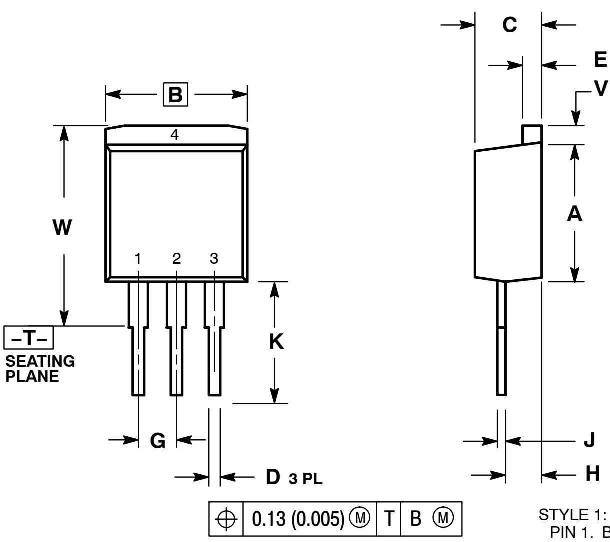
SSOVP BUTTON
CASE 416A–01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION M AND P MAXIMUM MISALIGNMENT OF HALFS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.110	0.120	2.79	3.05
B	0.110	0.120	2.79	3.05
C	0.072	0.080	1.83	2.03
E	0.006	0.010	0.15	0.25
M	---	4°	---	4°
N	0.073	0.077	1.85	1.96
P	---	0.130	---	3.30
R	0.065	0.070	1.65	1.78

D^{2}PAK, 3–LEAD, STRAIGHT
CASE 418–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418–01 THRU –04 OBSOLETE, NEW STANDARD 418–05.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.285	0.305	7.493	7.747
V	0.045	0.055	1.14	1.40
W	0.525	0.545	13.335	13.843

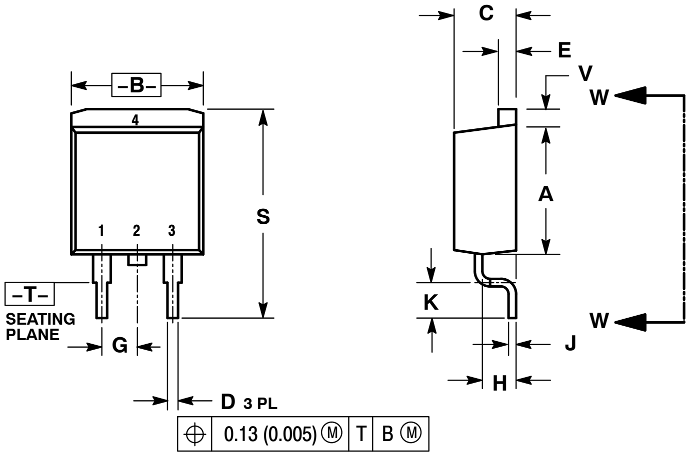
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

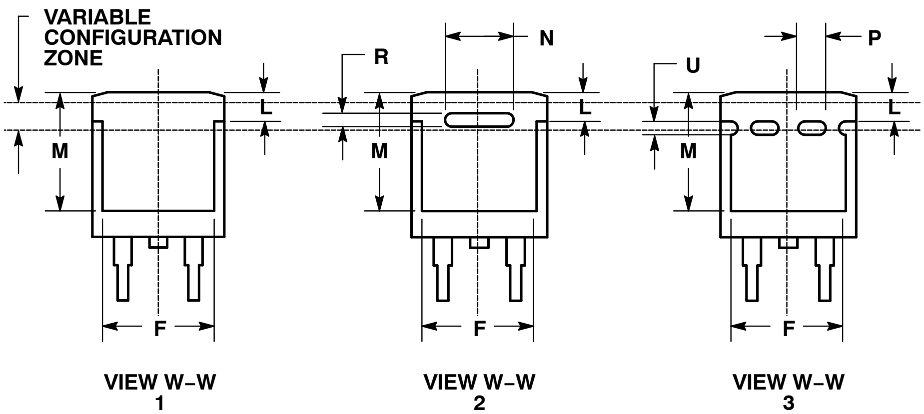
STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

D2PAK
CASE 418B−04
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

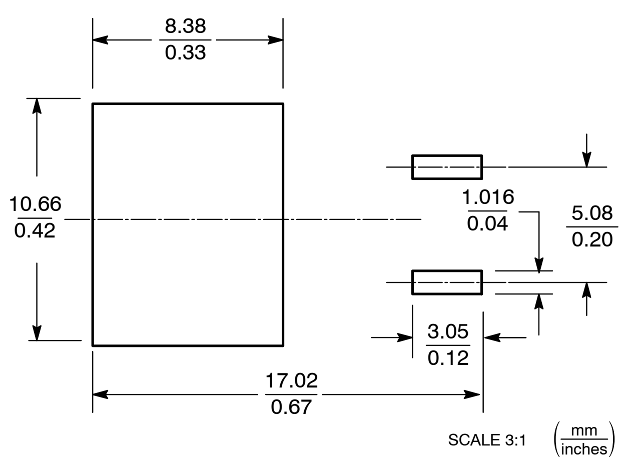
STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

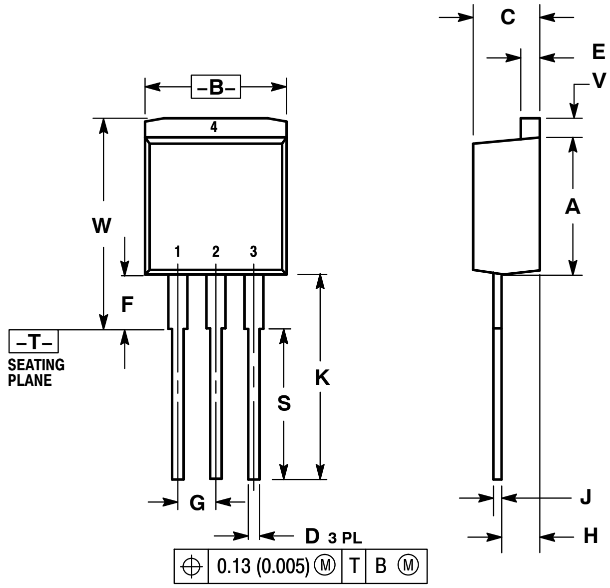
STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

I²PAK (TO−262)
CASE 418D−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.335	0.380	8.51	9.65
B	0.380	0.406	9.65	10.31
C	0.160	0.185	4.06	4.70
D	0.026	0.035	0.66	0.89
E	0.045	0.055	1.14	1.40
F	0.122 REF		3.10 REF	
G	0.100 BSC		2.54 BSC	
H	0.094	0.110	2.39	2.79
J	0.013	0.025	0.33	0.64
K	0.500	0.562	12.70	14.27
S	0.390 REF		9.90 REF	
V	0.045	0.070	1.14	1.78
W	0.522	0.551	13.25	14.00

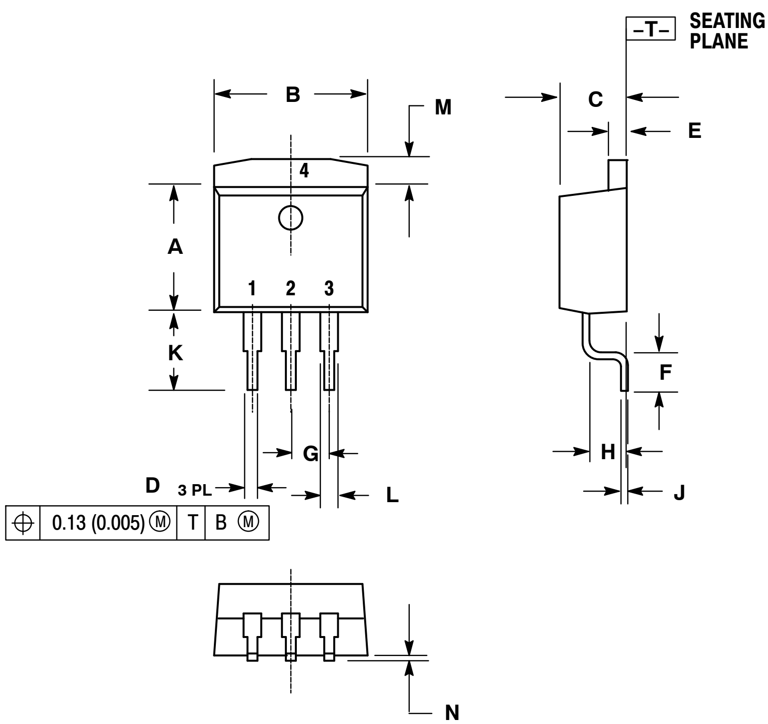
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

D²PAK LONG LEAD
CASE 418E−01
ISSUE O

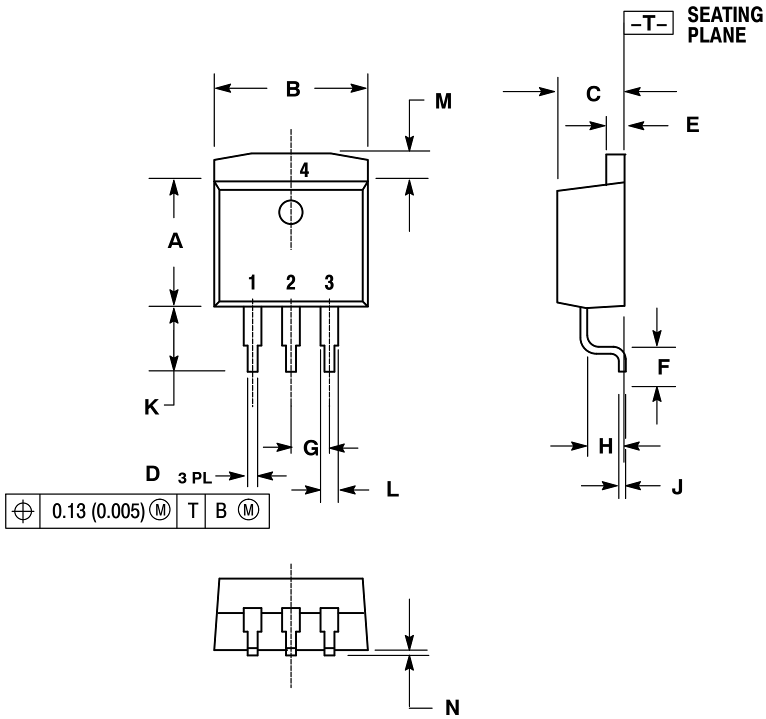


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.100 BSC		2.54 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
L	0.045	0.055	1.14	1.40
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

D²PAK SHORT LEAD

CASE 418F−01
ISSUE O

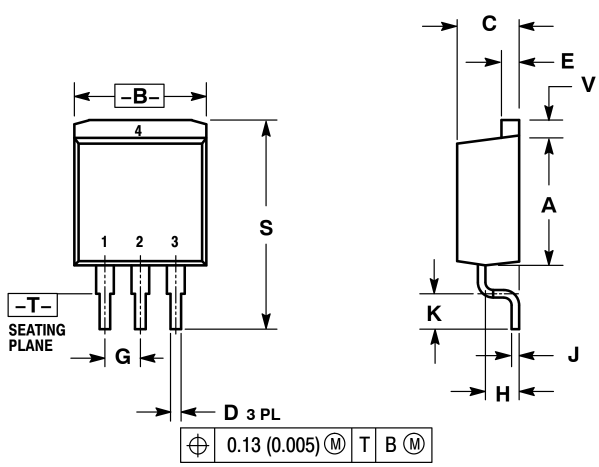


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.058	0.078	1.47	1.98
G	0.100 BSC		2.54 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.163	0.173	4.14	4.39
L	0.045	0.055	1.14	1.40
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

D²PAK

CASE 418G−01
ISSUE O

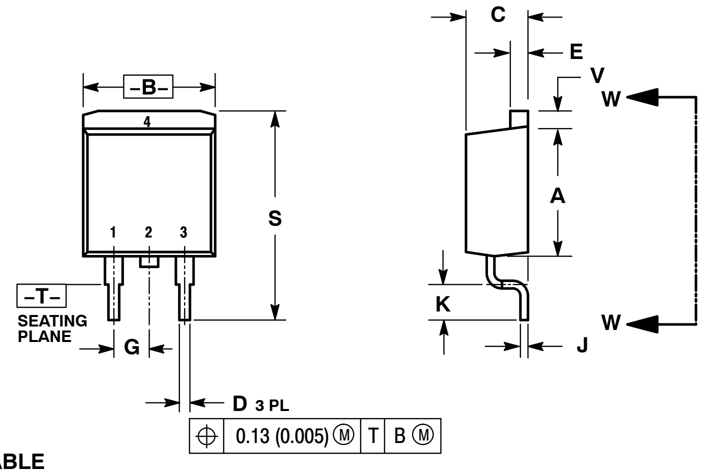


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

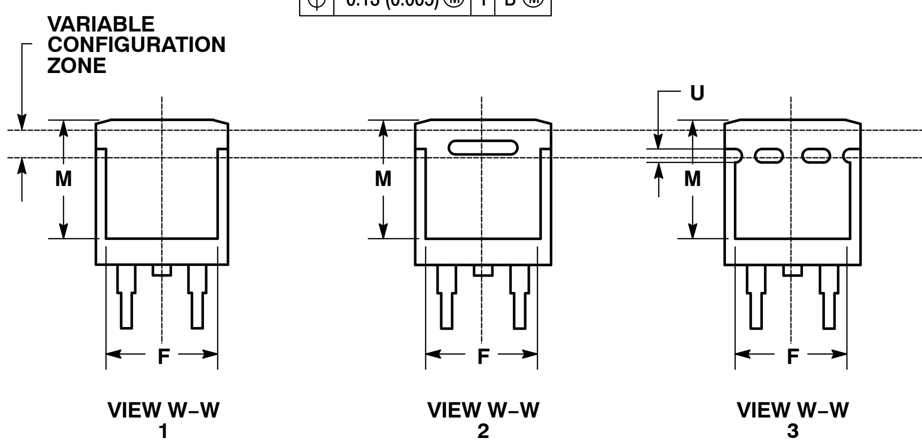
STYLE 1:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

D²PAK
CASE 418AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	−−−	7.87	−−−
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	−−−	7.11	−−−
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

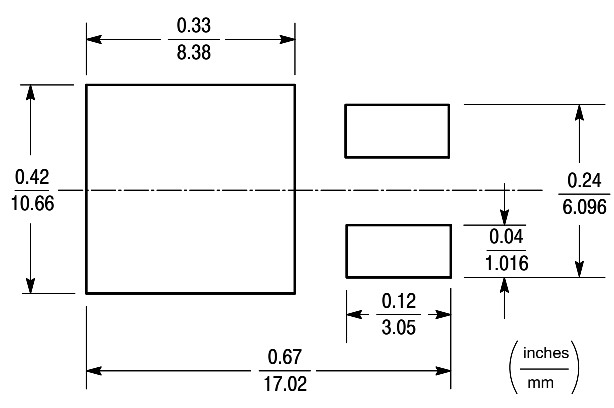
STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

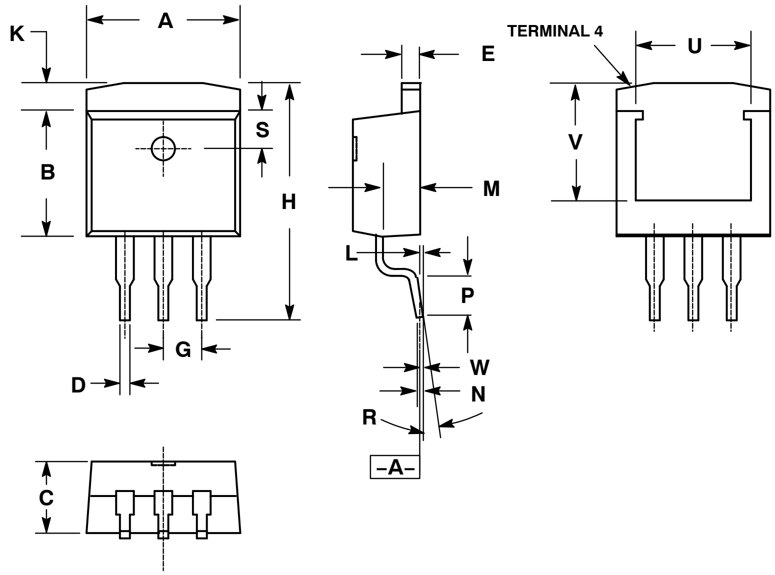
STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

RECOMMENDED FOOTPRINT



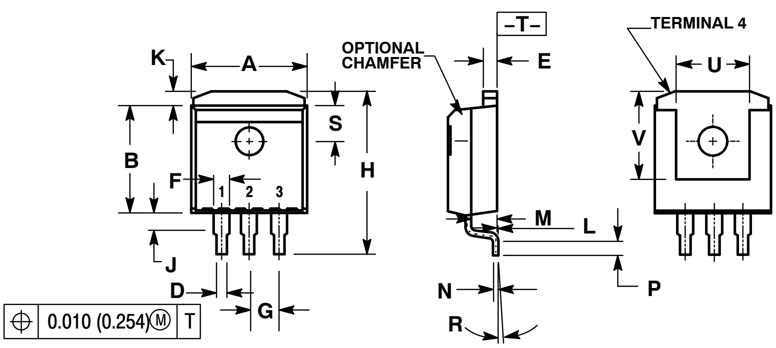
D²PAK−3
CASE 418AB−01
ISSUE O

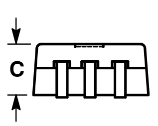


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURRS.
4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.396	0.406	10.05	10.31
B	0.330	0.340	8.38	8.64
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
G	0.100 REF		2.54 REF	
H	0.580	0.620	14.73	15.75
K	0.055	0.066	1.40	1.68
L	0.000	0.010	0.00	0.25
M	0.098	0.108	2.49	2.74
N	0.017	0.023	0.43	0.58
P	0.090	0.110	2.29	2.79
R	0°	8°	0°	8°
S	0.095	0.105	2.41	2.67
U	0.30 REF		7.62 REF	
V	0.305 REF		7.75 REF	
W	0.010		0.25	

D²PAK
CASE 418AF−01
ISSUE A

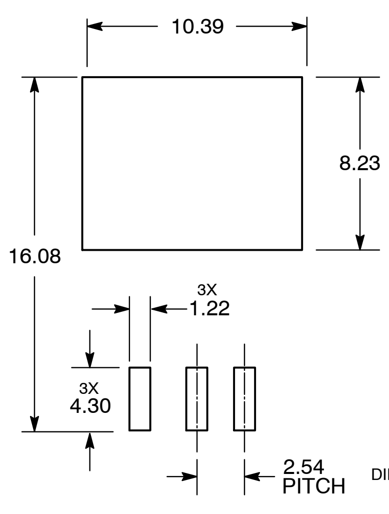




NOTES:
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.
5. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
6. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
7. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

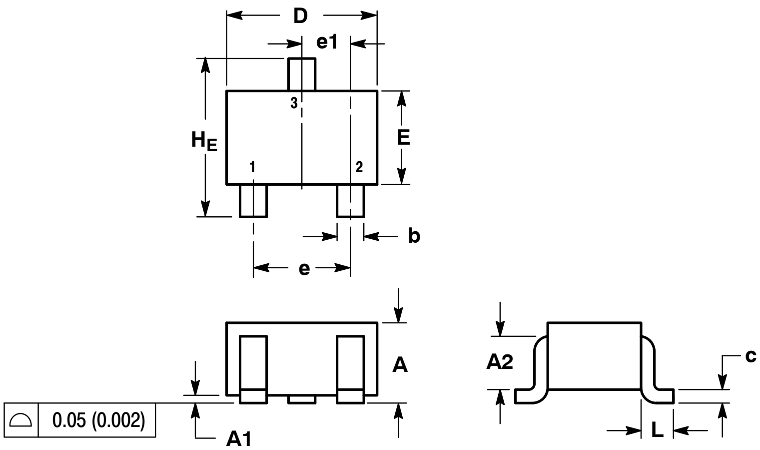
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT



DIMENSION: MILLIMETERS

SC−70
SOT−323
CASE 419−04
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.7 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L		0.425 REF			0.017 REF	
H_E	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

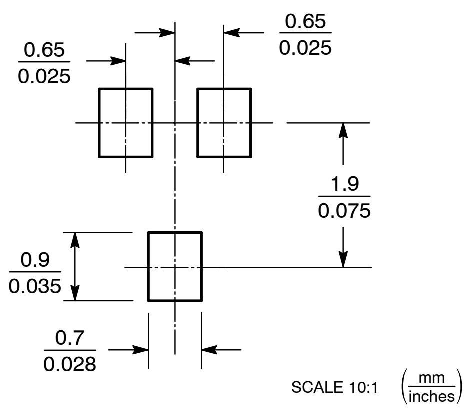
STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

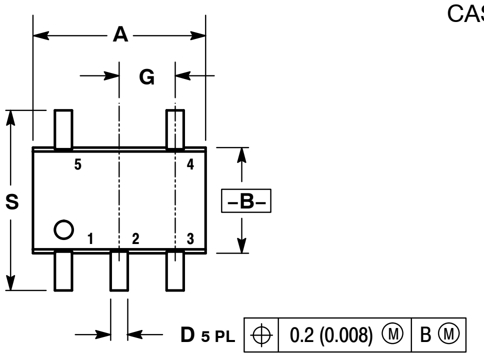
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

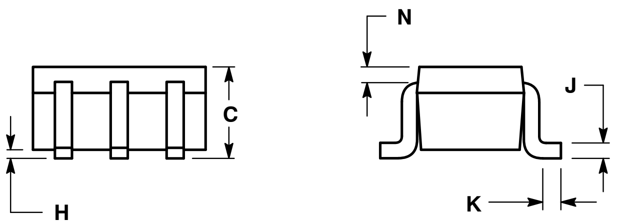
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SC−88A
SOT−353, SC70−5
CASE 419A−02
ISSUE J





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

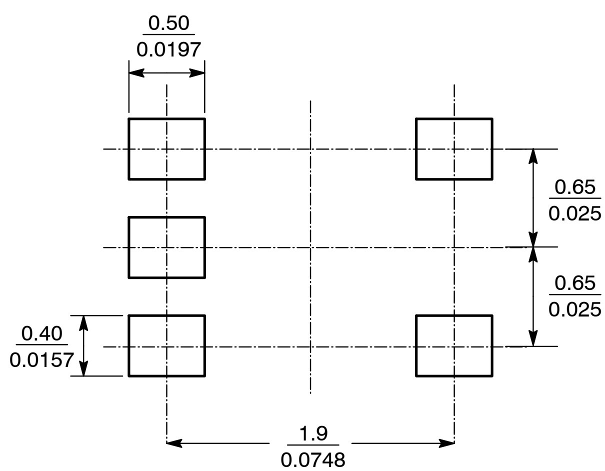
STYLE 6:
PIN 1. EMITTER
2. BASE
3. EMITTER
4. COLLECTOR
5. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

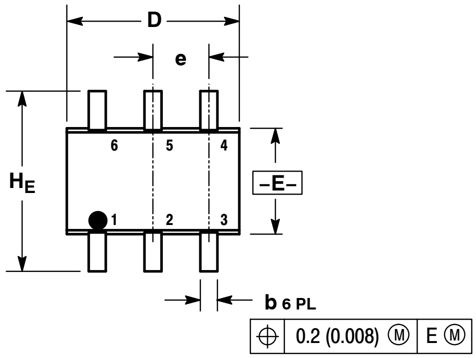
STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

SOLDERING FOOTPRINT*



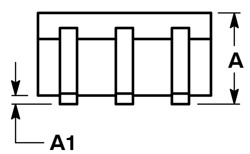
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

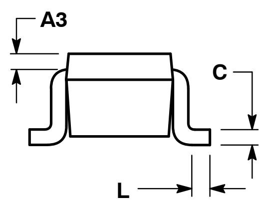


SC−88
SOT−363, SC70−6
CASE 419B−02
ISSUE W

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3		0.20 REF			0.008 REF	
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65 BSC			0.026 BSC	
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086





STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

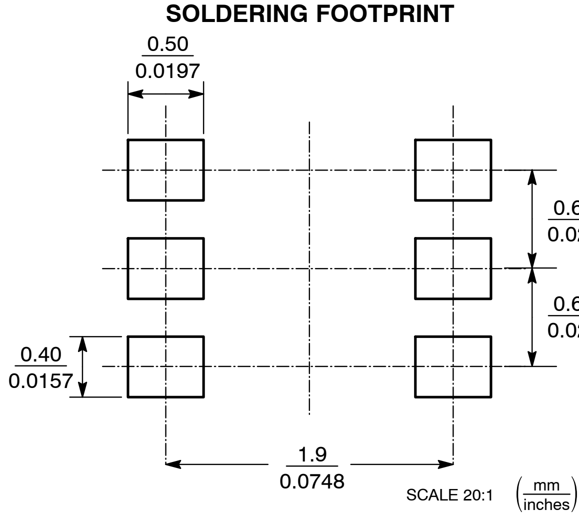
STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

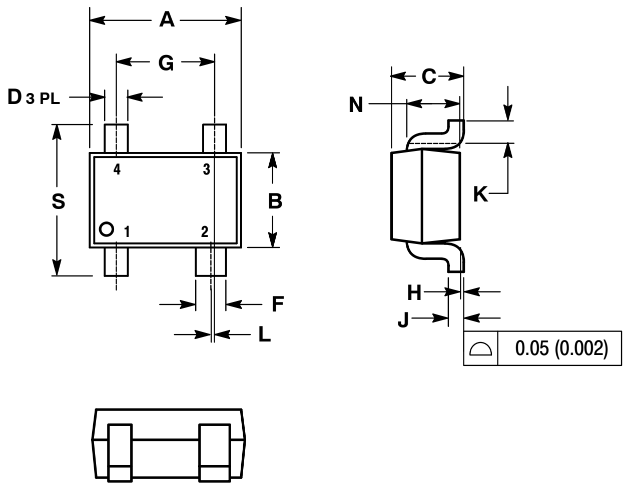
STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

SOLDERING FOOTPRINT



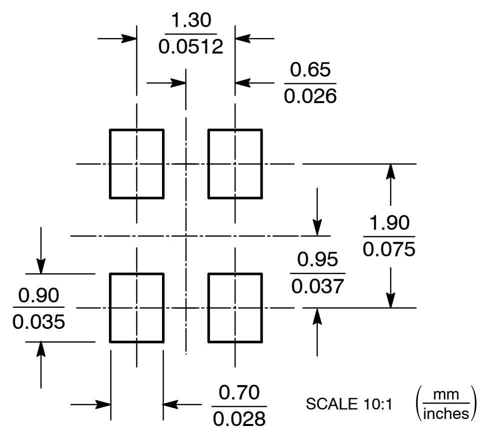
SC−82AB
SC70−4, SOT−343
CASE 419C−02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 419C−01 OBSOLETE. NEW STANDARD IS 419C−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

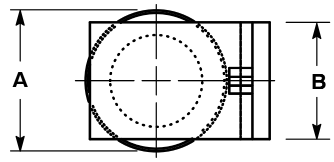
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.8	2.2	0.071	0.087
B	1.15	1.35	0.045	0.053
C	0.8	1.1	0.031	0.043
D	0.2	0.4	0.008	0.016
F	0.3	0.5	0.012	0.020
G	1.1	1.5	0.043	0.059
H	0.0	0.1	0.000	0.004
J	0.10	0.26	0.004	0.010
K	0.1	−−−	0.004	−−−
L	0.05 BSC		0.002 BSC	
N	0.2 REF		0.008 REF	
S	1.8	2.4	0.07	0.09

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

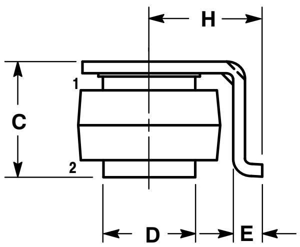
TAB MOUNT
CASE 421A−01
ISSUE A

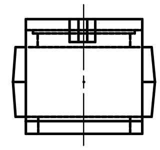


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

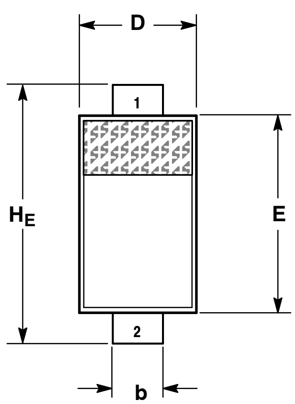
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.330	0.342	8.38	8.69
B	0.270	0.090	6.86	7.37
C	0.275	0.290	6.98	7.37
D	0.218	0.223	5.54	5.66
E	0.060	0.080	1.52	2.03
H	0.255	0.275	6.48	6.98

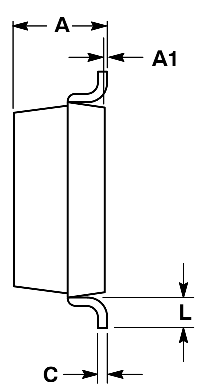
STYLE 1:
PIN 1. CATHODE
2. ANODE





SOD−123
SC−77
CASE 425−04
ISSUE E



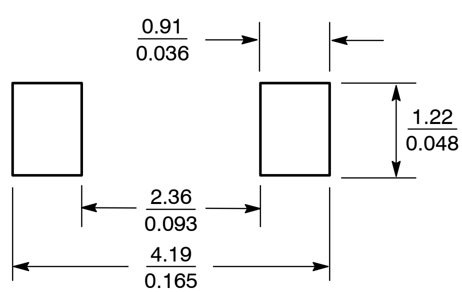


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX	INCHES MIN	INCHES NOM	INCHES MAX
A	0.94	1.17	1.35	0.037	0.046	0.053
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.51	0.61	0.71	0.020	0.024	0.028
c	---	---	0.15	---	---	0.006
D	1.40	1.60	1.80	0.055	0.063	0.071
E	2.54	2.69	2.84	0.100	0.106	0.112
H_E	3.56	3.68	3.86	0.140	0.145	0.152
L	0.25	---	---	0.010	---	---

STYLE 1:
PIN 1. CATHODE
2. ANODE

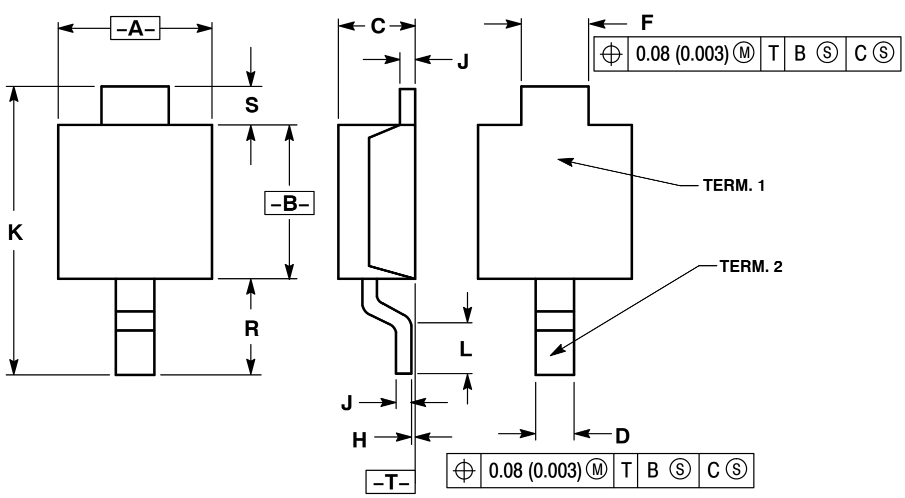
SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

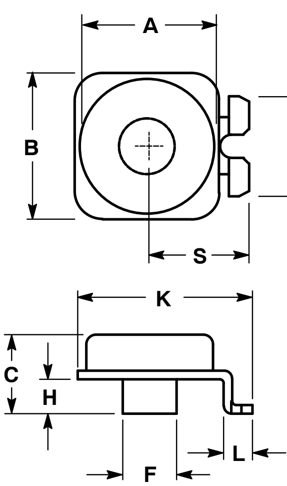
POWERMITE®
CASE 457−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.75	2.05	0.069	0.081
B	1.75	2.18	0.069	0.086
C	0.85	1.15	0.033	0.045
D	0.40	0.69	0.016	0.027
F	0.70	1.00	0.028	0.039
H	−0.05	+0.10	−0.002	+0.004
J	0.10	0.25	0.004	0.010
K	3.60	3.90	0.142	0.154
L	0.50	0.80	0.020	0.031
R	1.20	1.50	0.047	0.059
S	0.50 REF		0.019 REF	

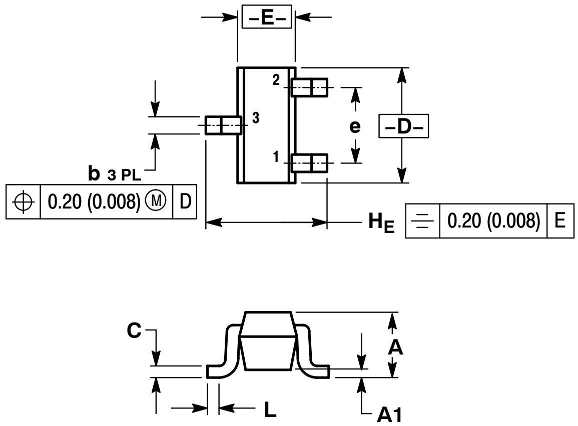
TOP CAN
CASE 460−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.1	9.5	0.358	0.374
B	9.5	9.9	0.374	0.390
C	5.2	5.6	0.205	0.220
D	6.4	6.8	0.252	0.268
F	3.4	3.8	0.134	0.149
H	2.0	2.4	0.079	0.095
K	11.4	11.8	0.449	0.465
L	1.8	2.2	0.071	0.087
S	6.5	6.9	0.256	0.272

SC−75
SOT−416
CASE 463−01
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.80	0.90	0.027	0.031	0.035
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.15	0.20	0.30	0.006	0.008	0.012
C	0.10	0.15	0.25	0.004	0.006	0.010
D	1.55	1.60	1.65	0.059	0.063	0.067
E	0.70	0.80	0.90	0.027	0.031	0.035
e	1.00 BSC			0.04 BSC		
L	0.10	0.15	0.20	0.004	0.006	0.008
H_E	1.50	1.60	1.70	0.061	0.063	0.065

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

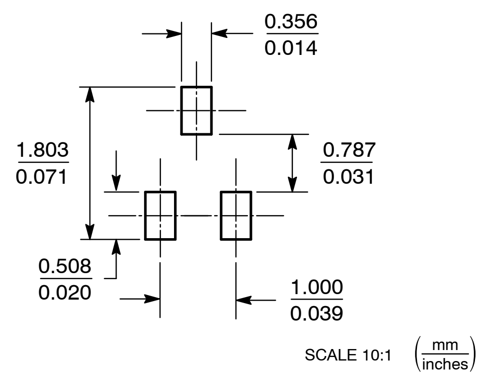
STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

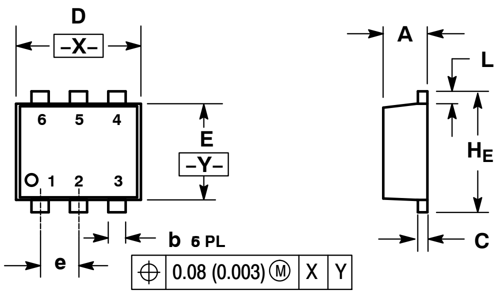
STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOT−563
CASE 463A−01
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

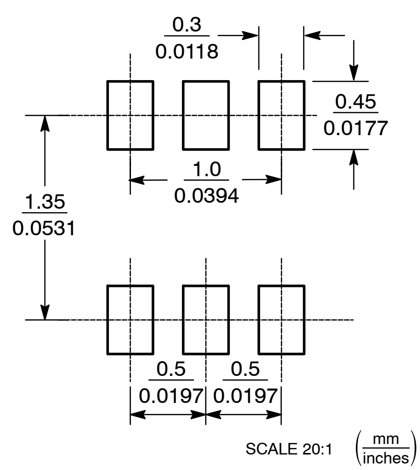
STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

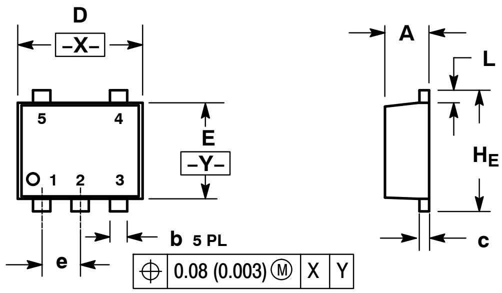
STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOT−553
CASE 463B−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.08	0.13	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.063	0.067
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.50 BSC			0.020 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.063	0.067

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

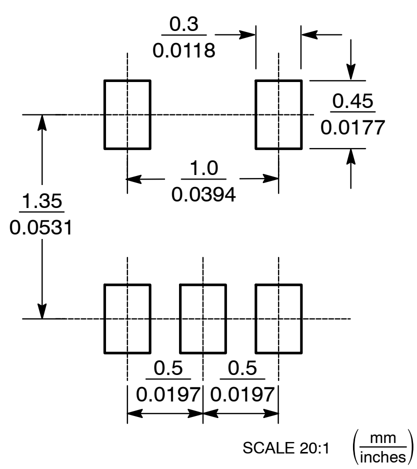
STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR 1
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

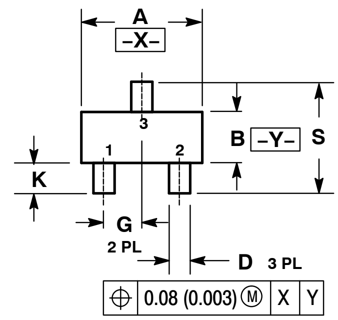
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

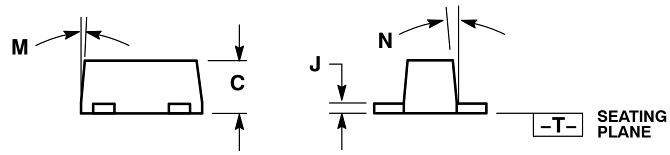
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SC−89
CASE 463C−03
ISSUE C





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C−01 OBSOLETE, NEW STANDARD 463C−02.

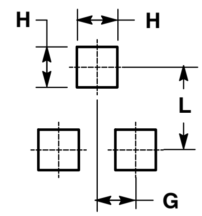
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50 BSC			0.020 BSC		
H	0.53 REF			0.021 REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L	1.10 REF			0.043 REF		
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

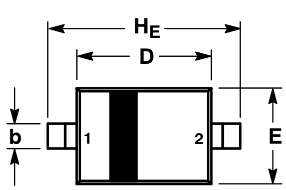
STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

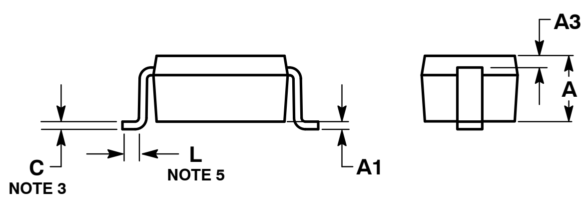


RECOMMENDED PATTERN OF SOLDER PADS

SOD−323
SC−76
CASE 477−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DIMENSION L IS MEASURED FROM END OF RADIUS.

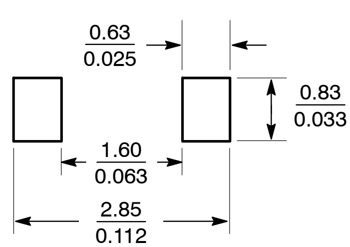


	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.031	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.15 REF			0.006 REF		
b	0.25	0.32	0.4	0.010	0.012	0.016
C	0.089	0.12	0.177	0.003	0.005	0.007
D	1.60	1.70	1.80	0.062	0.066	0.070
E	1.15	1.25	1.35	0.045	0.049	0.053
L	0.08			0.003		
H_E	2.30	2.50	2.70	0.090	0.098	0.105

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

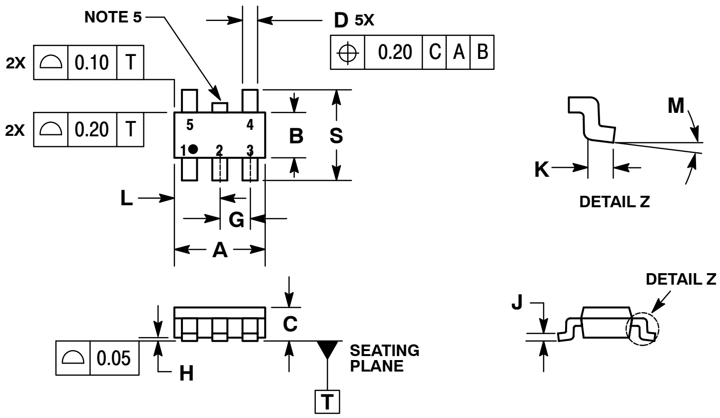
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

TSOP−5

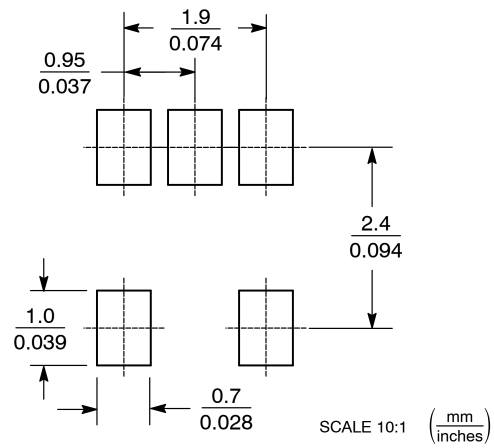
SOT23−5, SC59−5, SC−74A
CASE 483−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

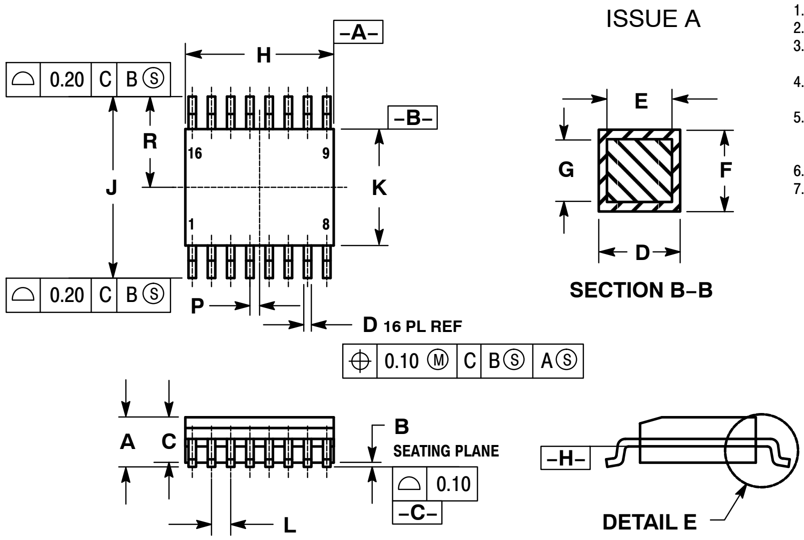
	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT

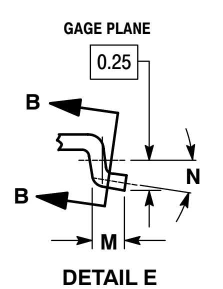


SOP

CASE 484−01
ISSUE A

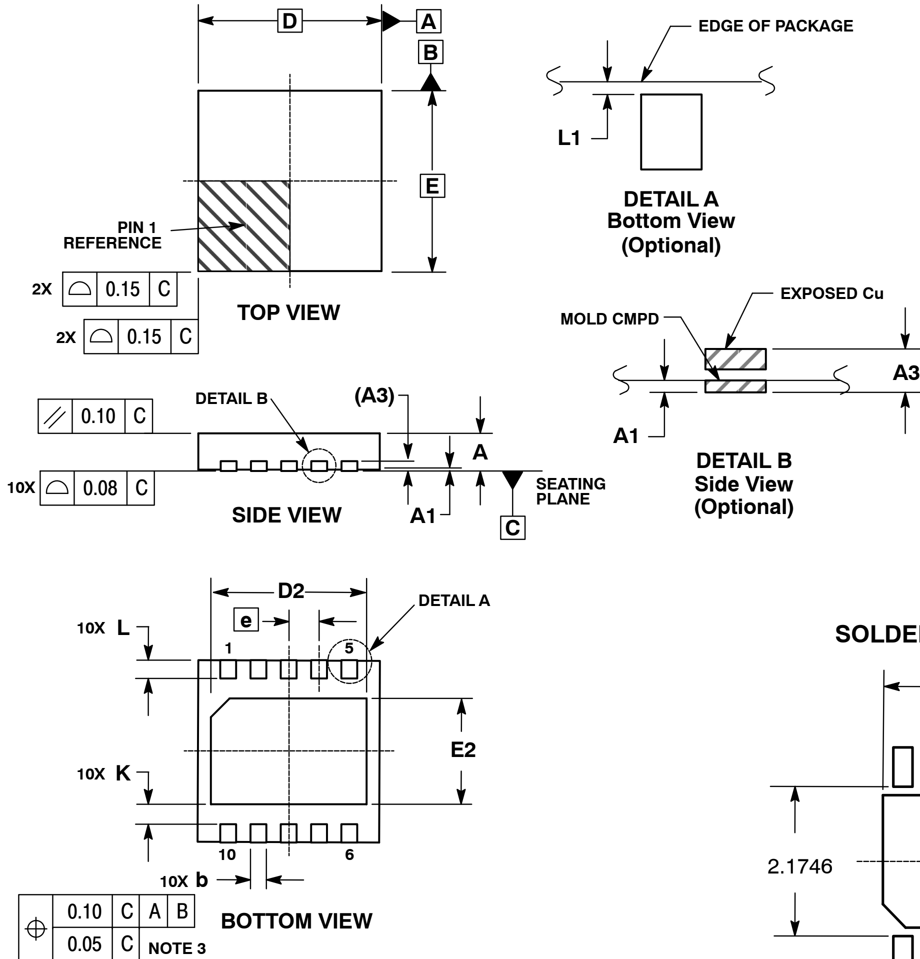


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION K DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION H AND J ARE TO BE DETERMINED AT DATUM PLANE H.



	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
B	0.10	0.25
C	1.10	1.65
D	0.21	0.31
E	−−−	−−−
F	0.19	0.25
G	−−−	−−−
H	4.80	4.98
J	6.00 BSC	
K	3.81	3.99
L	0.635 BSC	
M	0.41	1.27
N	0 °	8 °
P	0.318 BSC	
R	3.00 BSC	

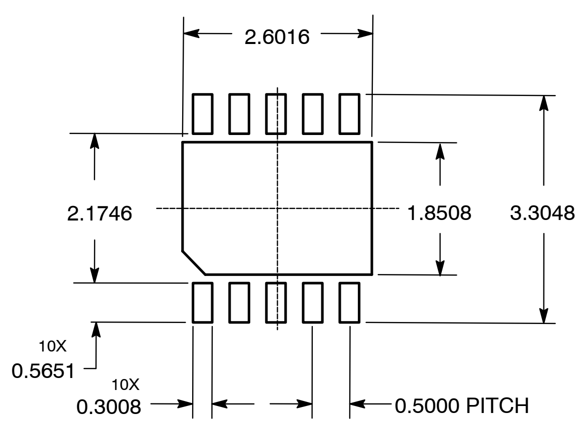
DFN10, 3x3
CASE 485C−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	2.45	2.55
E	3.00 BSC	
E2	1.75	1.85
e	0.50 BSC	
K	0.19 TYP	
L	0.35	0.45
L1	0.00	0.03

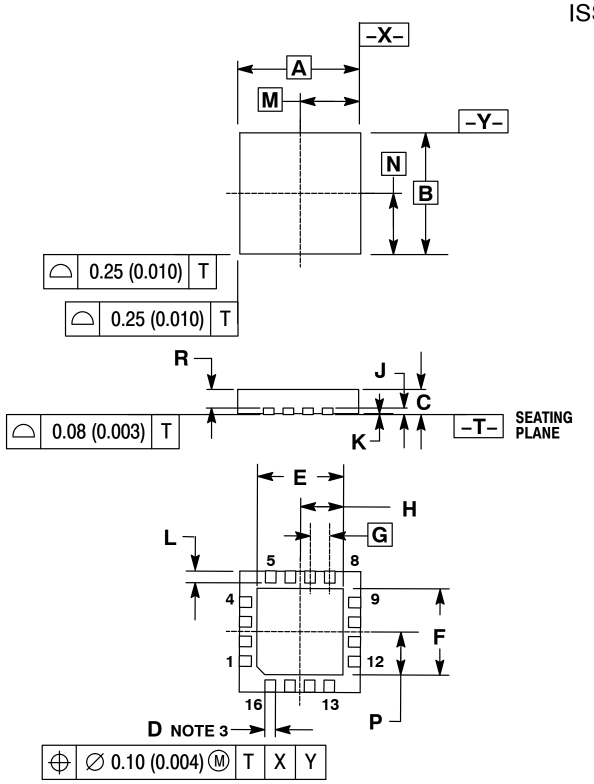
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

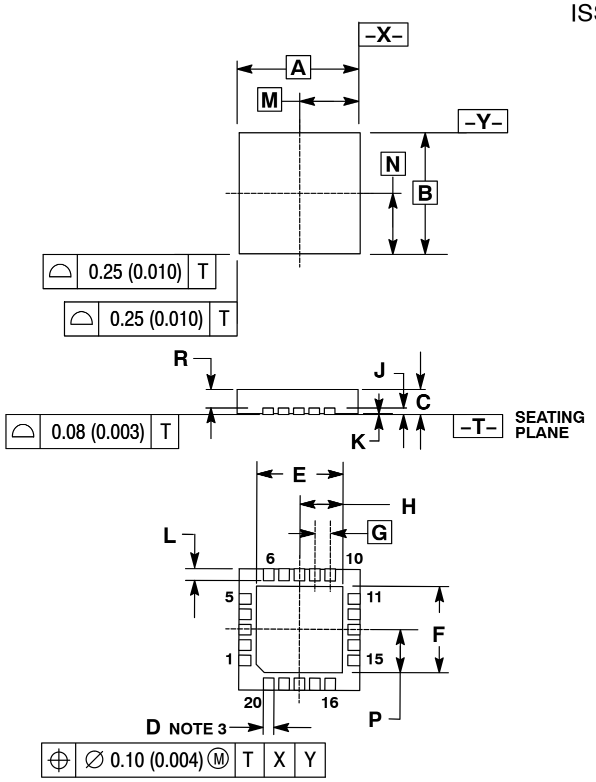
QFN16, 4x4
CASE 485D−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.00 BSC		0.157 BSC	
B	4.00 BSC		0.157 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.35	0.009	0.014
E	2.75	2.85	0.108	0.112
F	2.75	2.85	0.108	0.112
G	0.65 BSC		0.026 BSC	
H	1.38	1.43	0.054	0.056
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	2.00 BSC		0.079 BSC	
N	2.00 BSC		0.079 BSC	
P	1.38	1.43	0.054	0.056
R	0.60	0.80	0.024	0.031

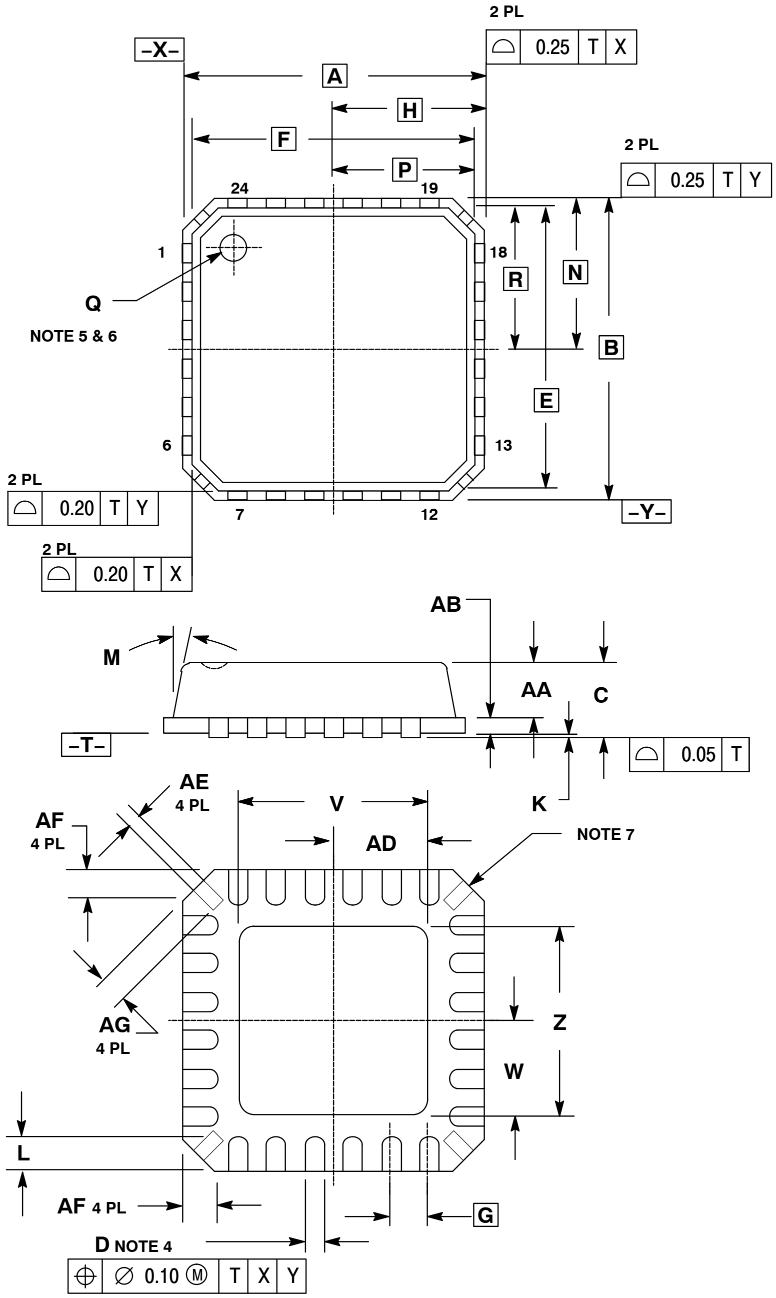
QFN20, 4x4
CASE 485E−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.00 BSC		0.157 BSC	
B	4.00 BSC		0.157 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.35	0.009	0.014
E	2.75	2.85	0.108	0.112
F	2.75	2.85	0.108	0.112
G	0.50 BSC		0.020 BSC	
H	1.38	1.43	0.054	0.056
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	2.00 BSC		0.079 BSC	
N	2.00 BSC		0.079 BSC	
P	1.38	1.43	0.054	0.056
R	0.60	0.80	0.024	0.031

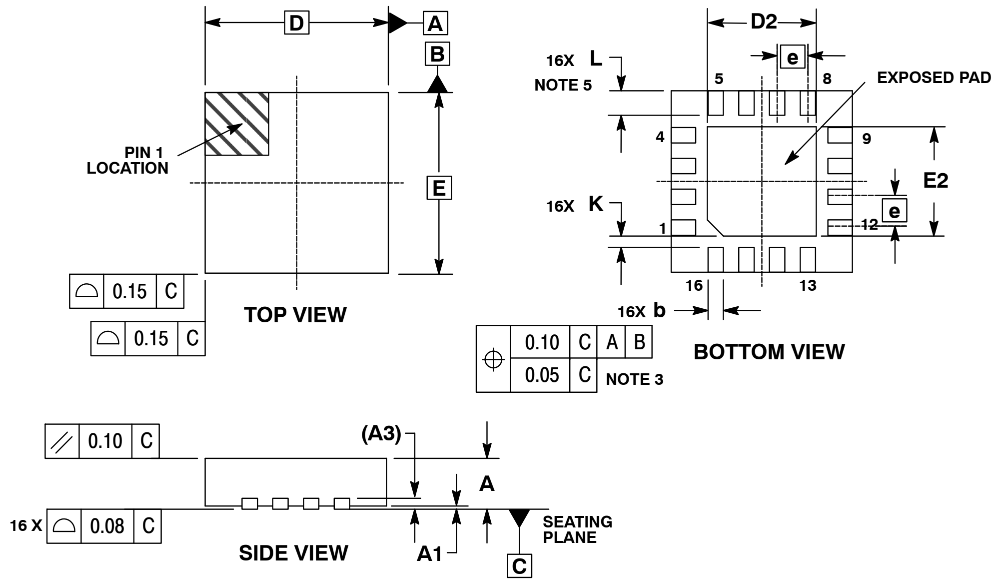
24−PIN MLF
CASE 485F−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIE THICKNESS ALLOWABLE IS 0.305 MM MAXIMUM (0.012 INCHES MAXIMUM).
4. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 MM FROM TERMINAL.
5. THE PIN #1 IDENTIFIER MUST BE ON THE TOP SURFACE OF THE PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
8. PACKAGE WARPAGE MAX 0.05 MM.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.00 BSC		0.157 BSC	
B	4.00 BSC		0.157 BSC	
C	---	1.00	---	0.039
D	0.18	0.30	0.007	0.012
E	3.75 BSC		0.148 BSC	
F	3.75 BSC		0.148 BSC	
G	0.50 BSC		0.020 BSC	
H	2.00 BSC		0.79 BSC	
K	0.01	0.05	0.000	0.002
L	0.30	0.55	0.012	0.022
M	---	12 °	---	12 °
N	2.00 BSC		0.079 BSC	
P	1.88 BSC		0.074 BSC	
Q	0.50 DIA		0.020 DIA	
R	1.88 BSC		0.079 BSC	
V	2.50 BSC		0.098 BSC	
W	1.30 BSC		0.051 BSC	
Z	2.50 BSC		0.098 BSC	
AA	0.65	0.80	0.026	0.031
AB	0.20 REF		0.008 REF	
AD	1.30 BSC		0.051 BSC	
AE	0.13	0.23	0.005	0.009
AF	0.24	0.60	0.009	0.024
AG	0.30	0.45	0.012	0.018

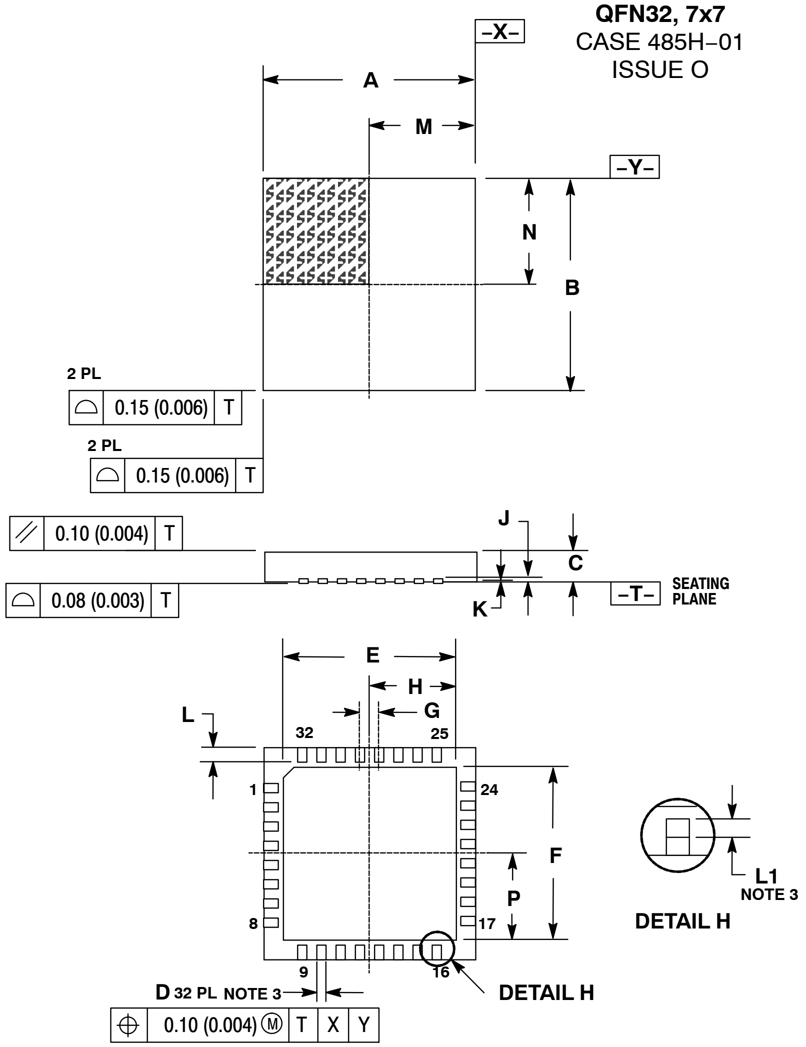
QFN16, 3x3
CASE 485G−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

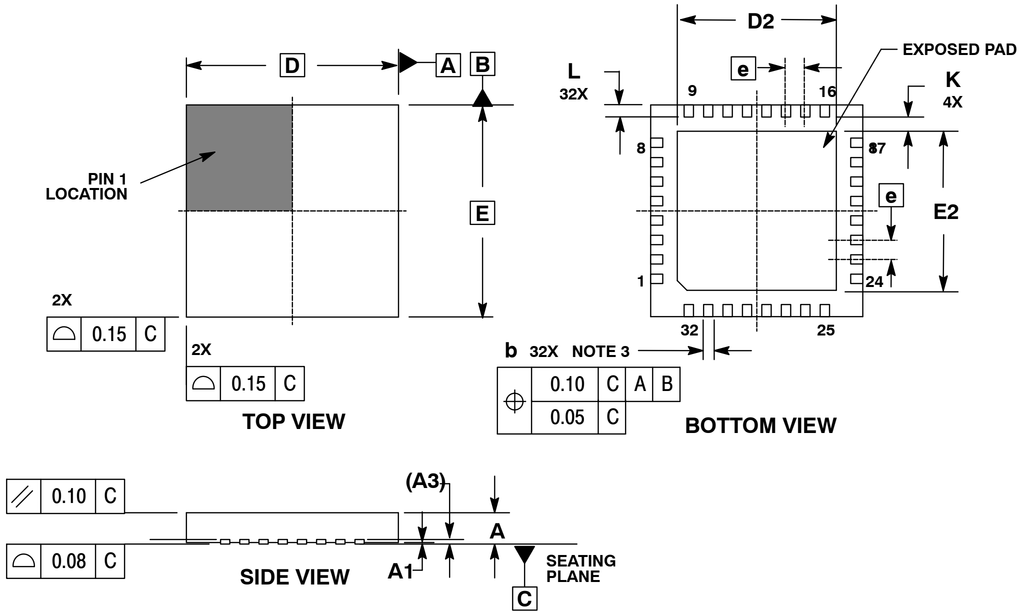
QFN32, 7x7
CASE 485H−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE UP TO 0.1 MM IS ACCEPTABLE. L1 IS OPTIONAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.90	7.10	0.272	0.280
B	6.90	7.10	0.272	0.280
C	0.80	1.00	0.031	0.039
D	0.30	0.35	0.012	0.014
E	5.65	5.95	0.222	0.234
F	5.65	0.95	0.222	0.234
G	0.65 BSC		0.026 BSC	
H	2.83	2.98	0.111	0.117
J	0.25 REF		0.010 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	3.45	3.55	0.136	0.140
N	3.45	3.55	0.136	0.140
P	2.83	2.98	0.111	0.117

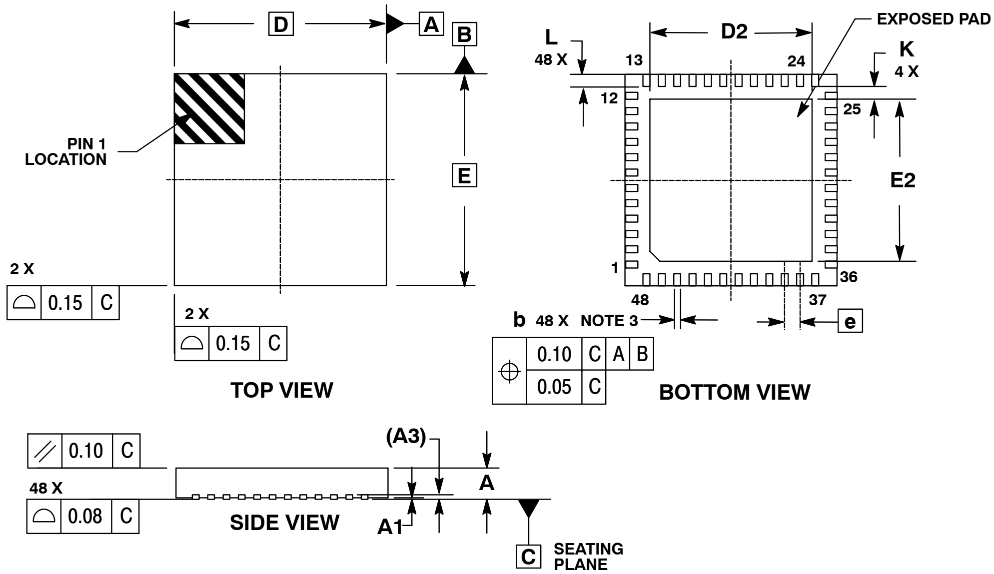
QFN32, 7x7
CASE 485J−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.250	0.250	0.350
D	7.00 BSC		
D2	5.160	5.260	5.360
E	7.00 BSC		
E2	5.160	5.260	5.360
e	0.650 BSC		
K	0.200	−−−	−−−
L	0.300	0.400	0.500

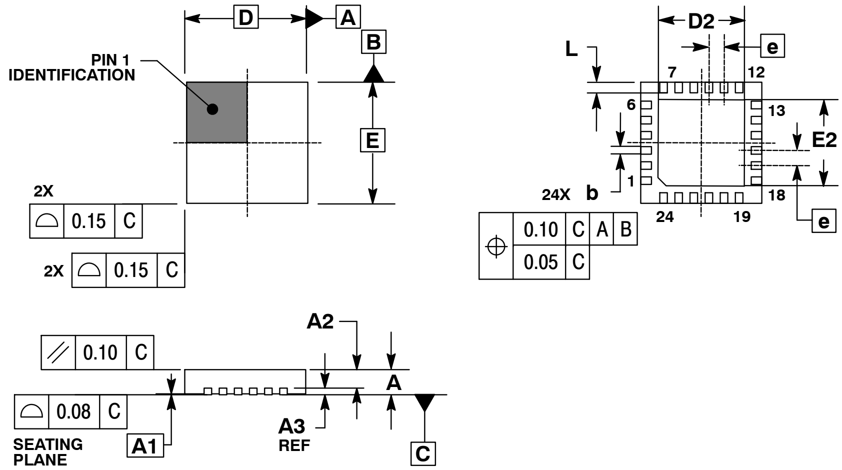
QFN48, 7x7
CASE 485K−02
ISSUE C



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	7.000 BSC		
D2	5.260	5.360	5.460
E	7.000 BSC		
E2	5.260	5.360	5.460
e	0.500 BSC		
K	0.200	−−−−	−−−−
L	0.300	0.400	0.500

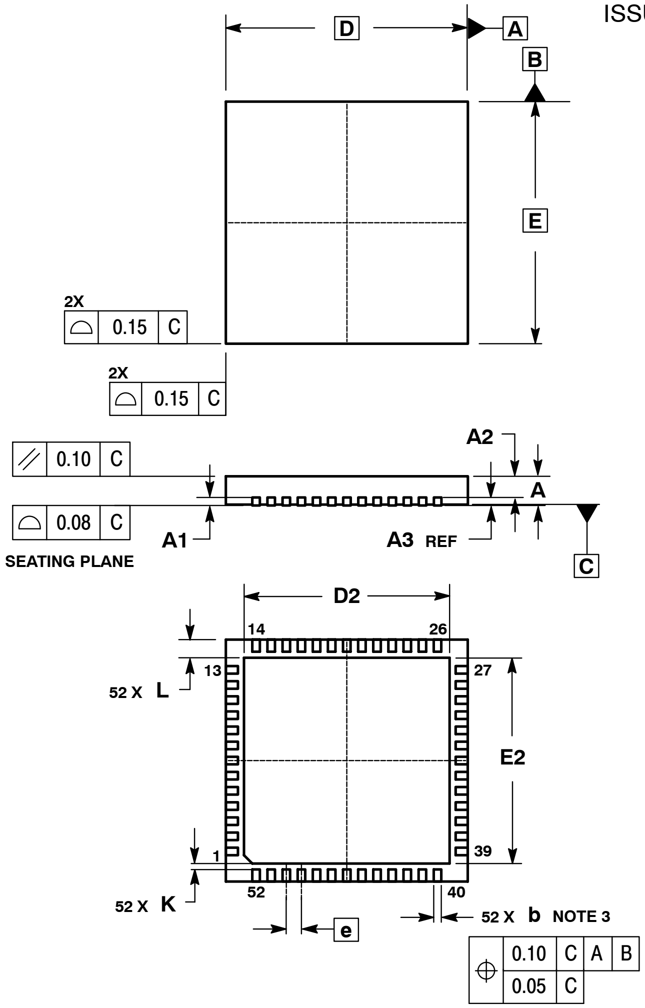
QFN24, 4x4
CASE 485L−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.23	0.28
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.35	0.45

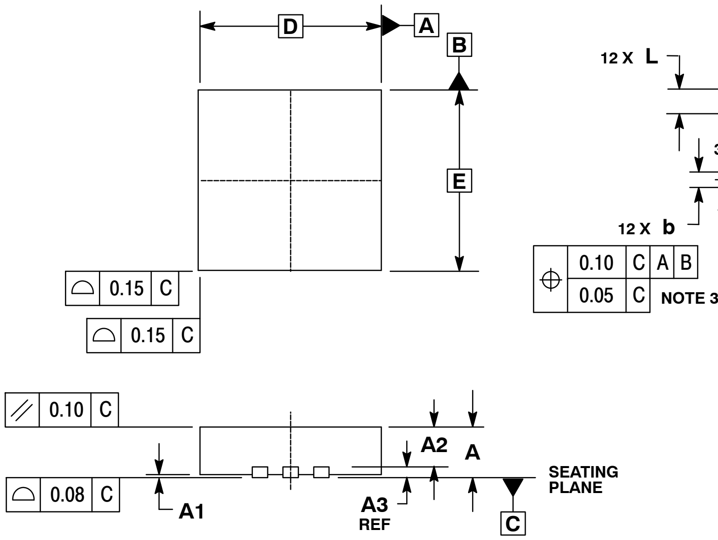
QFN52, 8x8
CASE 485M−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

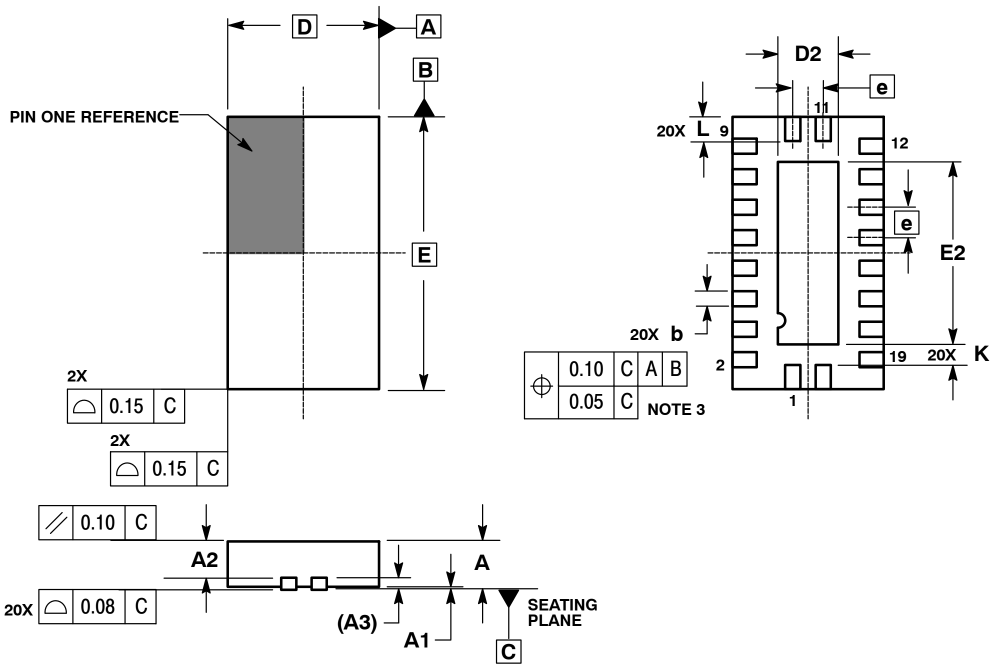
QFN12, 3x3
CASE 485N−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.50	1.80
E	3.00 BSC	
E2	1.50	1.80
e	0.50 BSC	
K	0.20	---
L	0.35	0.45

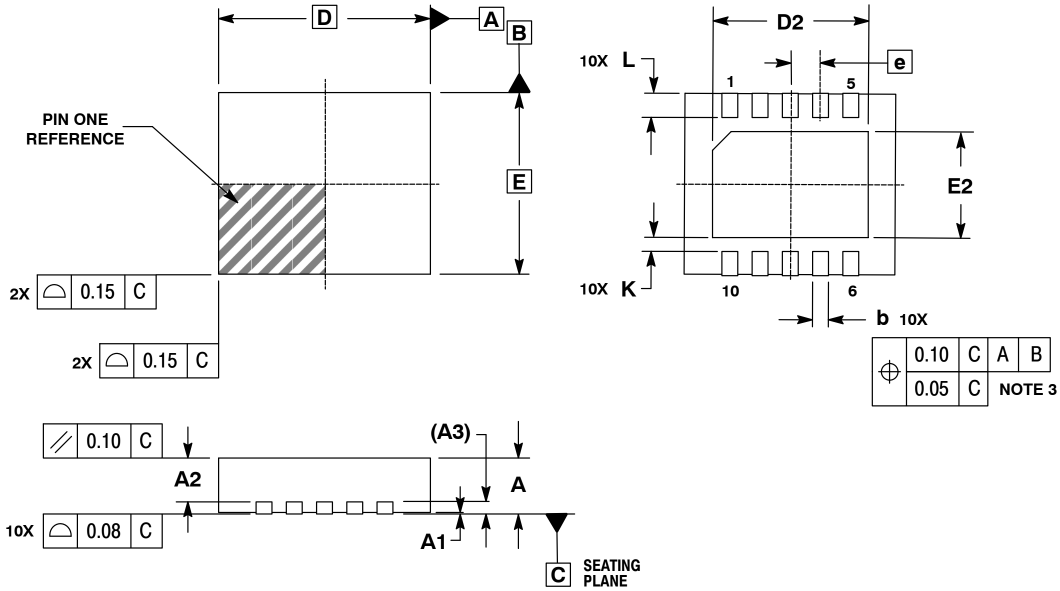
QFN20, 2.5x4.5
CASE 485AA−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	4.50 BSC	
E2	2.85	3.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45

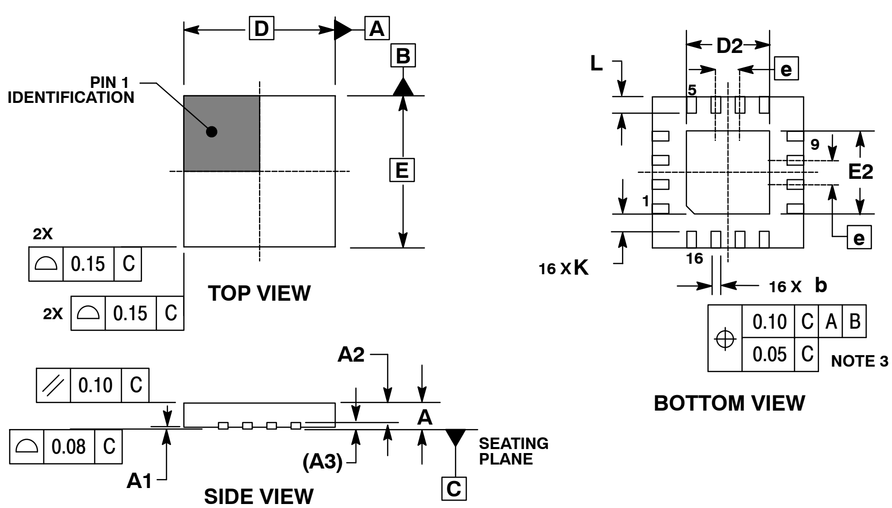
DFN10, 3.5x3
CASE 485AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	3.50 BSC	
D2	2.50	2.80
E	3.00 BSC	
E2	1.55	1.85
e	0.50 BSC	
K	0.20	---
L	0.35	0.45

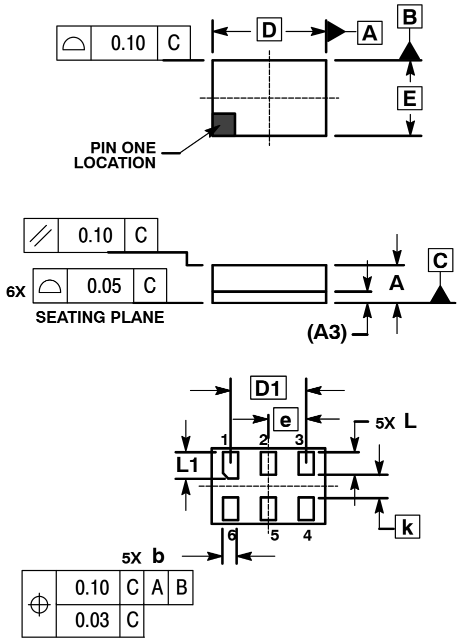
QFN16, 5x5
CASE 485AC−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.25	0.35
D	5.00 BSC	
D2	2.55	2.85
E	5.00 BSC	
E2	2.55	2.85
e	0.80 BSC	
K	0.20	−−−
L	0.35	0.75

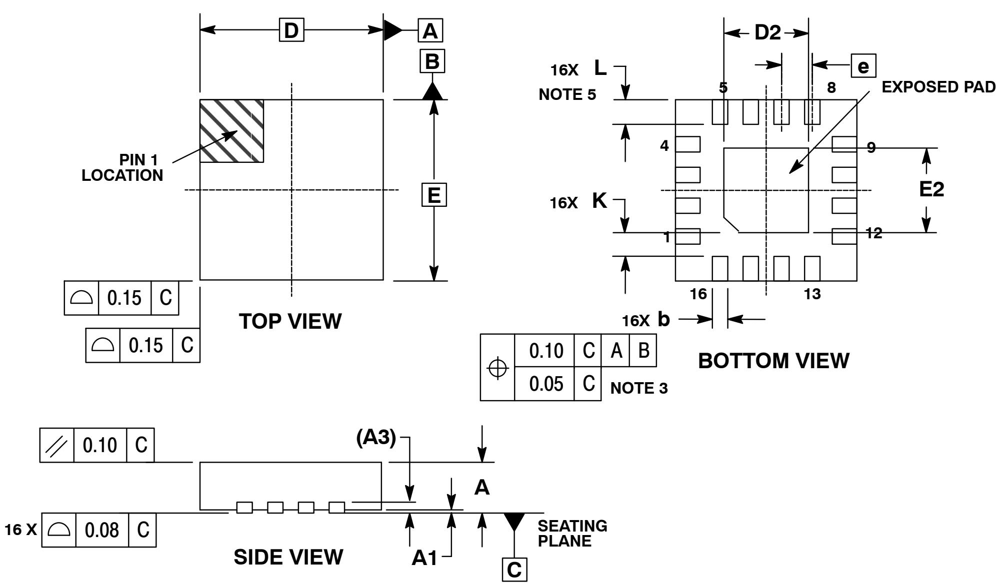
6−PIN, BT QFN
CASE 485AD−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.450	0.550
A3	0.150 BSC	
D	1.500 BSC	
D1	1.000 BSC	
E	1.000 BSC	
b	0.150	0.250
e	0.500 BSC	
L	0.250	0.350
L1	0.300	0.400
k	0.300 BSC	

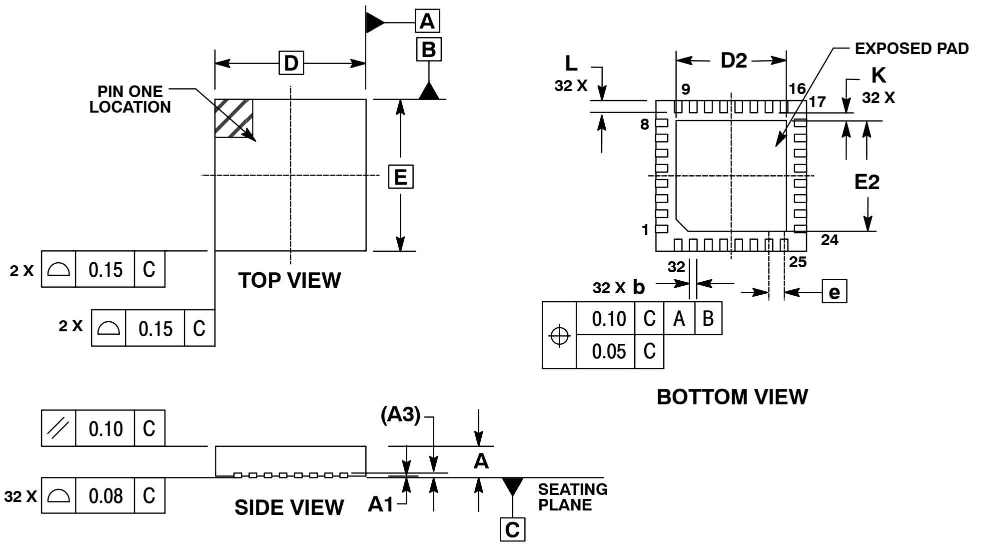
QFN16, 3x3
CASE 485AE−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OUTLINE MEETS JEDEC DIMENSIONS PER MO−220, VARIATION VEED−6.

DIM	MILLIMETERS MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		3.00 BSC	
D2	1.250	1.40	1.550
E		3.00 BSC	
E2	1.250	1.40	1.550
e		0.500 BSC	
K	0.200	−−−	−−−
L	0.300	0.400	0.500

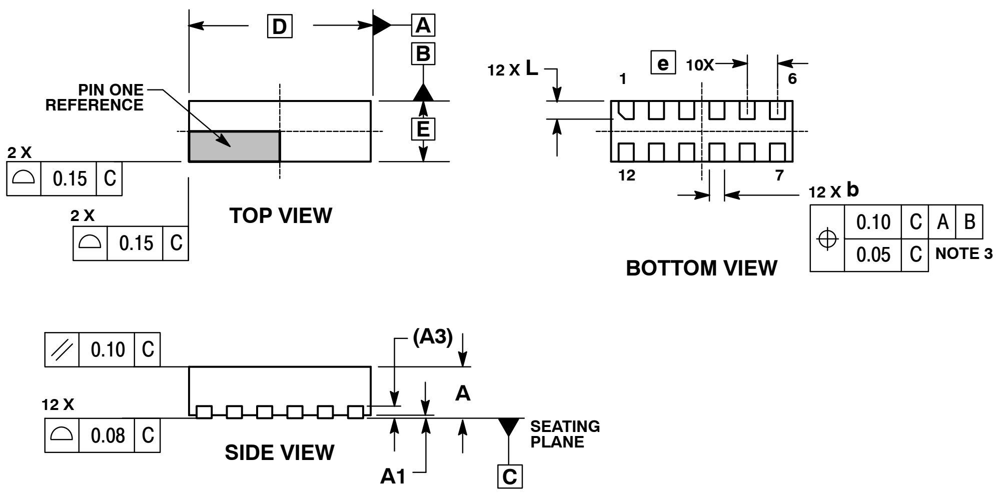
QFN32, 5x5
CASE 485AF−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	3.500	3.650	3.800
E	5.00 BSC		
E2	3.500	3.650	3.800
e	0.500 BSC		
K	0.200	−−−	−−−
L	0.300	0.400	0.500

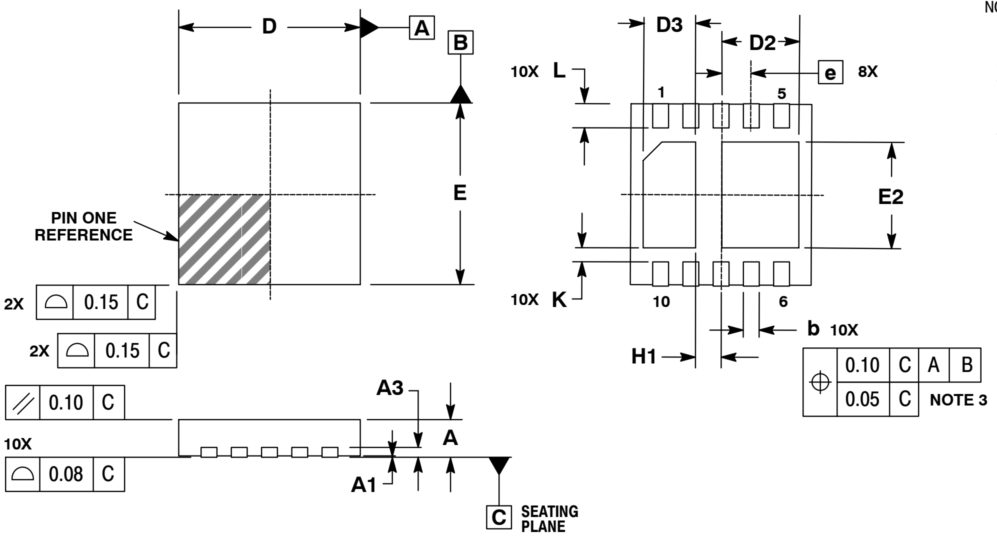
WDFN12, 3x1
CASE 485AG−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.20	0.40

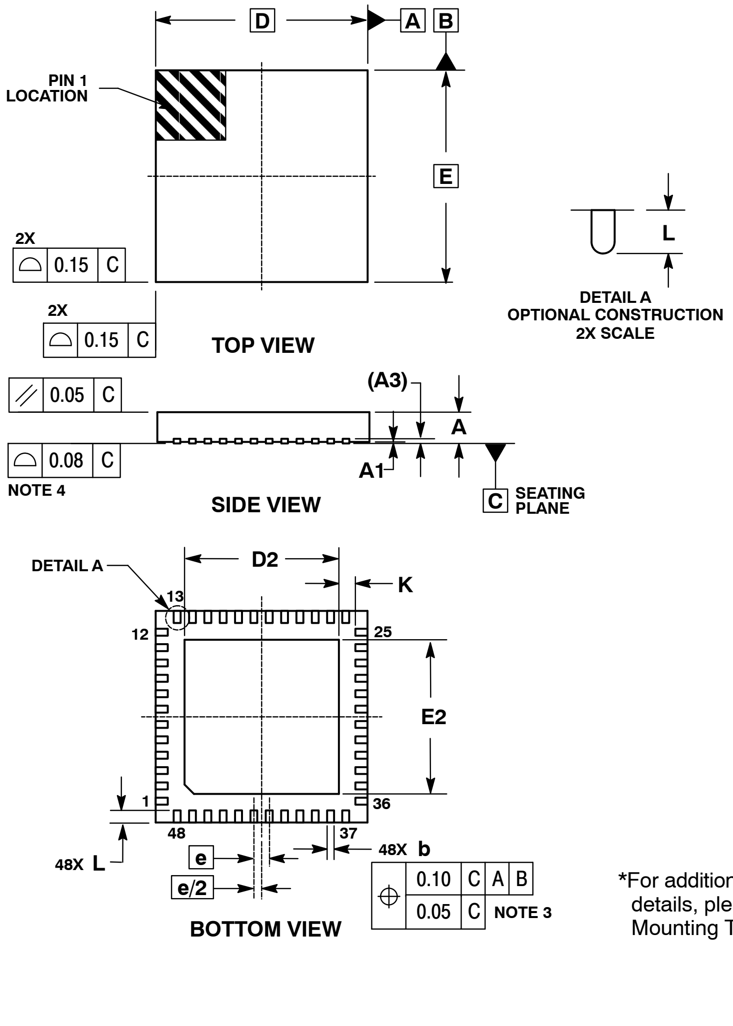
DFN10, 3x3
CASE 485AH−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	3.00 BSC		
D2	1.10	1.20	1.30
D3	0.65	0.75	0.85
E	3.00 BSC		
E2	1.50	1.60	1.70
e	0.50 BSC		
K	0.21	---	---
L	0.30	0.40	0.50
H1	0.45 REF		

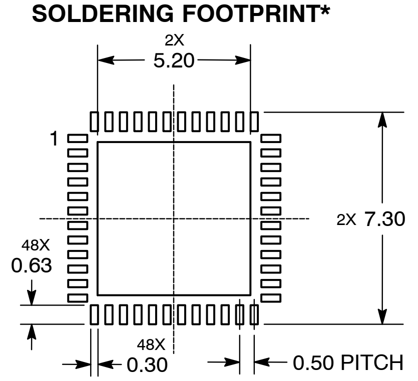
QFN48, 7x7, 0.5P
CASE 485AJ−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	7.00 BSC	
D2	5.00	5.20
E	7.00 BSC	
E2	5.00	5.20
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

SOLDERING FOOTPRINT*

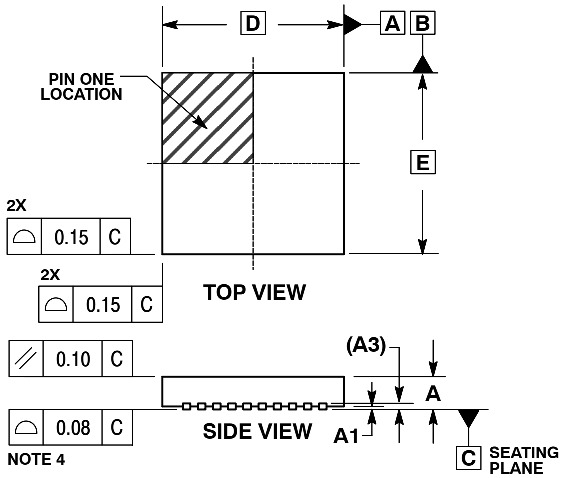


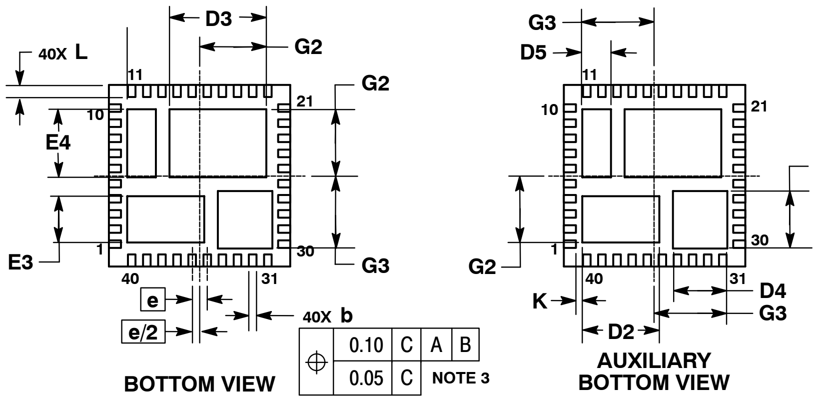
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

QFN40, 6x6, 0.5P

CASE 485AK−01
ISSUE A

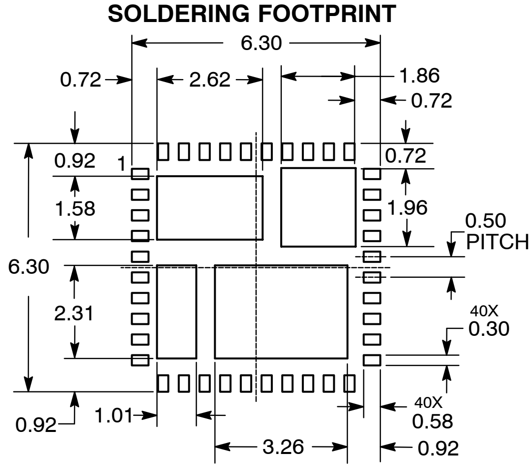




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

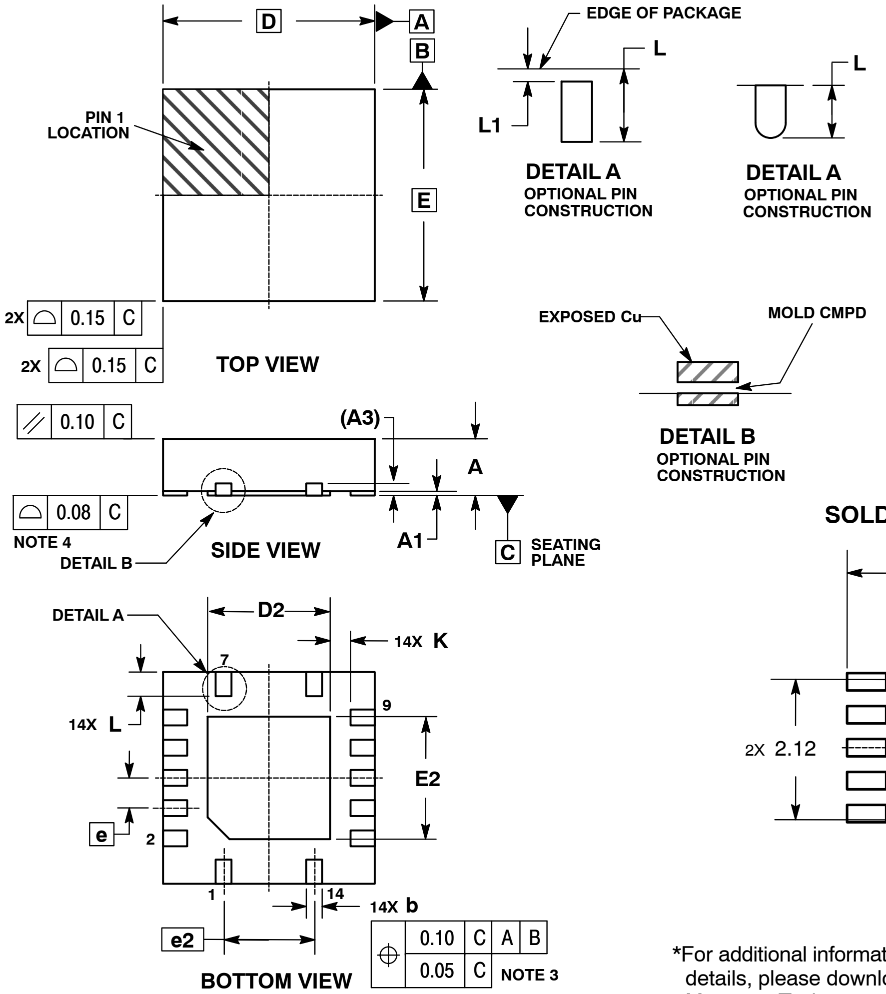
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.45	2.65
D3	3.10	3.30
D4	1.70	1.90
D5	0.85	1.05
E	6.00 BSC	
E2	1.80	2.00
E3	1.43	1.63
E4	2.15	2.35
e	0.50 BSC	
G2	2.10	2.30
G3	2.30	2.50
K	0.20	---
L	0.30	0.50

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

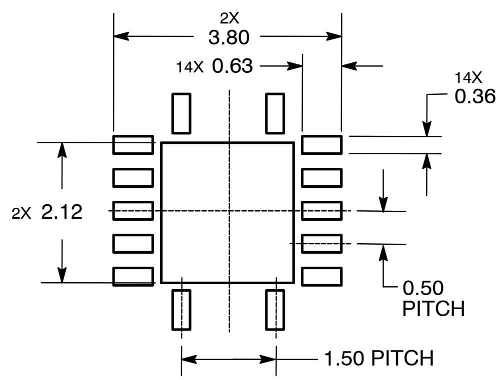
QFN14, 3.5x3.5, 0.5P
CASE 485AL−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.50 BSC	
D2	1.90	2.15
E	3.50 BSC	
E2	1.90	2.15
e	0.50 BSC	
e2	1.50 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.03

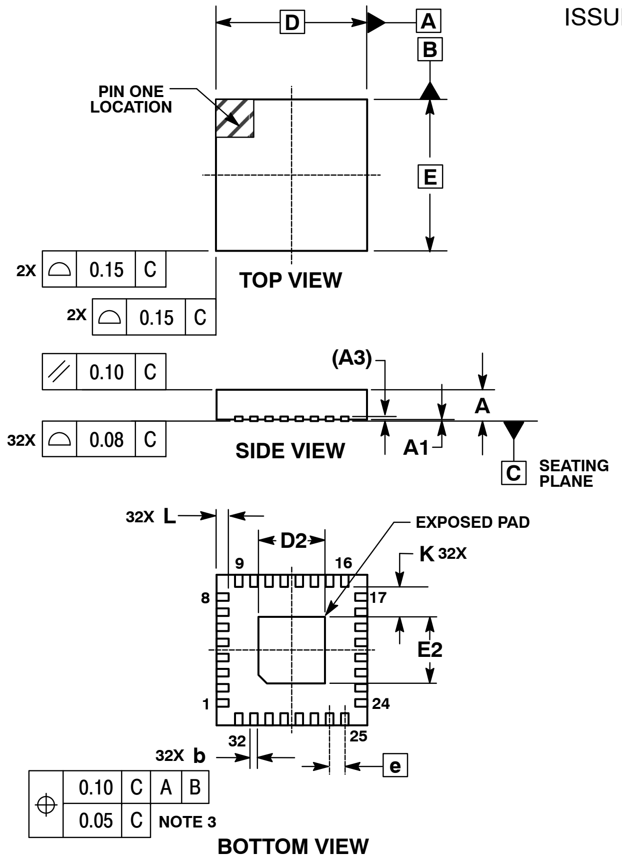
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

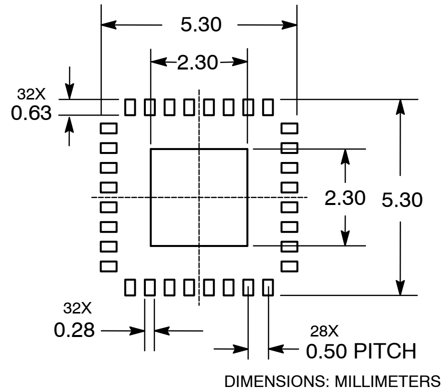
QFN32, 5x5, 0.5P
CASE 485AM−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

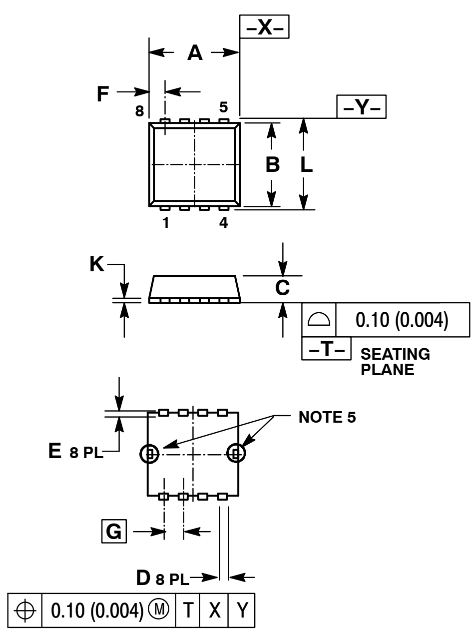
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.100	2.200	2.300
E	5.00 BSC		
E2	2.100	2.200	2.300
e	0.500 BSC		
K	1.000 REF		
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

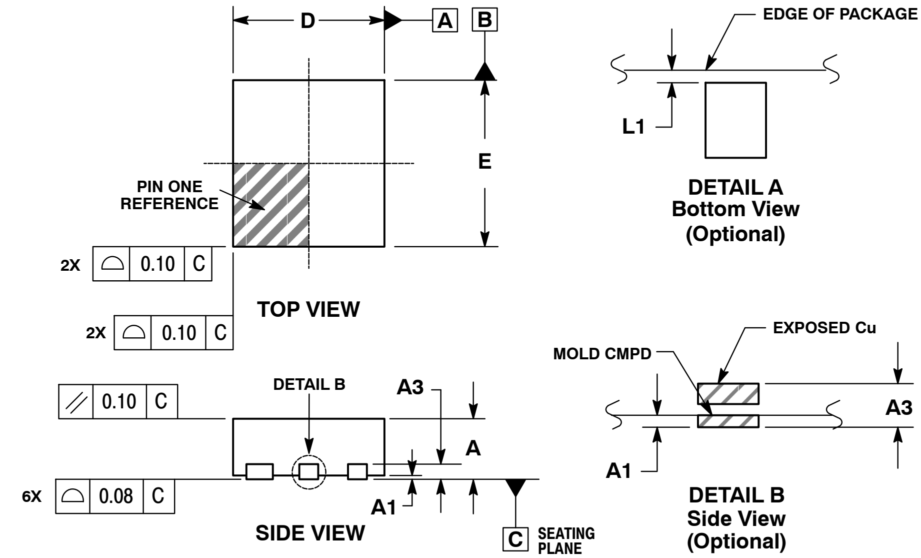
SON−8
CASE 486−01
ISSUE O

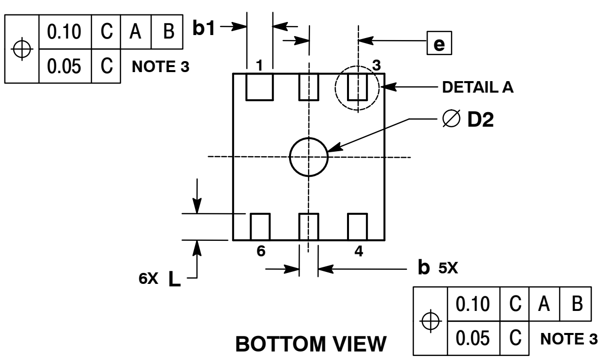


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TAB SUSPENSION LEADS HAVE V_{no} VOLTAGE LEVEL. (THEY ARE CONNECTED TO THE REVERSE SIDE OF THIS IC). DO NOT CONNECT TO OTHER WIRES OR LAND PATTERNS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.70	3.10	0.106	0.122
B	2.60	3.00	0.102	0.118
C	---	0.90	---	0.035
D	0.20	0.40	0.008	0.016
E	0.20 REF		0.008 REF	
F	0.48 TYP		0.019 TYP	
G	0.65 TYP		0.026 TYP	
K	0.08	0.18	0.003	0.007
L	2.80	3.20	0.110	0.126

DFN6, 2x2.2
SC70−LLS
CASE 488−03
ISSUE G

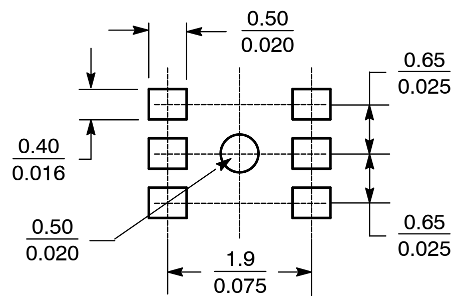




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE AND SIDE EDGE OF PACKAGE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
b1	0.30	0.35	0.40
D	2.00 BSC		
D2	0.40	0.50	0.60
E	2.20 BSC		
e	0.65 BSC		
L	0.30	0.35	0.40
L1	0.00	0.05	0.10

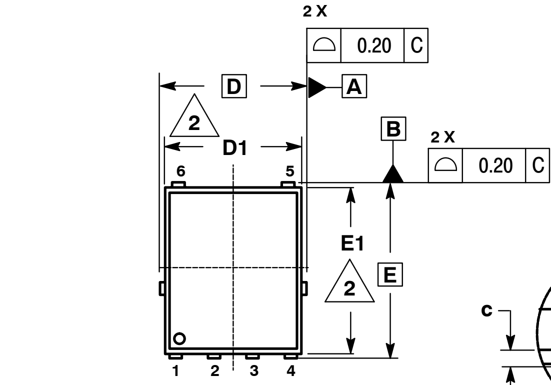
SOLDERING FOOTPRINT*



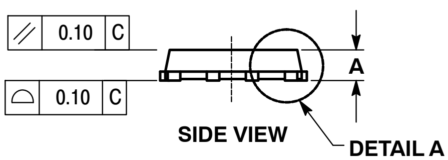
SCALE 10:1

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

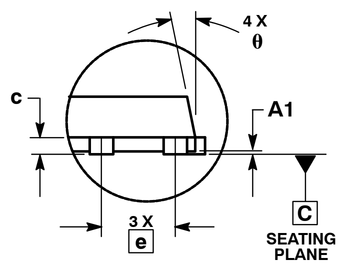
DFN6, 5x6
SO−8 FL
CASE 488AA−01
ISSUE C



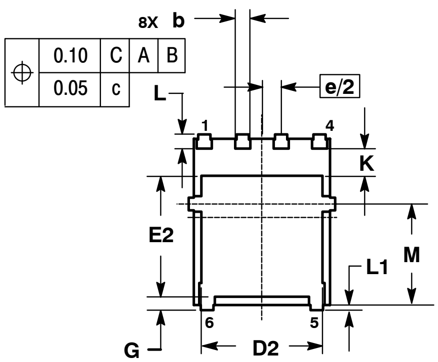
TOP VIEW



SIDE VIEW



DETAIL A



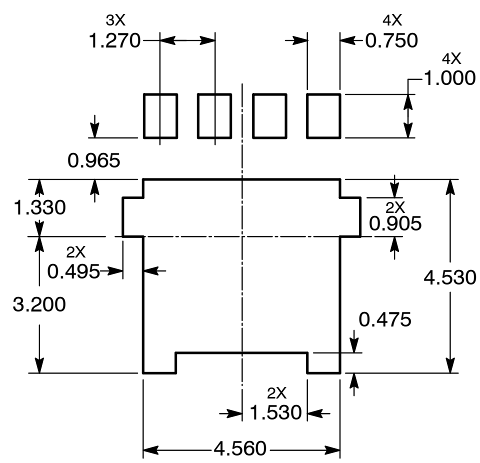
BOTTOM VIEW

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

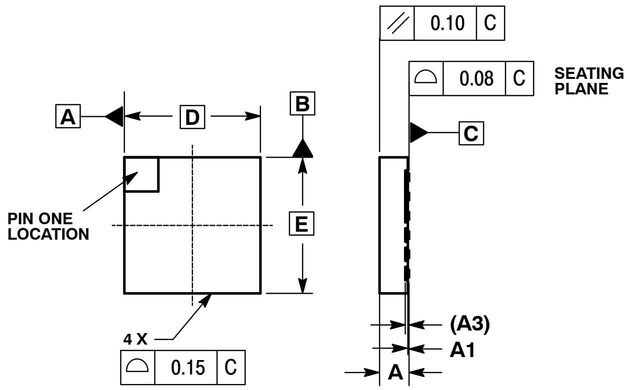
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.50	4.90	5.10
D2	3.50	−−−	4.22
E		6.15 BSC	
E1	5.50	5.80	6.10
E2	3.45	−−−	4.30
e		1.27 BSC	
G	0.51	0.61	0.71
K	0.51	−−−	−−−
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	−−−	12 °

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

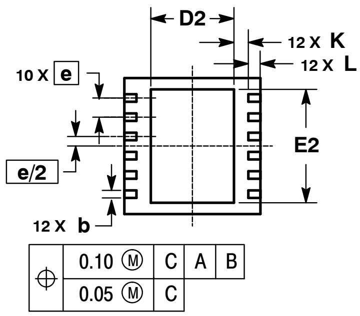
PLLP−12
CASE 488AB−01
ISSUE C



TOP VIEW　　SIDE VIEW

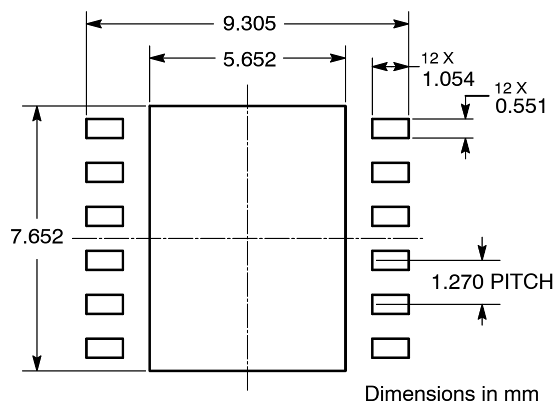
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE LEAD, DIMENSION B, AND EXPOSED PAD.

DIM	MILLIMETERS MIN	MAX
A	1.750	1.950
A1	0.000	0.050
A3	0.254 REF	
b	0.400	0.600
D	9.000 BSC	
E	9.000 BSC	
e	1.270 BSC	
D2	5.400	5.600
E2	7.400	7.600
K	0.850 REF	
L	0.850	0.950



BOTTOM VIEW

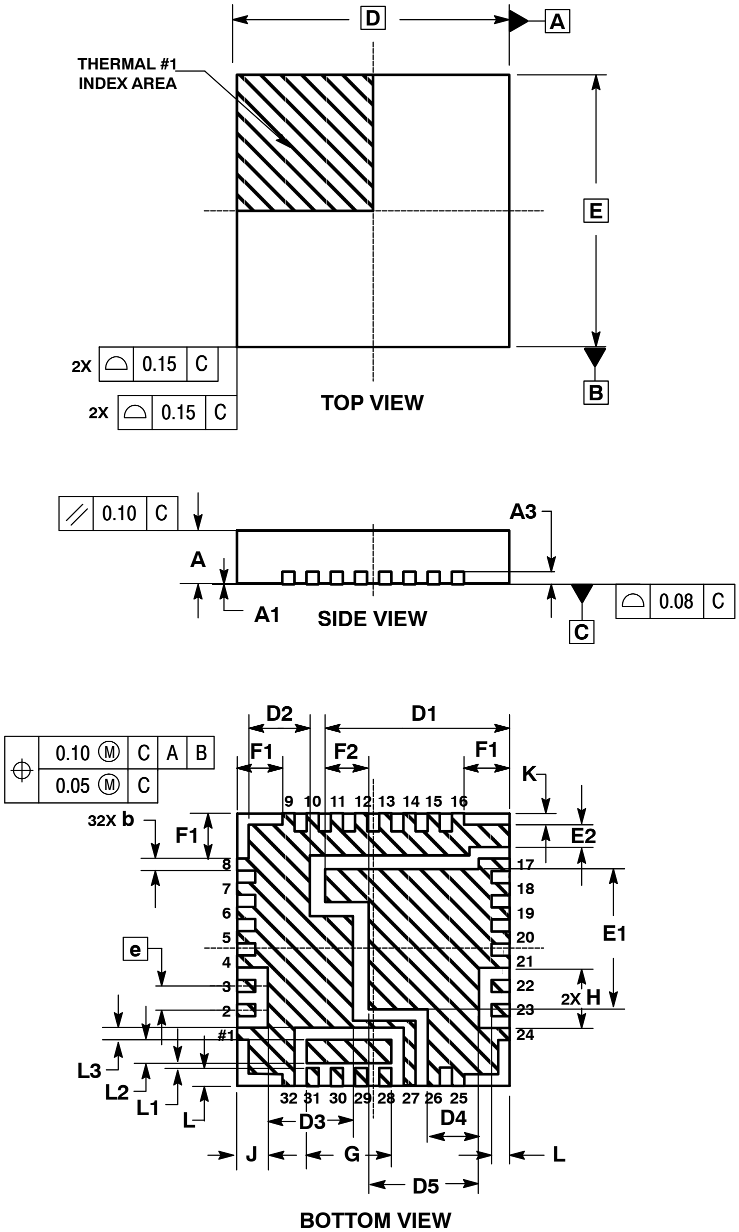
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:
PIN 1. OVLO
2. UVLO
3. ENABLE/TIMER
4. GND
5. CCHARGE
6. CURRENT LIMIT
7. POWER GOOD
8. N/C
9. N/C
10. SOURCE
11. SOURCE
12. SOURCE

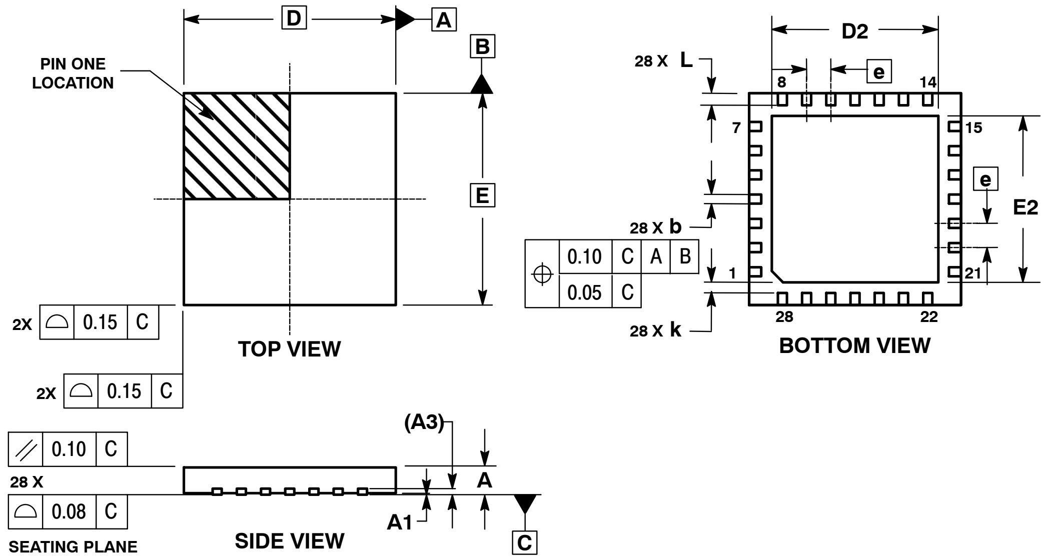
PLLP−32
CASE 488AC−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 40 MM FROM TERMINAL TIP
4. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THEIR TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.750	1.850	1.950
A1	0.000	−−−−	0.050
A3	0.254 REF		
b	0.350	0.400	0.450
D	9.000 BSC		
D1	5.987	6.087	6.187
D2	1.924	2.024	2.124
D3	2.713	2.813	2.913
D4	1.584	1.684	1.784
D5	3.547	3.647	3.747
E	9.000 BSC		
E1	4.472	4.572	4.672
E2	0.638	0.738	0.838
e	0.800 BSC		
F1	1.500 REF		
F2	1.324	1.424	1.524
G	2.700	2.800	2.900
H	2.000 REF		
J	1.016 BSC		
K	0.381 REF		
L	0.500	0.600	0.700
L1	0.062	0.162	0.262
L2	0.760	0.770	0.870
L3	0.281	0.381	0.481

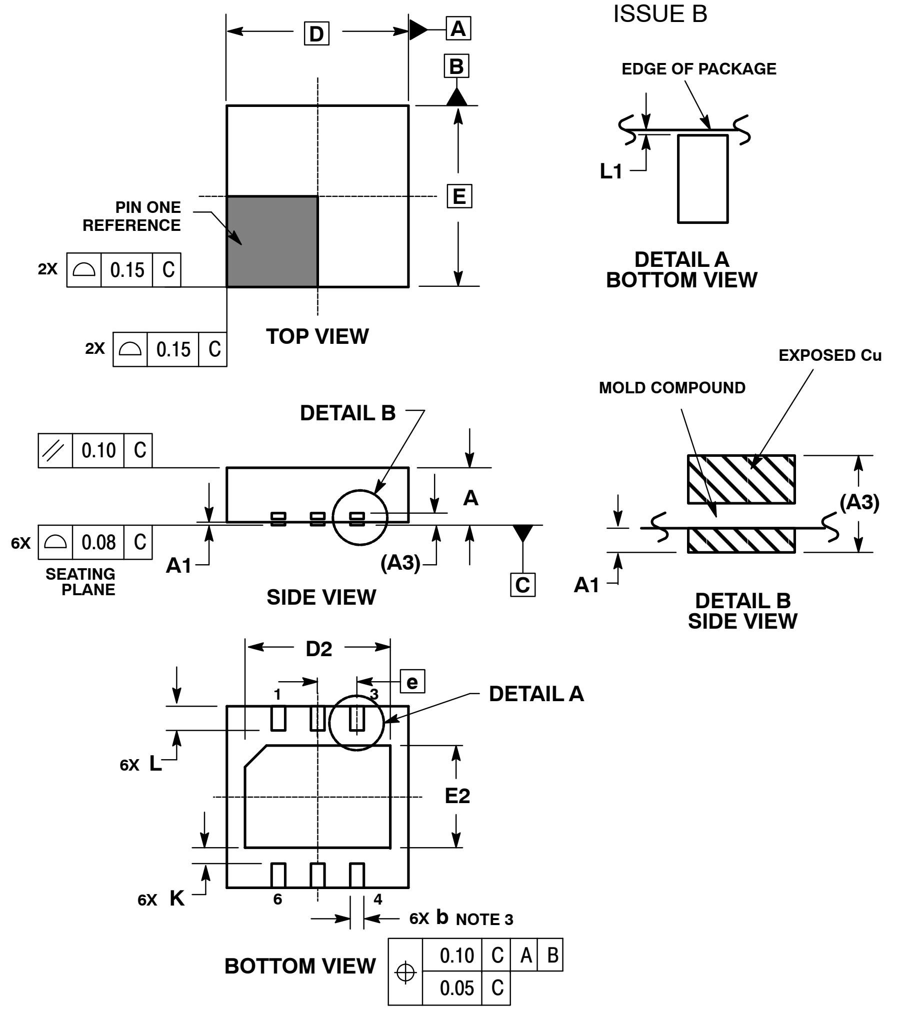
QFN28, 7x7
CASE 488AD−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MESURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	7.00 BSC	
D2	5.40	5.60
E	7.00 BSC	
E2	5.40	5.60
e	0.80 BSC	
L	0.30	0.50
k	0.20	−−−−

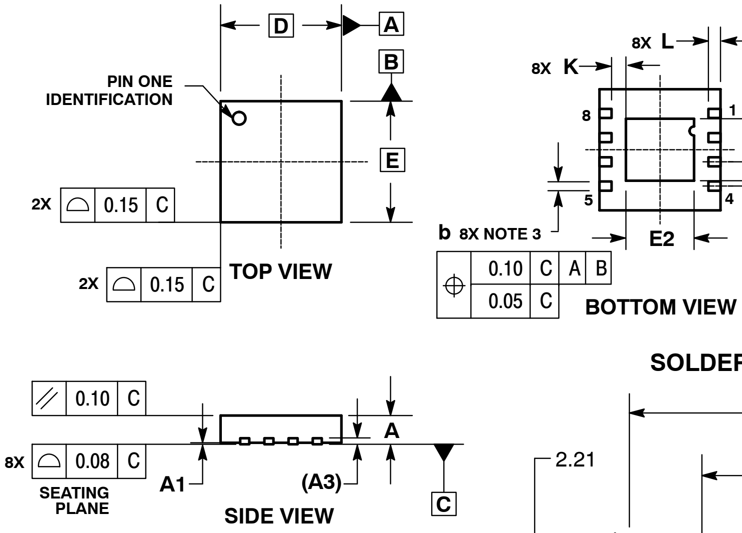
DFN6, 3x3
CASE 488AE−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	0.25
b	0.18	0.30
D	3.00 BSC	
D2	2.25	2.55
E	3.00 BSC	
E2	1.55	1.85
e	0.65 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.021

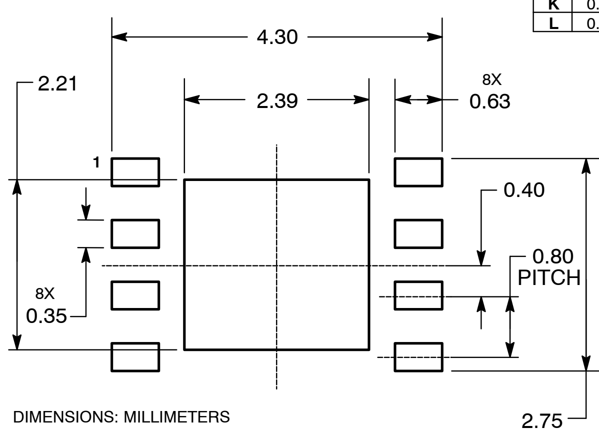
DFN8, 4x4
CASE 488AF−01
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	−−−
L	0.30	0.50

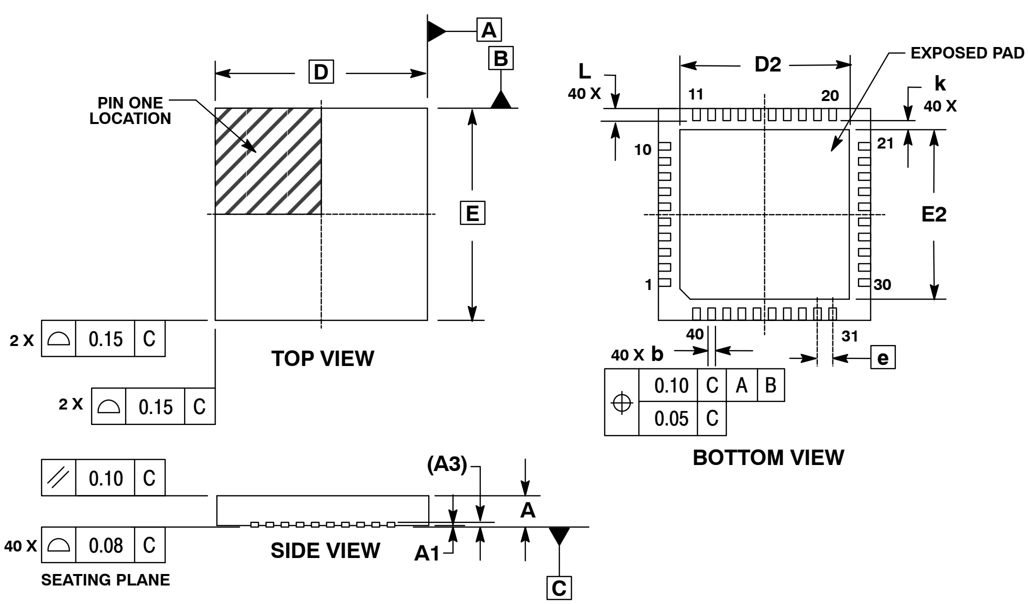
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

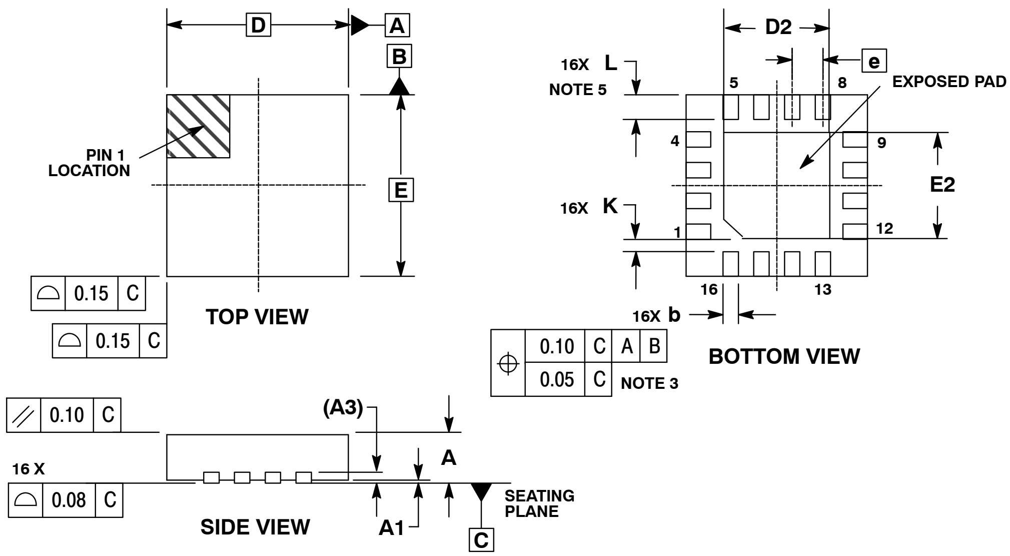
QFN40, 7x7
CASE 488AG−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETER.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	7.00 BSC	
D2	5.50	5.70
E	7.00 BSC	
E2	5.50	5.70
e	0.50 BSC	
L	0.30	0.50
k	0.20	−−−

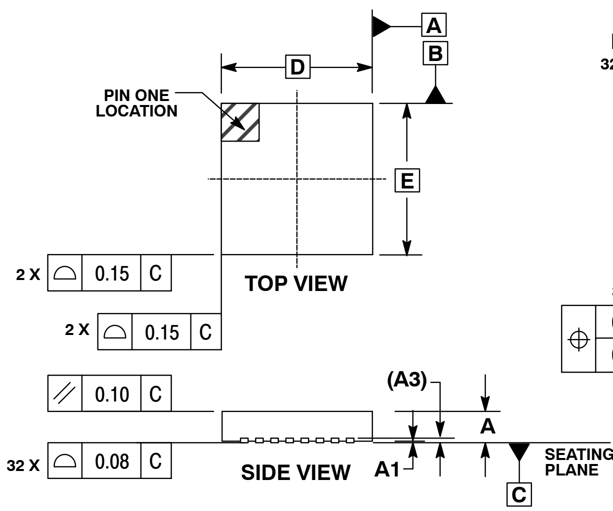
QFN16, 3x3
CASE 488AK−01
ISSUE O

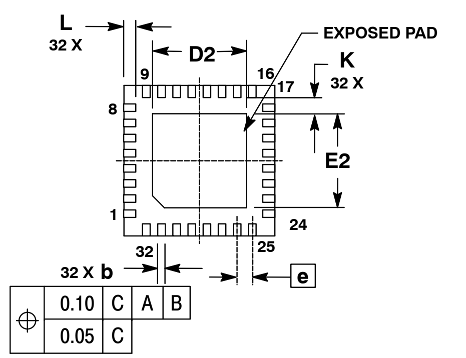


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

QFN32, 5x5
CASE 488AM−01
ISSUE O



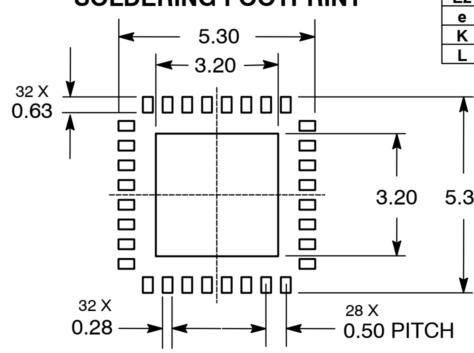


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

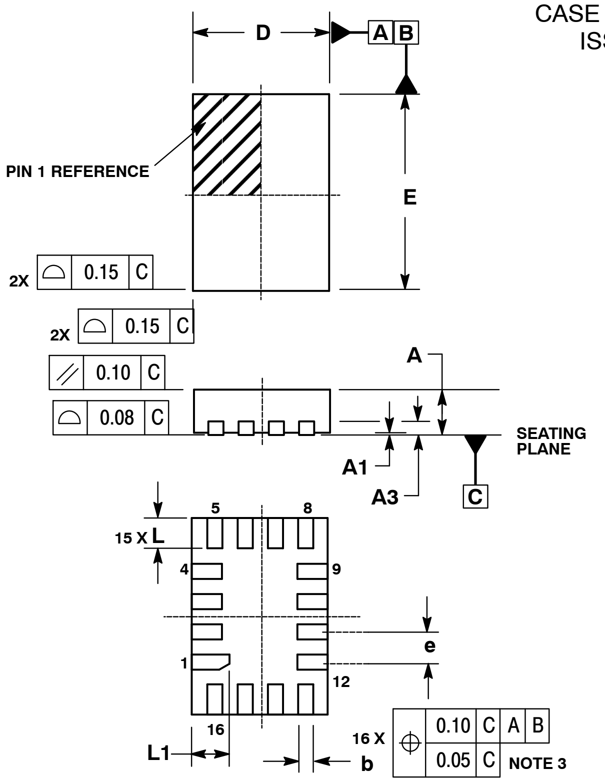
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3	0.200 REF		
b	0.180	0.250	0.300
D	5.00 BSC		
D2	2.950	3.100	3.250
E	5.00 BSC		
E2	2.950	3.100	3.250
e	0.500 BSC		
K	0.200	−−−	−−−
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

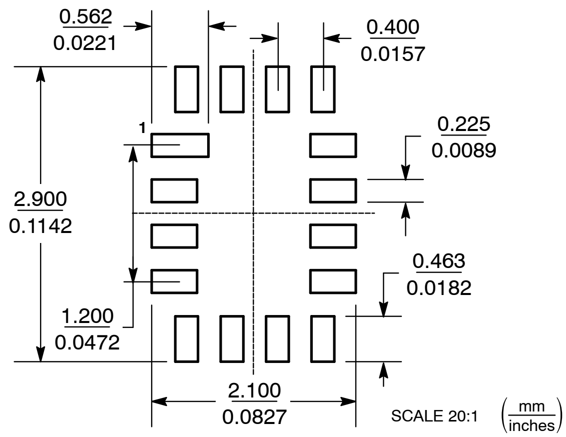
WQFN16, 1.8x2.6
CASE 488AP−01
ISSUE A



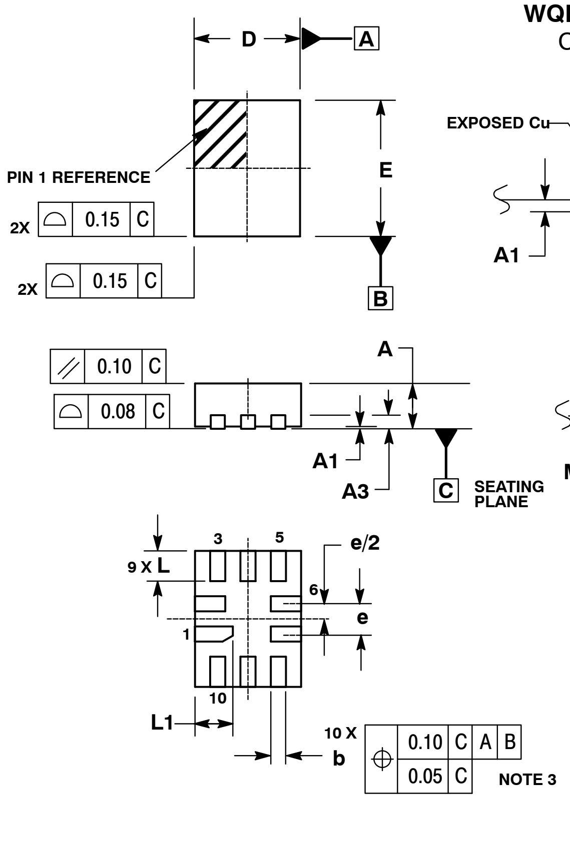
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

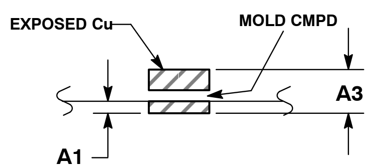
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.40	0.60

MOUNTING FOOTPRINT

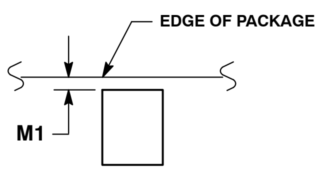


WQFN10, 1.4x1.8, 0.4P
CASE 488AQ−01
ISSUE C





DETAIL B
Side View
(Optional)

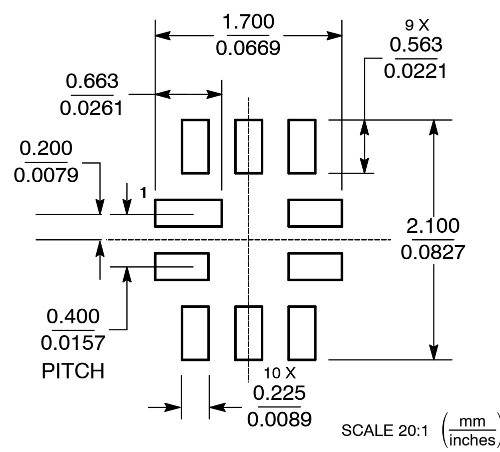


DETAIL A
Bottom View
(Optional)

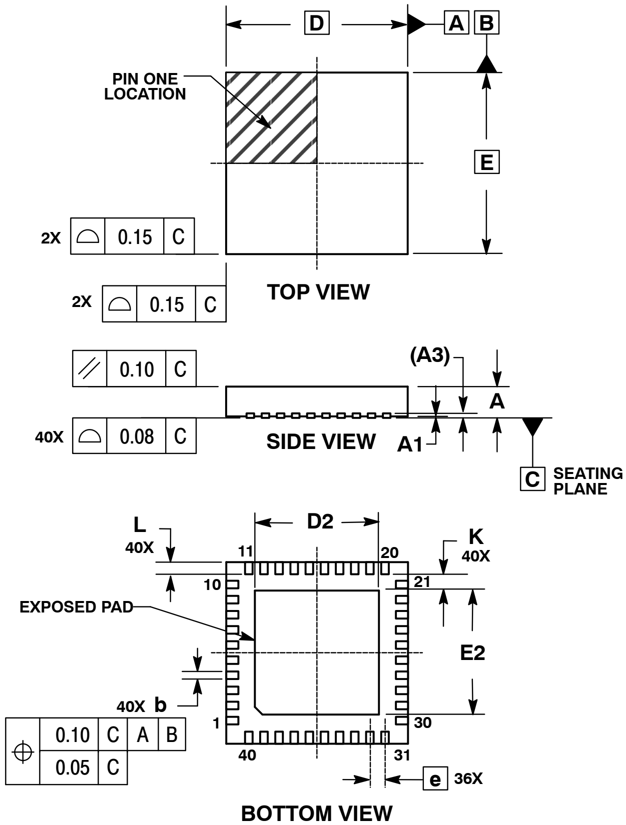
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.40	0.60
M1	0.00	0.05

MOUNTING FOOTPRINT



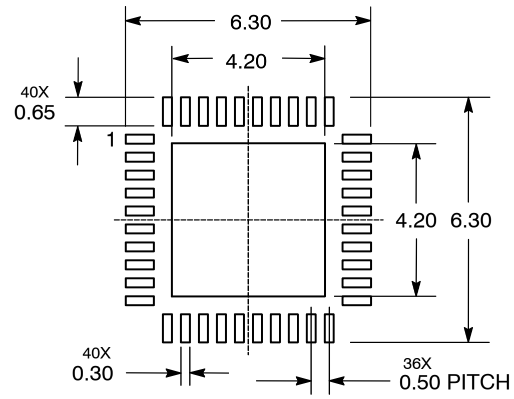
QFN40, 6x6, 0.5P
CASE 488AR−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	4.00	4.20
E	6.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
K	0.20	−−−

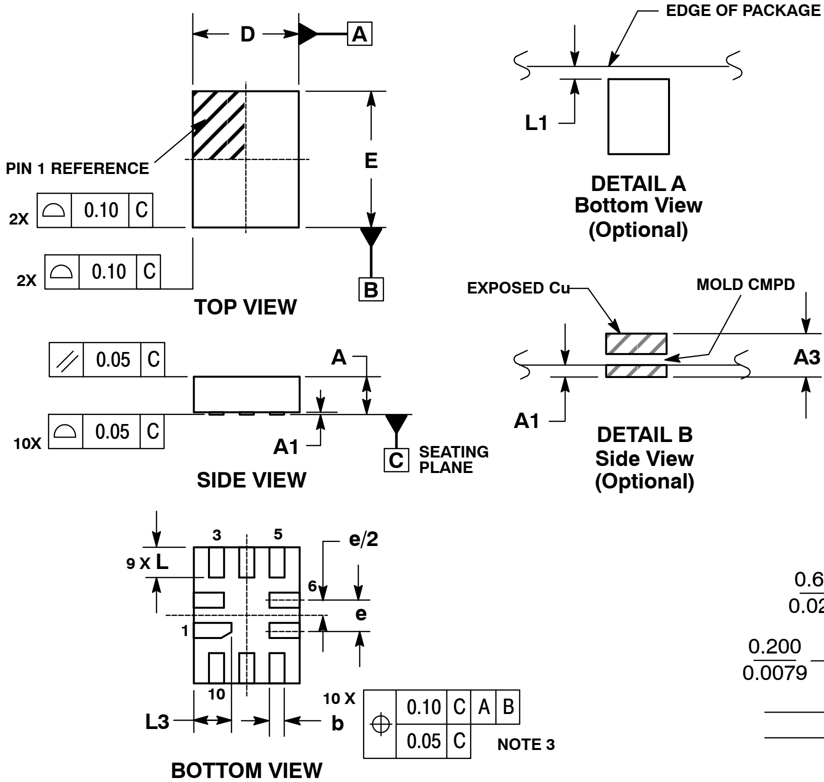
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

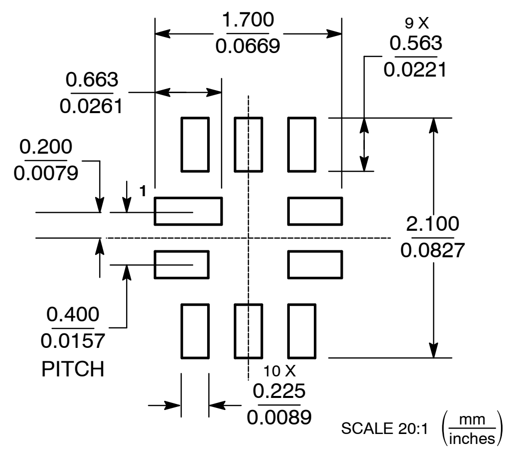
UQFN10, 1.4x1.8, 0.4P
CASE 488AT−01
ISSUE A



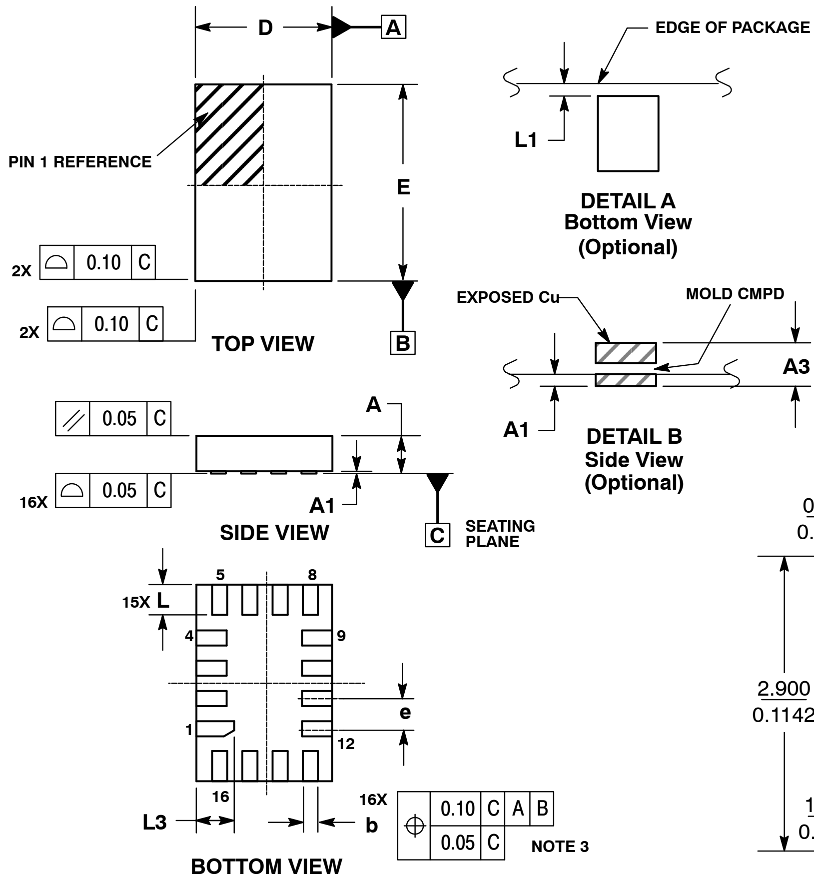
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

MOUNTING FOOTPRINT



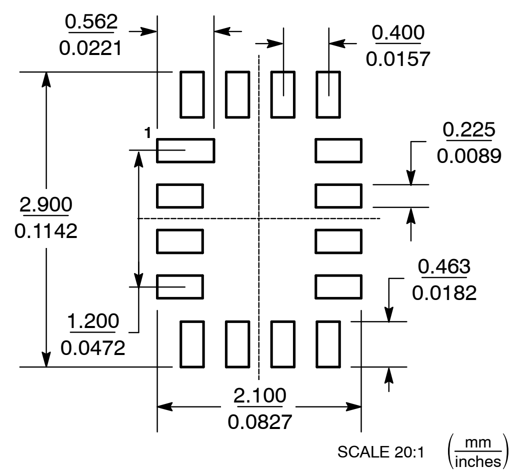
UQFN16, 1.8x2.6, 0.4P
CASE 488AU−01
ISSUE A



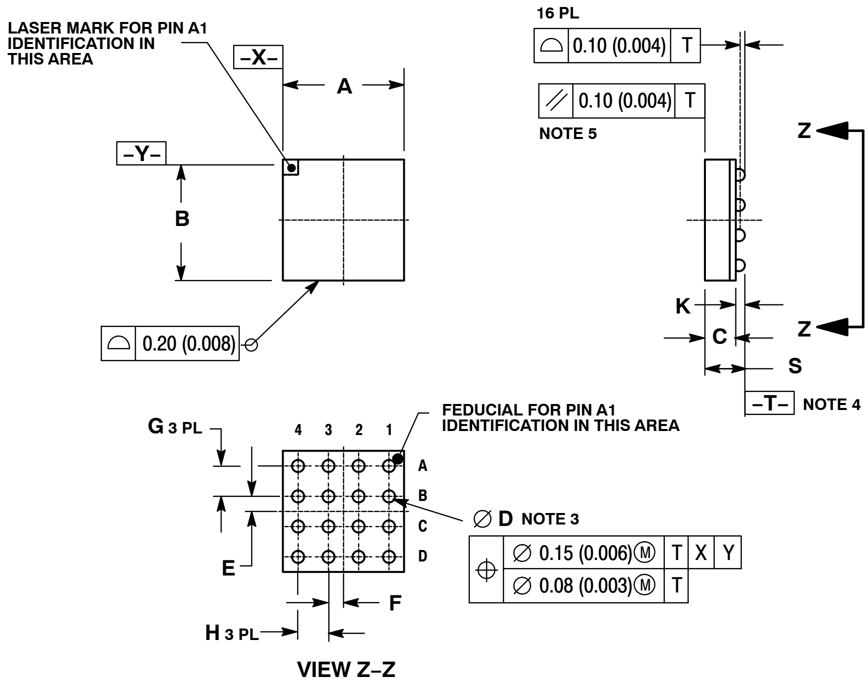
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.80 BSC	
E	2.60 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

MOUNTING FOOTPRINT



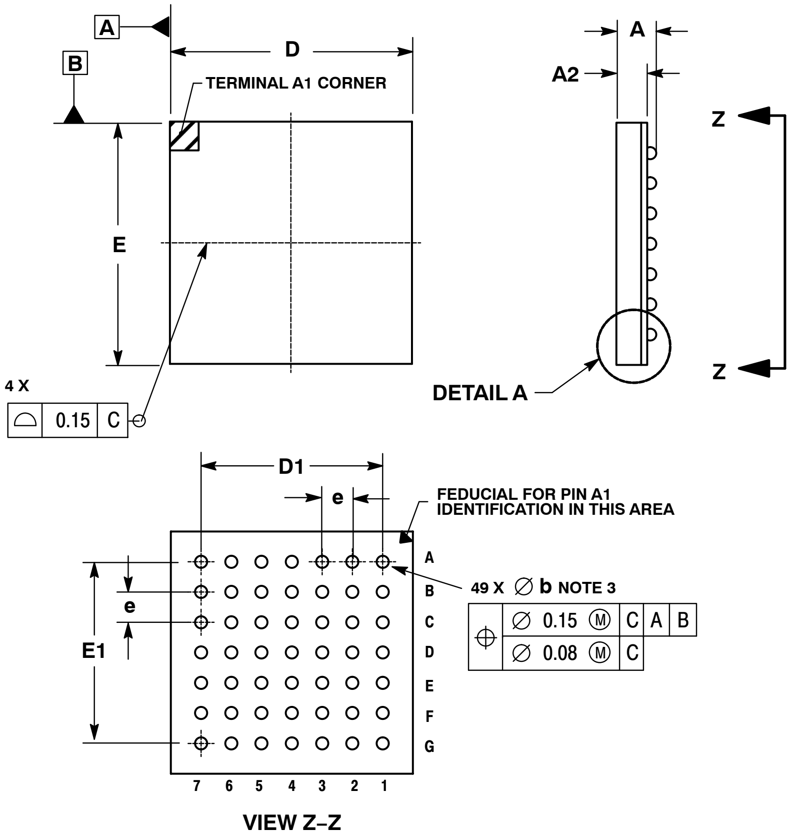
16−PIN FLIP−CHIP BGA
CASE 489−01
ISSUE O



NOTES:
1. DIMENSIONIN AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE −T−.
4. DATUM −T− (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

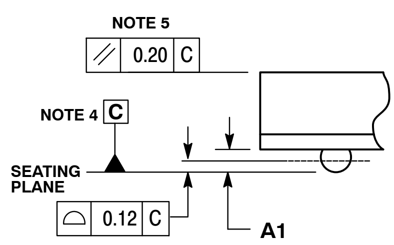
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.00 BSC		0.157 BSC	
B	4.00 BSC		0.157 BSC	
C	1.02 REF		0.040 REF	
D	∅ 0.30	∅ 0.50	∅ 0.012	∅ 0.020
E	0.50 BSC		0.020 BSC	
F	0.50 BSC		0.020 BSC	
G	1.00 BSC		0.039 BSC	
H	1.00 BSC		0.039 BSC	
K	0.25	0.35	0.010	0.014
S	1.40 MAX		0.055 MAX	

49−PIN FLIP−CHIP BGA
CASE 489A−02
ISSUE A



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
4. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 489A−01 OBSOLETE, NEW STANDARD 489A−02.

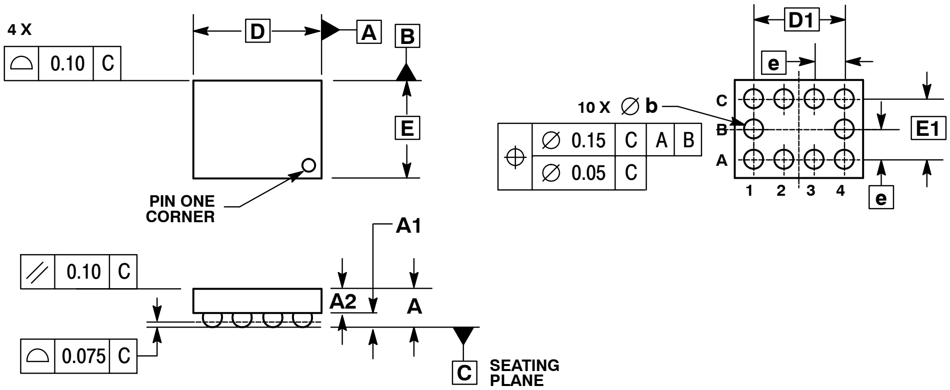
	MILLIMETERS	
DIM	MIN	MAX
A	---	1.40
A1	0.3	0.5
A2	0.91 REF	
b	0.40	0.60
D	8.00 BSC	
D1	6.00 BSC	
E	8.00 BSC	
E1	6.00 BSC	
e	1.00 BSC	



DETAIL A
(ROTATED 90° C.W.)

10−PIN FLIP−CHIP

CASE 489AA−01
ISSUE A

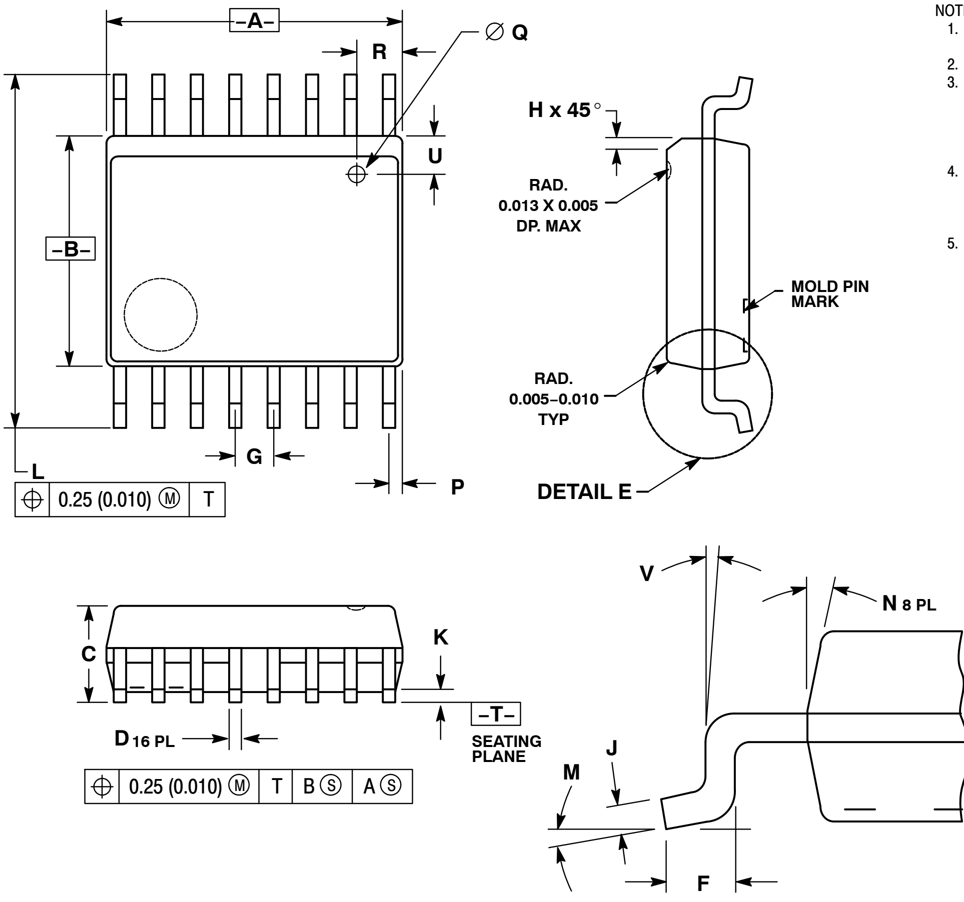


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.650
A1	0.210	0.270
A2	0.280	0.380
D	1.965 BSC	
E	1.465 BSC	
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

QSOP−16

CASE 492−01
ISSUE O

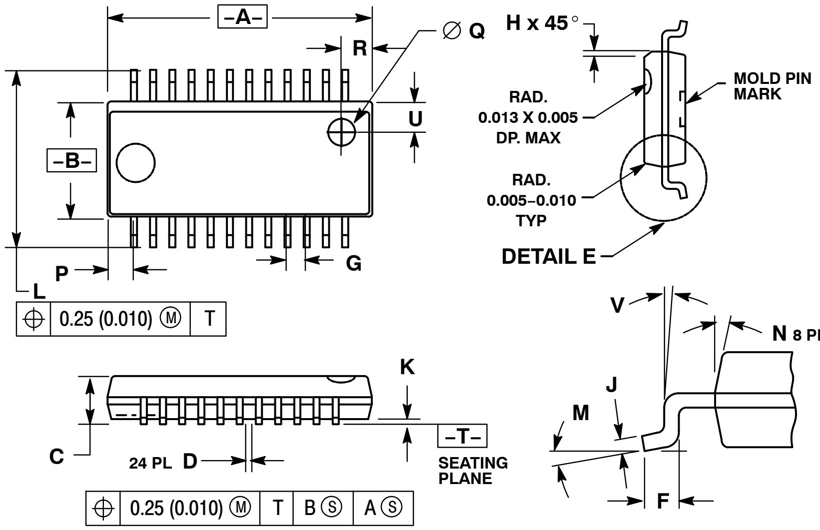


DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.189	0.196	4.80	4.98
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.007	0.011	0.18	0.28
Q	0.020 DIA		0.51 DIA	
R	0.025	0.035	0.64	0.89
U	0.025	0.035	0.64	0.89
V	0°	8°	0°	8°

QSOP−24
CASE 492B−01
ISSUE O

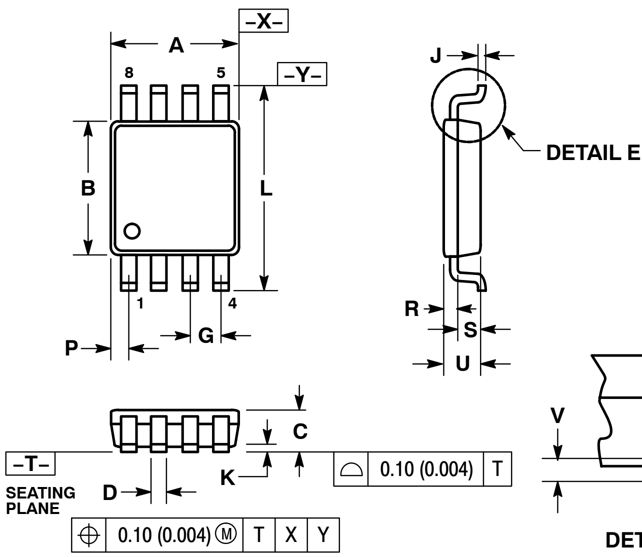


DETAIL E

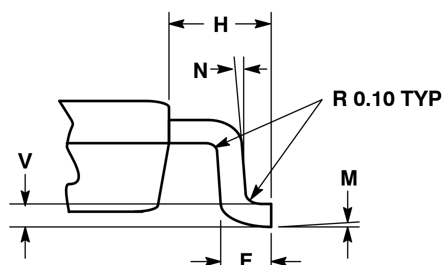
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
4. PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
5. BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

	INCHES		MILLIMETERS	
DIM	MAX	MIN	MAX	MIN
A	0.337	0.344	8.56	8.74
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.027	0.037	0.69	0.94
Q	0.035 DIA		0.89 DIA	
R	0.035	0.045	0.89	1.14
U	0.035	0.045	0.89	1.14
V	0°	8°	0°	8°

US8
CASE 493−02
ISSUE B



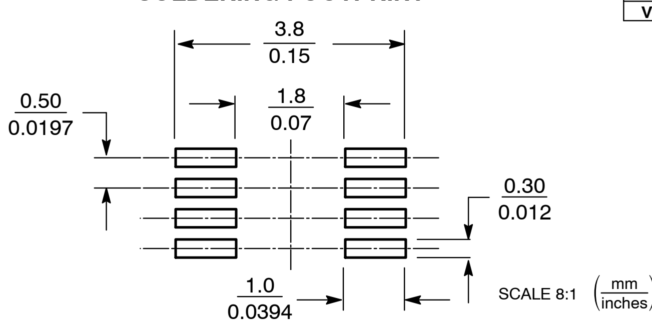
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055”) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSION. INTER−LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055”) PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076−0.0203 MM. (300−800 “).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 “).



DETAIL E

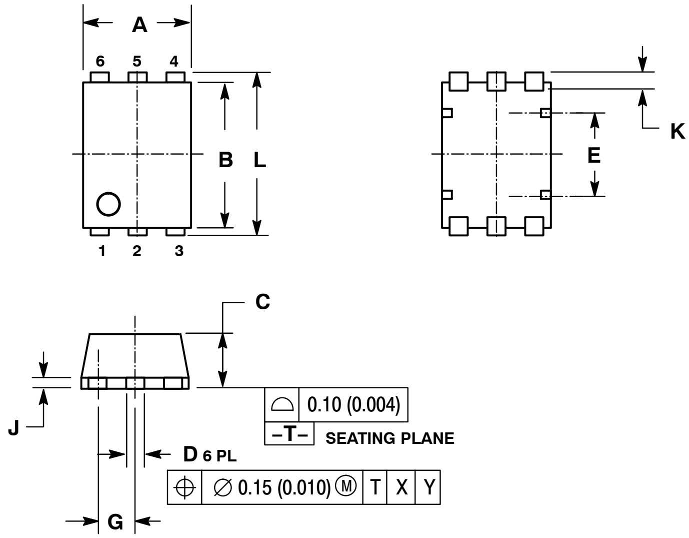
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0°	6°	0°	6°
N	5°	10°	5°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

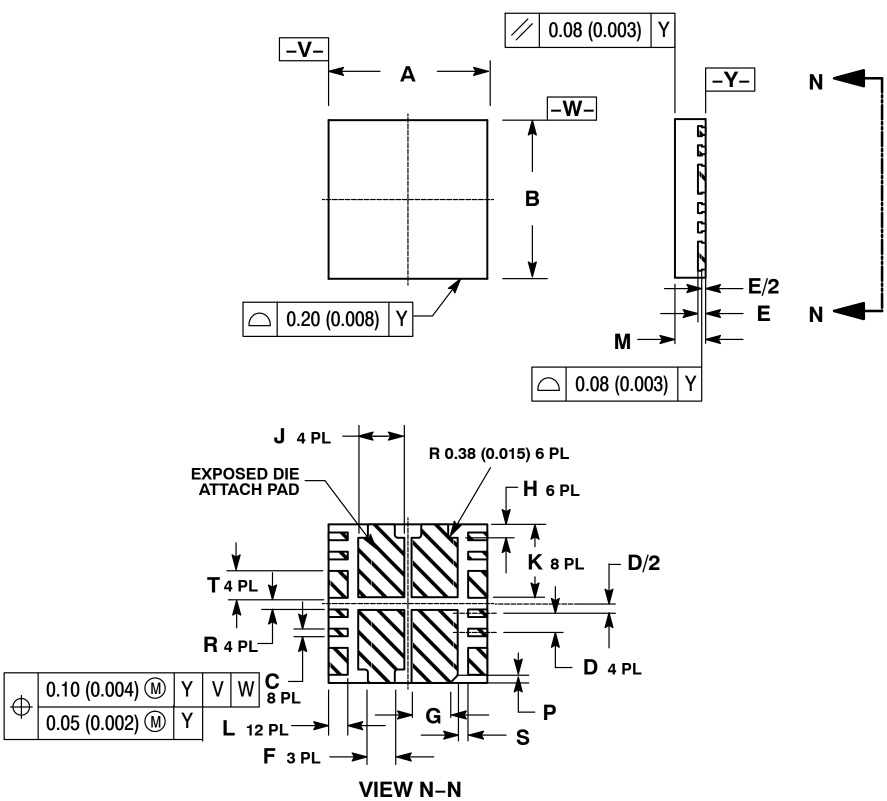
SON−6
CASE 494−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.40	1.80	0.055	0.071
B	2.40	2.80	0.094	0.110
C	---	0.90	---	0.035
D	0.10	0.30	0.004	0.012
E	1.24	1.44	0.049	0.057
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.30 BSC		0.012 BSC	
L	2.85	3.15	0.112	0.124

QFN FBIP
CASE 495−01
ISSUE A



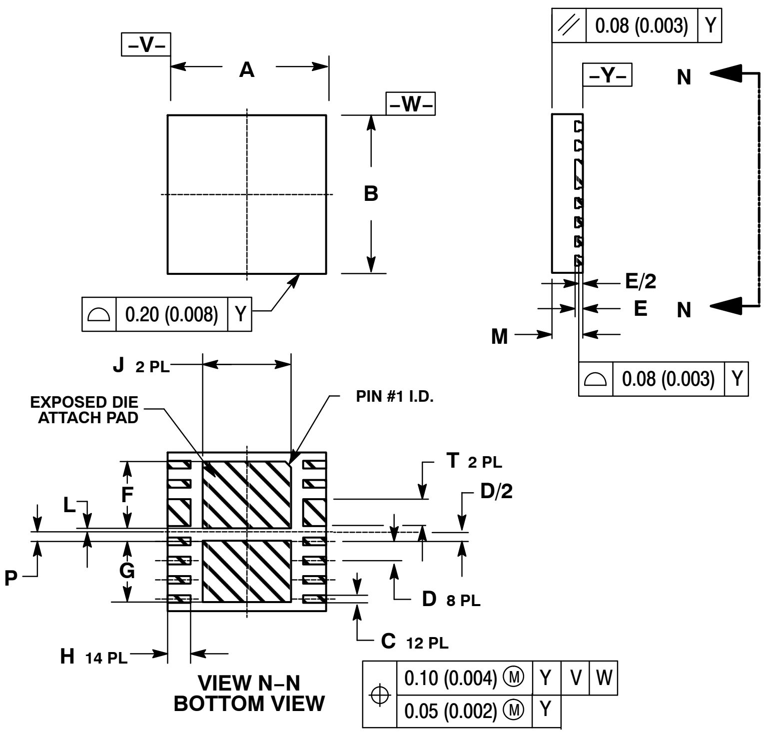
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO LEAD. DIE ATTACHED PAD.
4. OPTIONAL FEATURES ARE FOR REFERENCE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.40	10.60	0.409	0.417
B	10.40	10.60	0.409	0.417
C	0.40	0.50	0.016	0.020
D	1.27 BSC		0.050 BSC	
E	0.50	0.52	0.020	0.020
F	1.70	1.90	0.067	0.075
G	2.45	2.55	0.096	0.100
H	0.80	1.00	0.031	0.039
J	2.90	3.10	0.114	0.122
K	4.75	4.95	0.187	0.195
L	1.10	1.30	0.043	0.051
M	2.00	2.20	0.079	0.087
P	0.30	0.50	0.012	0.020
R	0.70	0.90	0.028	0.035
S	0.58	0.78	0.023	0.031
T	1.68	1.78	0.066	0.070

QFN14, 10.5x10.5

CASE 495A−01

ISSUE O



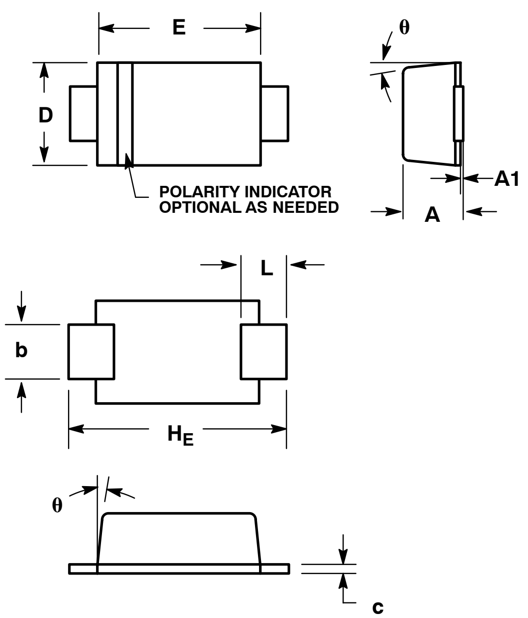
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO LEAD. DIE ATTACHED PAD.
4. OPTIONAL FEATURES ARE FOR REFERENCE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.50 BSC		0.413 BSC	
B	10.50 BSC		0.413 BSC	
C	0.407	0.507	0.0160	0.0200
D	1.27 BSC		0.050 BSC	
E	0.50	0.52	0.020	0.020
F	4.319	4.519	0.1700	0.1780
G	4.015	4.215	0.1580	0.1660
H	1.40	1.60	0.055	0.063
J	5.789	5.989	0.2280	0.2360
L	0.20	0.30	0.08	0.012
M	2.00	2.20	0.079	0.087
P	0.505	0.605	0.0200	0.0240
T	1.677	1.777	0.0660	0.0700

SOD−123FL

CASE 498−01

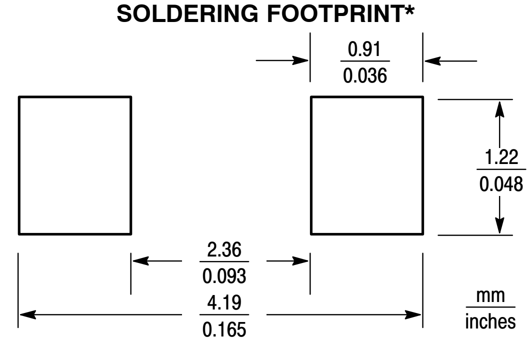
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH.
4. DIMENSIONS D AND J ARE TO BE MEASURED ON FLAT SECTION OF THE LEAD: BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.

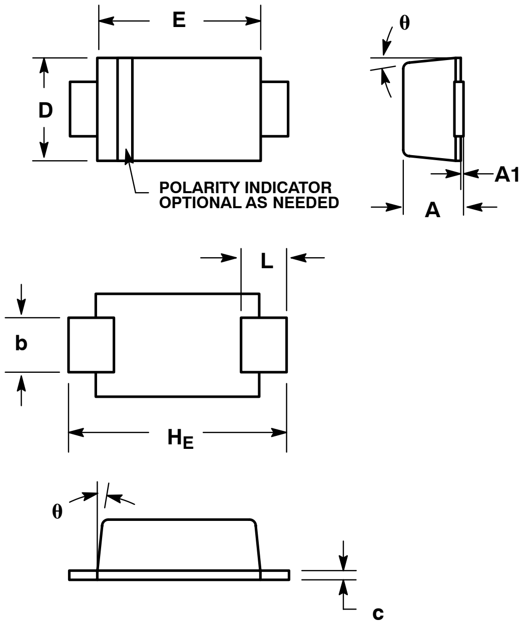
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	0.95	1.00	0.035	0.037	0.039
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.70	0.90	1.10	0.028	0.035	0.043
c	0.10	0.15	0.20	0.004	0.006	0.008
D	1.50	1.65	1.80	0.059	0.065	0.071
E	2.50	2.70	2.90	0.098	0.106	0.114
L	0.55	0.75	0.95	0.022	0.030	0.037
H_E	3.40	3.60	3.80	0.134	0.142	0.150
θ	0°	–	8°	0°	–	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

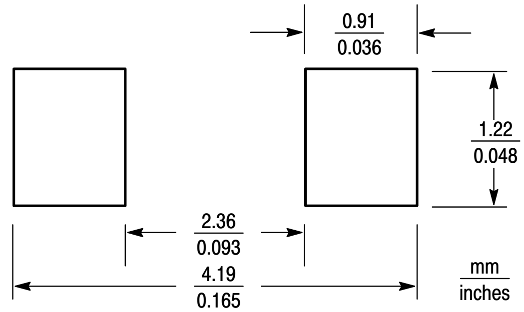
SOD−123F
CASE 498AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH.
4. DIMENSIONS D AND J ARE TO BE MEASURED ON FLAT SECTION OF THE LEAD: BETWEEN 0.10 AND 0.25 MM FROM THE LEAD TIP.

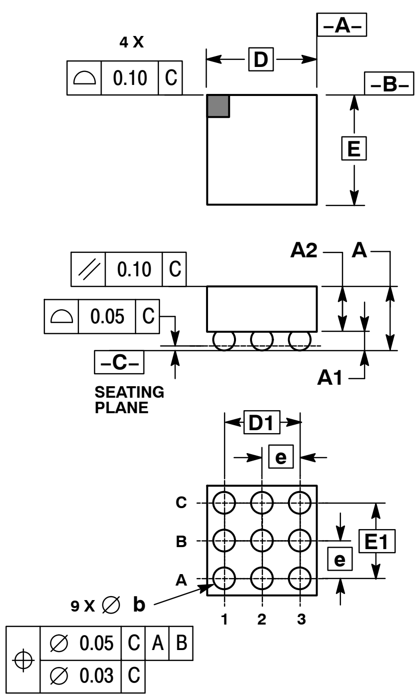
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.05	0.10	0.000	0.002	0.004
b	0.85	0.92	0.99	0.033	0.036	0.039
c	0.12	0.17	0.22	0.005	0.007	0.009
D	1.50	1.60	1.70	0.059	0.063	0.067
E	2.60	2.70	2.80	0.102	0.106	0.110
H_E	3.30	3.50	3.70	0.130	0.138	0.146
L	0.49	0.64	0.79	0.019	0.025	0.031
θ	4°	–	10°	4°	–	10°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

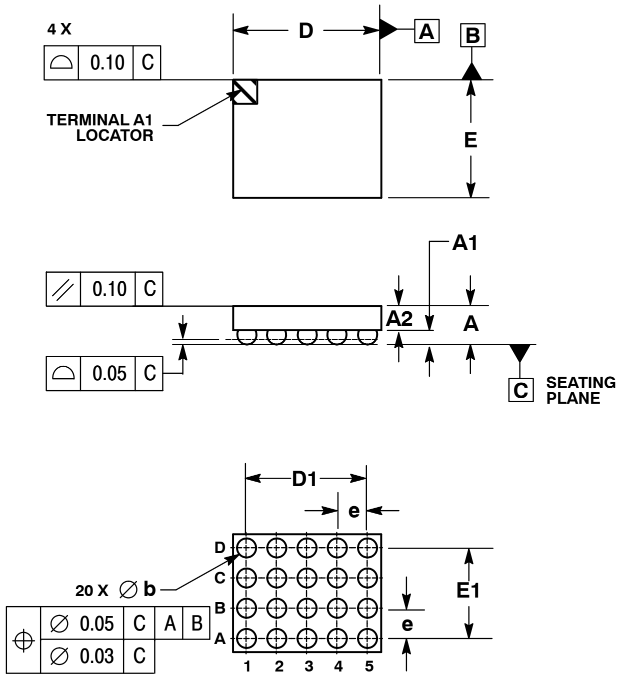
9−PIN FLIP−CHIP
CASE 499−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.945
A1	0.210	0.270
A2	0.625	0.675
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

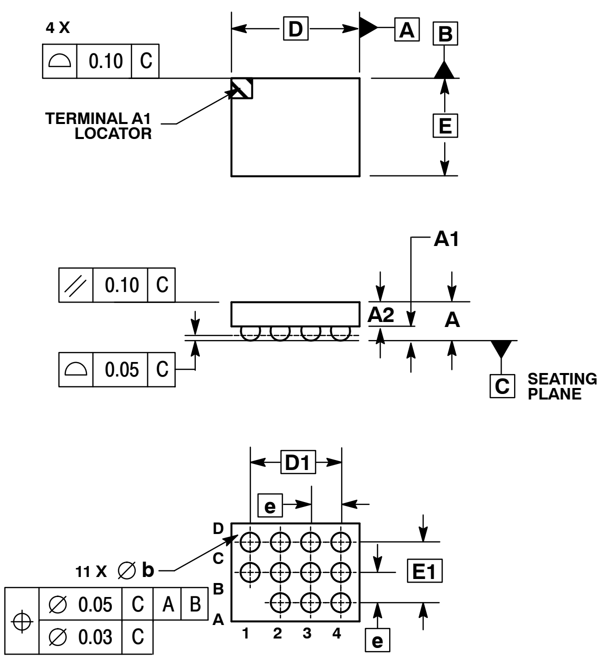
20–PIN FLIP–CHIP
CASE 499A–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.450 BSC	
E	1.950 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	2.000 BSC	
E1	1.500 BSC	

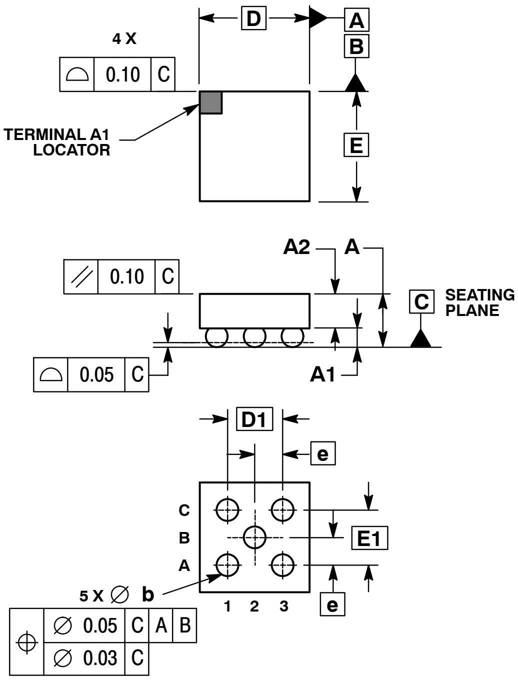
11–PIN FLIP–CHIP
CASE 499B–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.120 BSC	
E	1.620 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

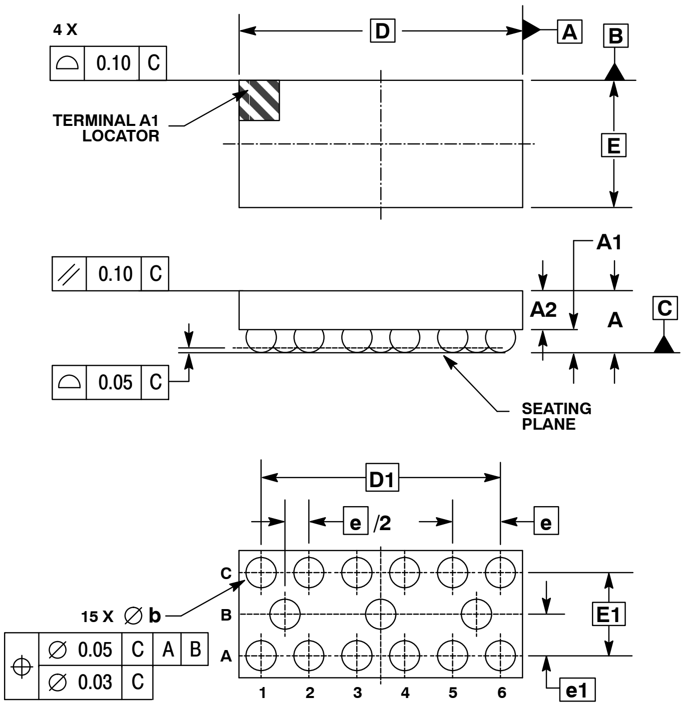
5−PIN FLIP−CHIP
CASE 499C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.300 BSC	
E	1.300 BSC	
b	0.290	0.340
e	0.354 BSC	
D1	0.707 BSC	
E1	0.707 BSC	

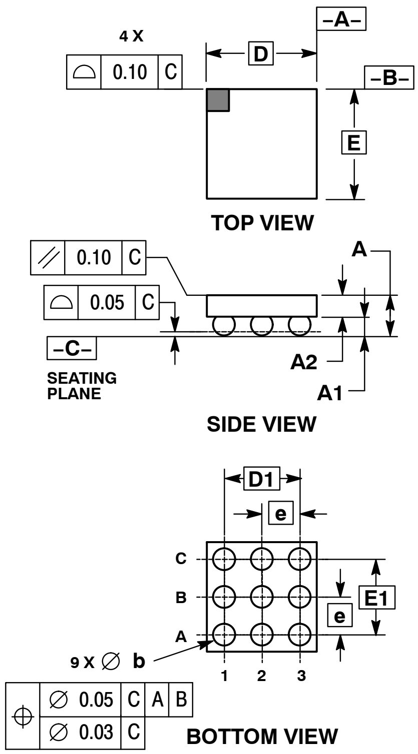
15−PIN FLIP−CHIP
CASE 499D−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.960 BSC	
E	1.330 BSC	
b	0.290	0.340
e	0.500 BSC	
e1	0.435 BSC	
D1	2.500 BSC	
E1	0.870 BSC	

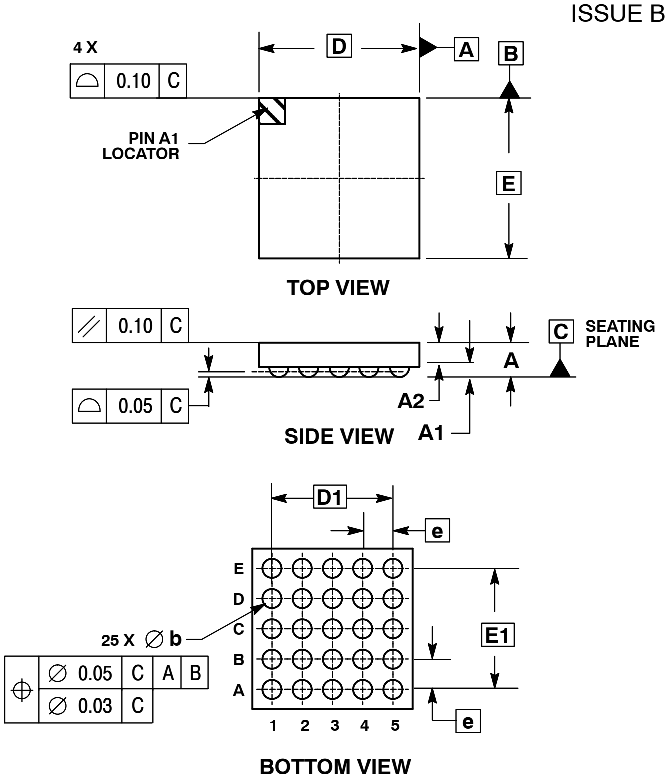
9−PIN FLIP−CHIP
CASE 499E−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

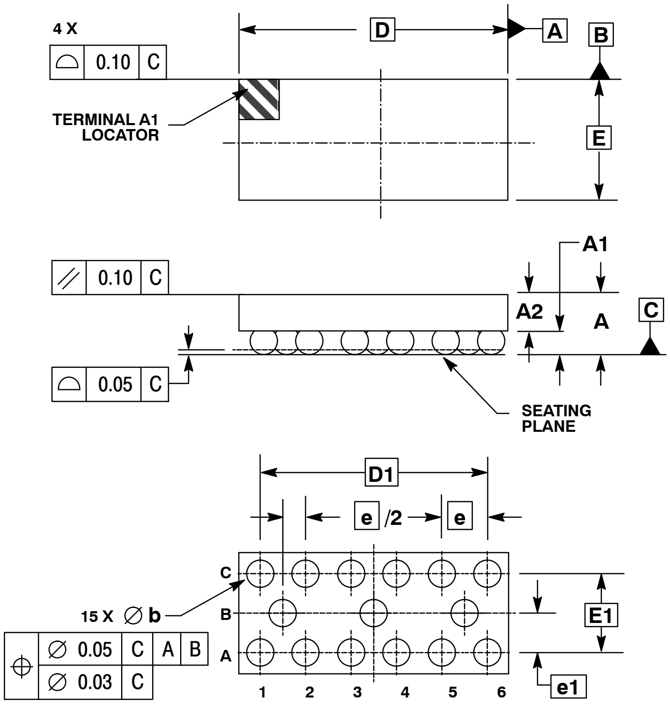
25−PIN FLIP−CHIP
CASE 499G−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.650 BSC	
E	2.650 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	2.000 BSC	
E1	2.000 BSC	

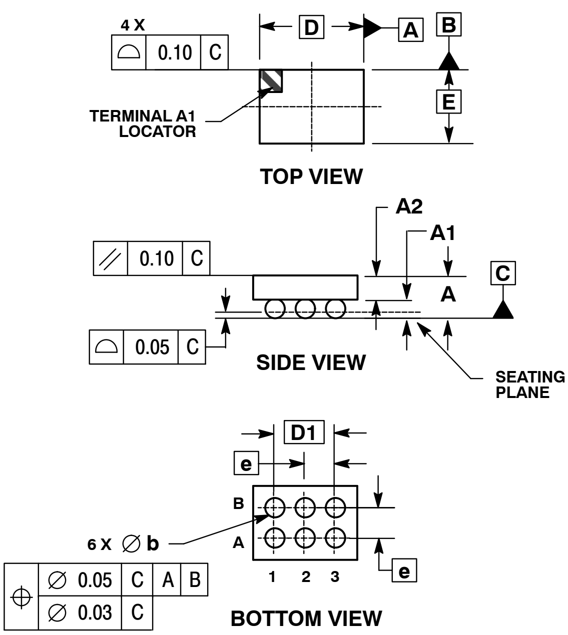
15−PIN FLIP−CHIP
CASE 499H−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	−−−	0.700
A1	0.240	0.280
A2	0.380	0.430
D	2.960 BSC	
E	1.330 BSC	
b	0.300	0.350
e	0.500 BSC	
e1	0.435 BSC	
D1	2.500 BSC	
E1	0.870 BSC	

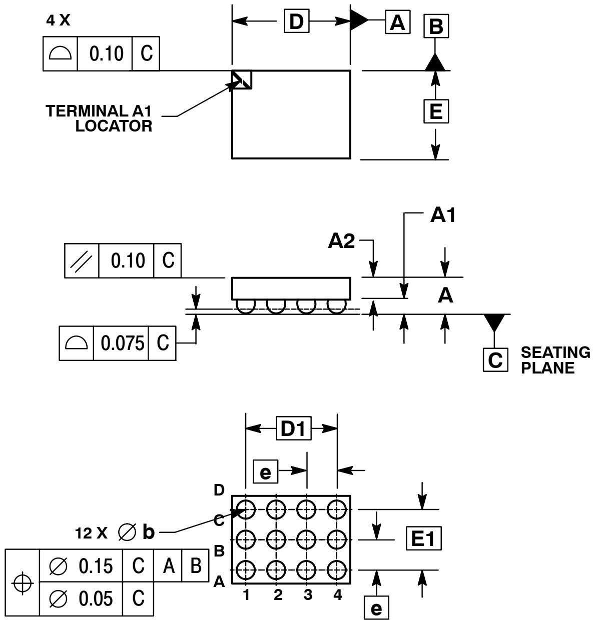
6−PIN FLIP−CHIP
CASE 499J−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.720 BSC	
E	1.220 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	

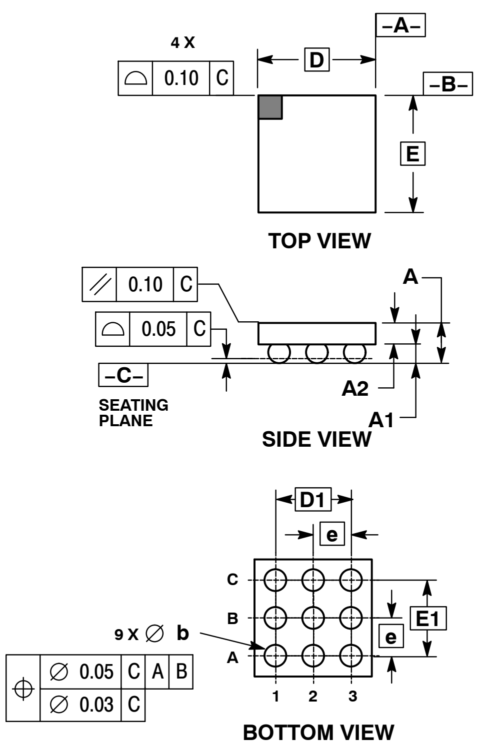
12−PIN FLIP−CHIP
CASE 499AB−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.550	0.650
A1	0.215	0.265
A2	0.36 REF	
D	1.90	2.00
E	1.4	1.5
b	0.250	0.350
e	0.500 BSC	
D1	1.500 BSC	
E1	1.000 BSC	

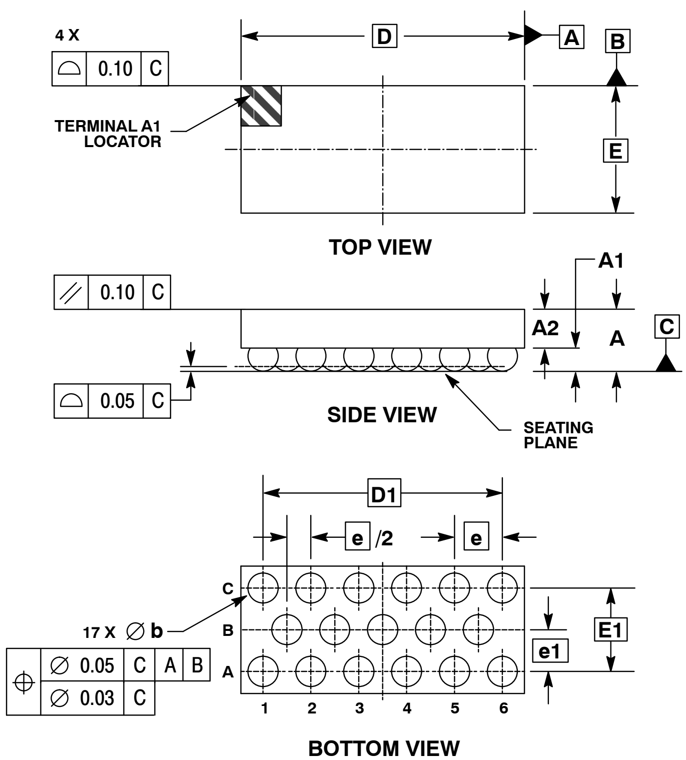
9−PIN FLIP−CHIP
CASE 499AC−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.550 BSC	
E	1.550 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

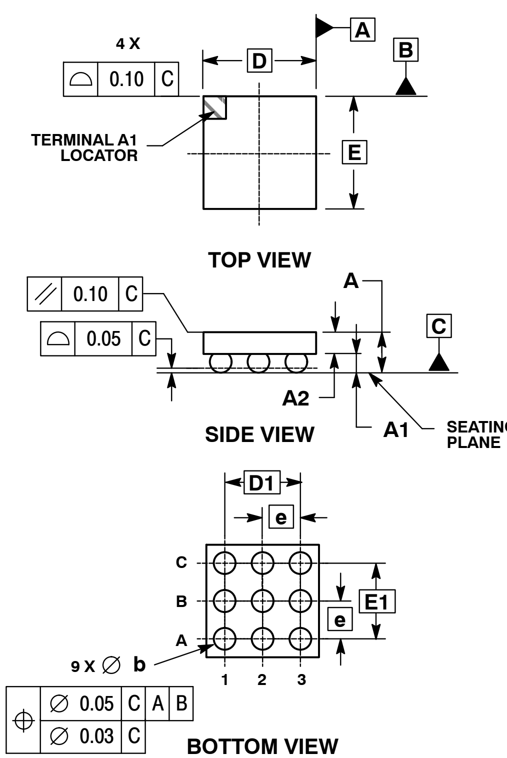
17−PIN FLIP−CHIP
CASE 499AD−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.740
A1	0.250	0.310
A2	0.380	0.430
D	2.960 BSC	
E	1.330 BSC	
b	0.350	0.410
e	0.500 BSC	
e1	0.435 BSC	
D1	2.500 BSC	
E1	0.870 BSC	

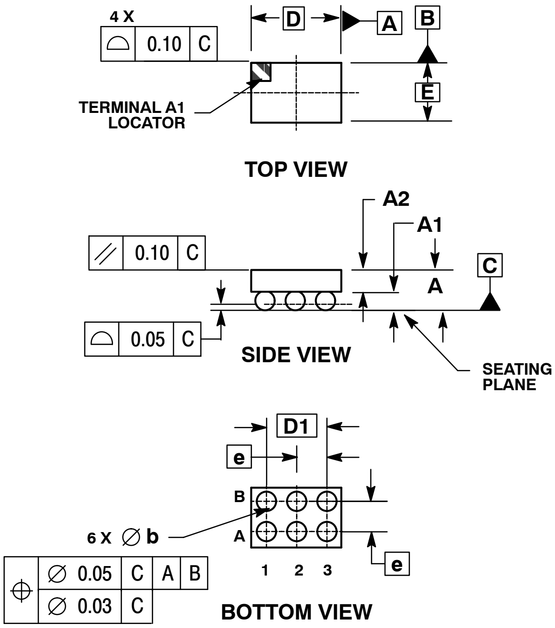
9−PIN FLIP−CHIP
CASE 499AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	– – –	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.489 BSC	
E	1.489 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

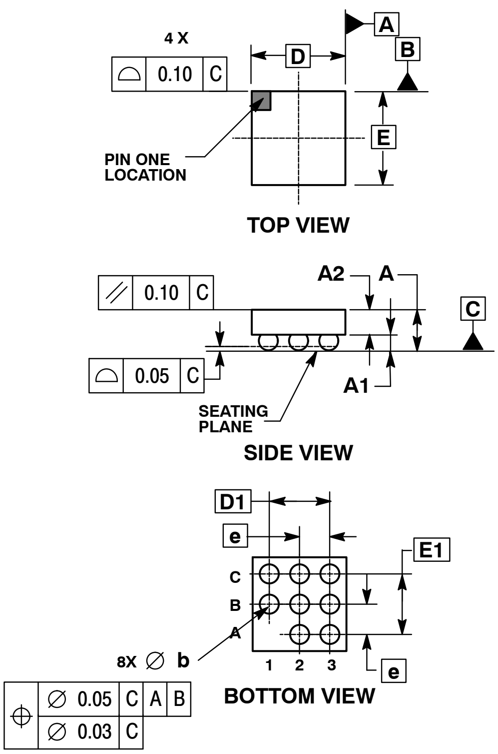
6−PIN FLIP−CHIP
CASE 499AF−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.489 BSC	
E	0.989 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	

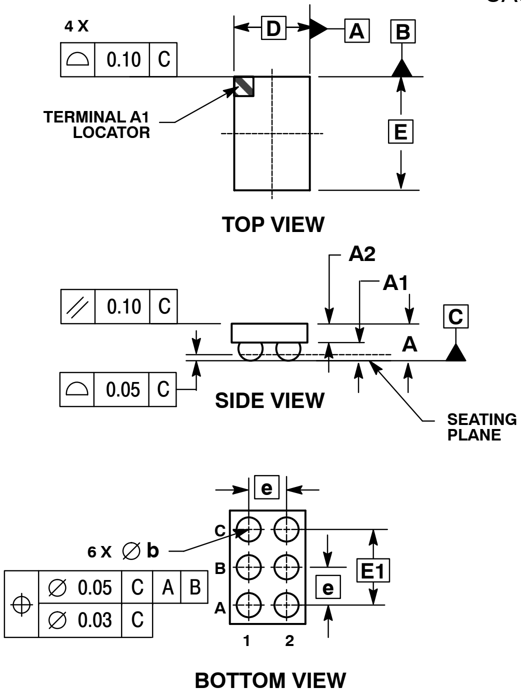
8−PIN FLIP−CHIP
CASE 499AG−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.550 BSC	
E	1.550 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

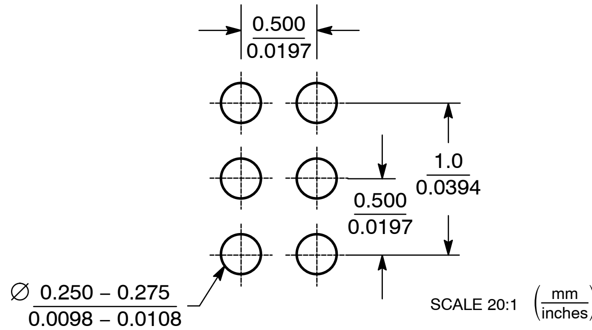
6−PIN FLIP−CHIP
CASE 499AH−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

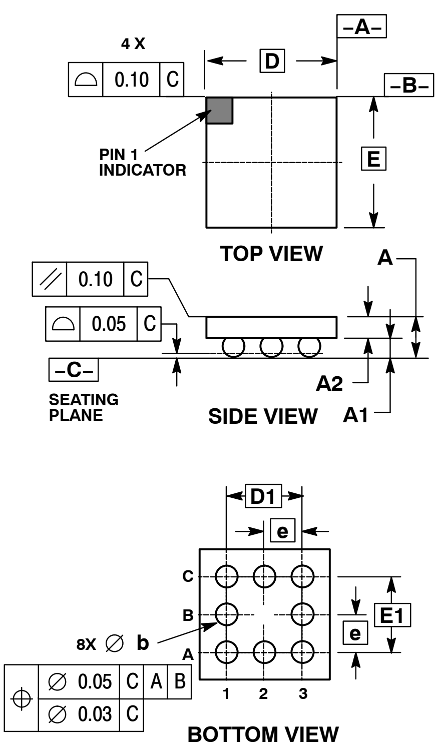
	MILLIMETERS	
DIM	MIN	MAX
A	0.448	0.533
A1	0.210	0.270
A2	0.238	0.263
D	1.000 BSC	
E	1.50 BSC	
b	0.290	0.340
e	0.500 BSC	
E1	1.000 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

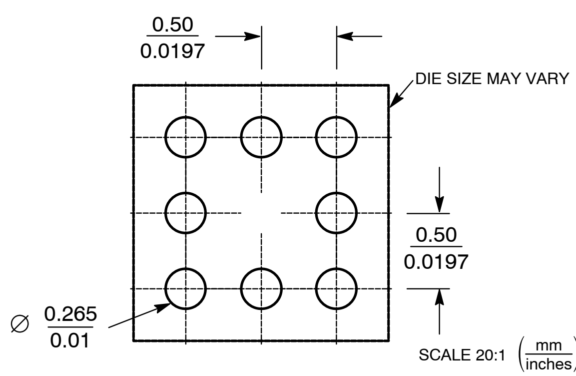
8−PIN FLIP−CHIP
CASE 499AJ−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

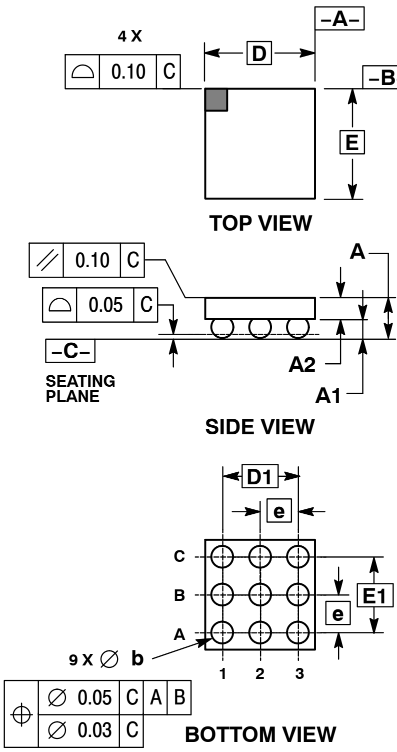
	MILLIMETERS	
DIM	MIN	MAX
A	0.6 BSC	
A1	0.210	0.270
A2	0.330	0.390
D	1.70 BSC	
E	1.70 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

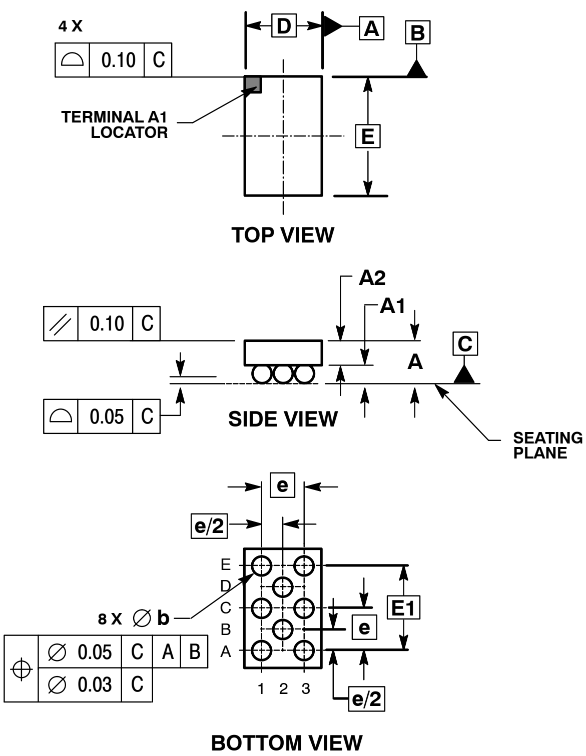
9−PIN FLIP−CHIP
CASE 499AL−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.540	0.660
A1	0.210	0.270
A2	0.330	0.390
D	1.450 BSC	
E	1.450 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	
E1	1.000 BSC	

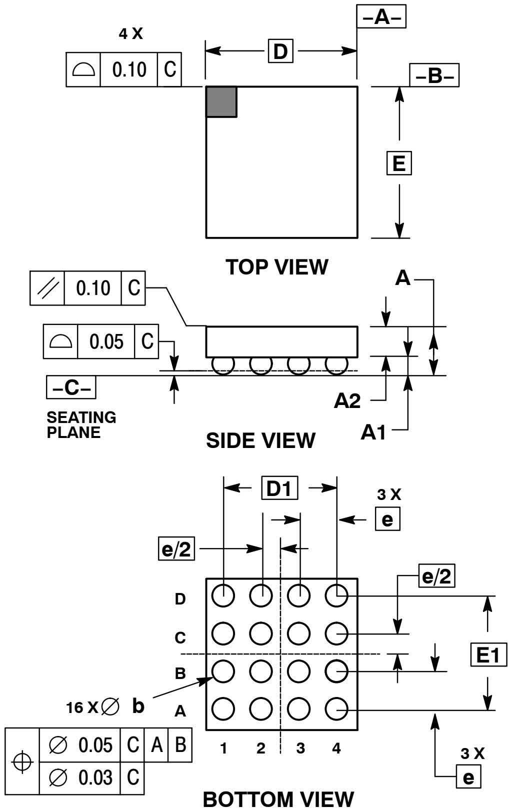
8−PIN FLIP−CHIP
CASE 499AM−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	1.270 BSC	
E	1.970 BSC	
b	0.290	0.340
e	0.700 BSC	
E1	1.400 BSC	

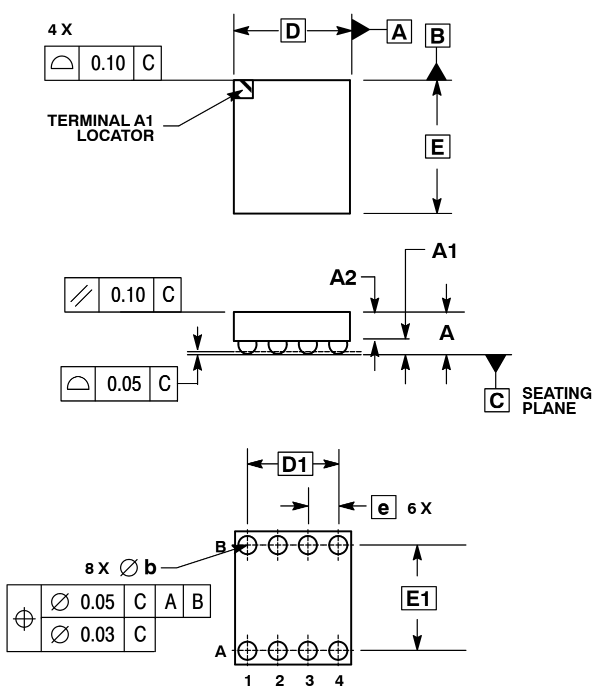
16−PIN FLIP−CHIP
CASE 499AN−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.700
A1	0.210	0.270
A2	0.380	0.430
D	2.000 BSC	
E	2.000 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.500 BSC	
E1	1.500 BSC	

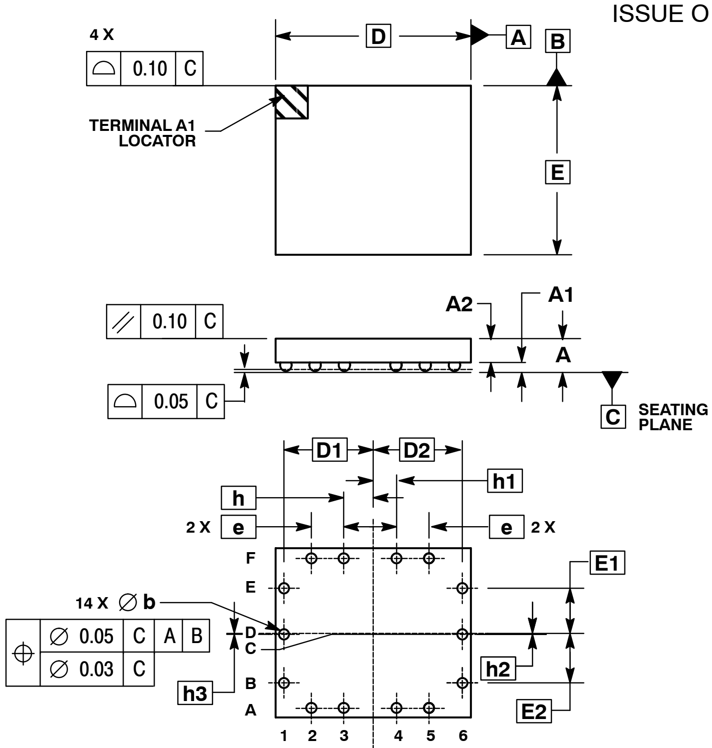
8−PIN FLIP−CHIP
CASE 499AP−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	−−−	0.647	0.697
A1	0.142	0.167	0.192
A2	0.455	0.480	0.505
b	0.190	0.220	0.224
D	1.920 BSC		
D1	1.512 BSC		
E	2.200 BSC		
E1	1.796 BSC		
e	0.504 BSC		

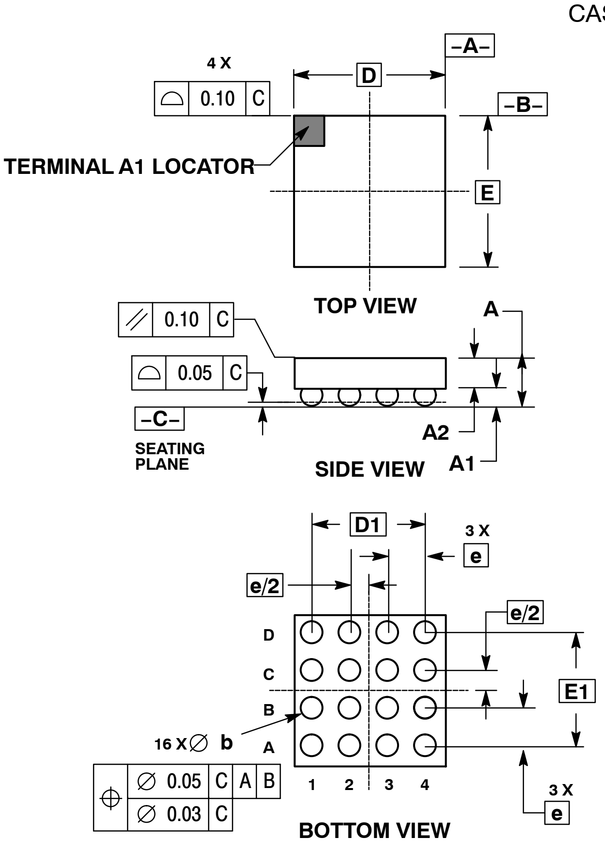
14−PIN FLIP−CHIP
CASE 499AQ−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	0.692	0.742
A1	0.142	0.167	0.192
A2	0.500	0.525	0.550
b	0.190	0.220	0.224
D	4.300 BSC		
D1	1.983 BSC		
D2	1.949 BSC		
E	3.730 BSC		
E1	1.016 BSC		
E2	1.075 BSC		
e	0.716 BSC		
h	0.648 BSC		
h1	0.514 BSC		
h2	0.034 BSC		
h3	0.029 BSC		

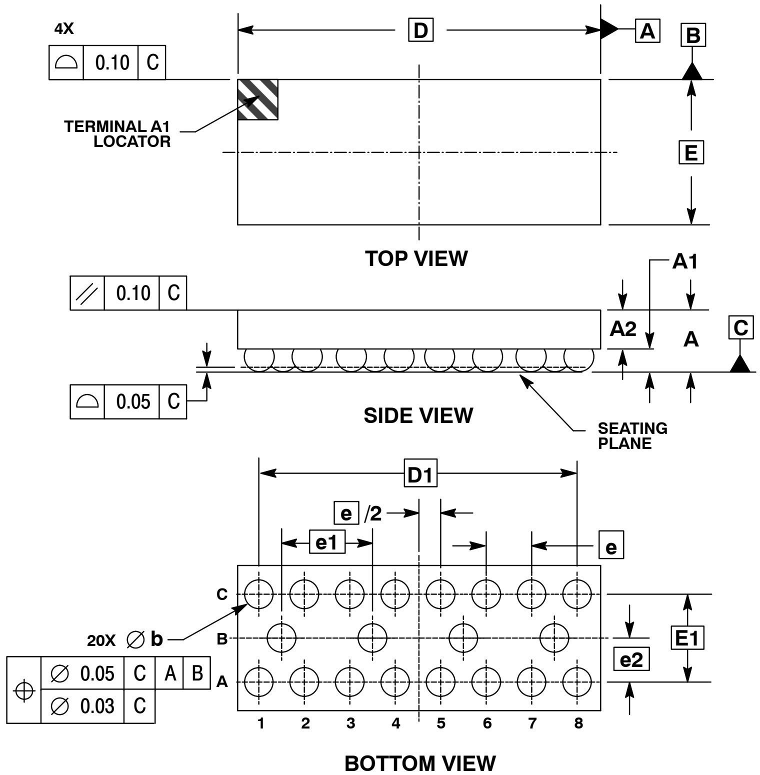
16−PIN FLIP−CHIP
CASE 499AR−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.650
A1	0.210	0.270
A2	0.280	0.380
D	2.050 BSC	
E	2.050 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.500 BSC	
E1	1.500 BSC	

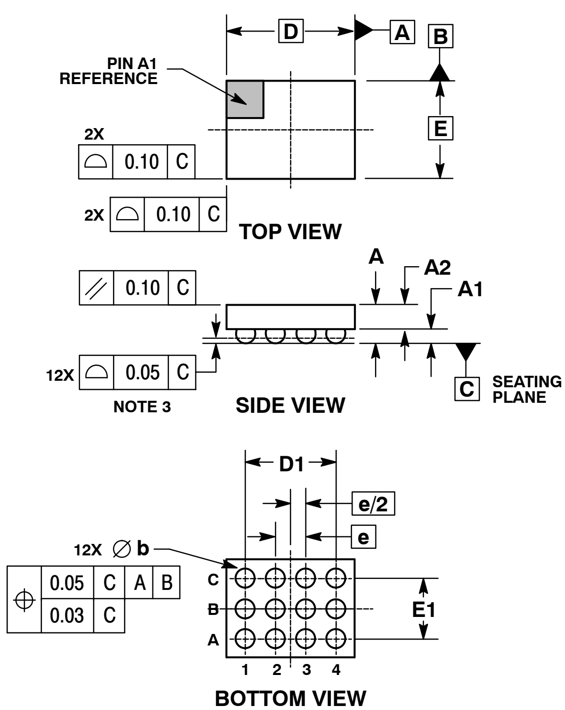
20−PIN FLIP−CHIP
CASE 499AS−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.650
A1	0.210	0.270
A2	0.280	0.380
b	0.290	0.340
D	4.000 BSC	
D1	3.500 BSC	
E	1.600 BSC	
E1	0.870 BSC	
e	0.500 BSC	
e1	1.000 BSC	
e2	0.435 BSC	

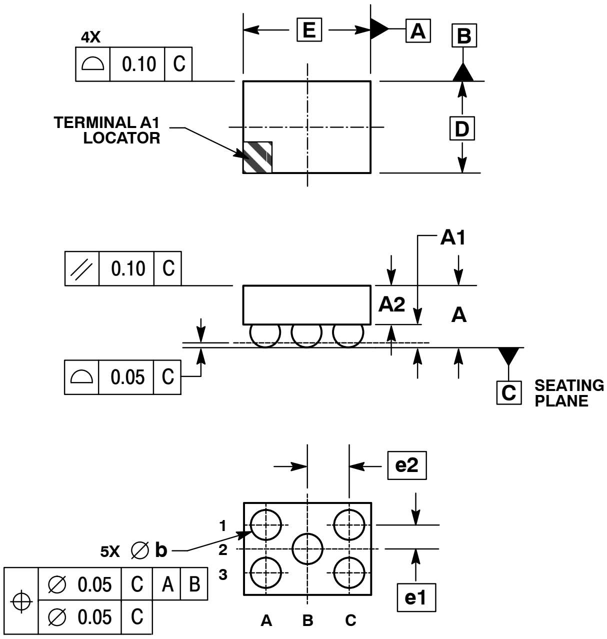
12−PIN FLIP−CHIP
CASE 499AU−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.66
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.02 BSC	
D1	1.50 BSC	
E	1.54 BSC	
E1	1.00 BSC	
e	0.50 BSC	

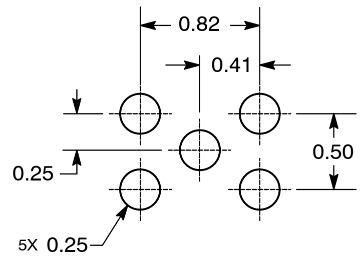
5−PIN FLIP−CHIP
CASE 499AY−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.475	0.530	0.585
A1	0.170	0.200	0.230
A2	0.305	0.330	0.355
b	0.220	0.250	0.270
D		1.028 BSC	
E		1.190 BSC	
e1		0.250 BSC	
e2		0.410 BSC	

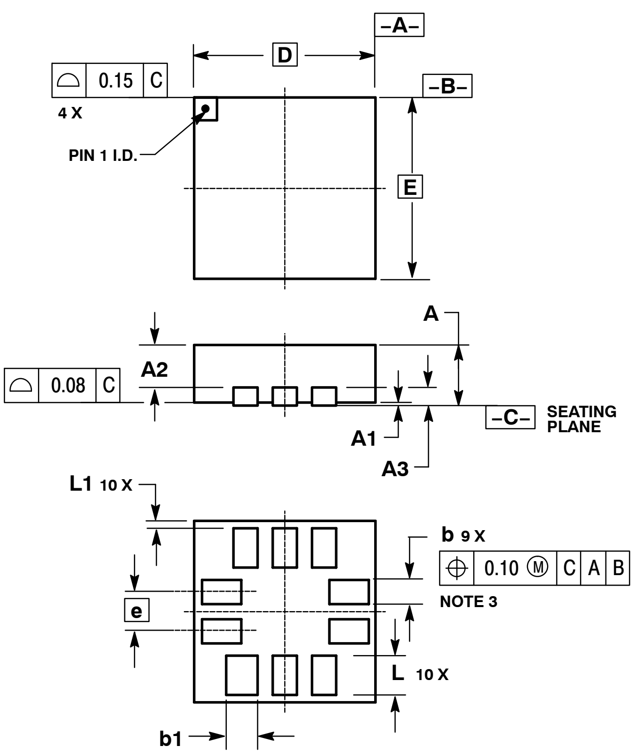
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

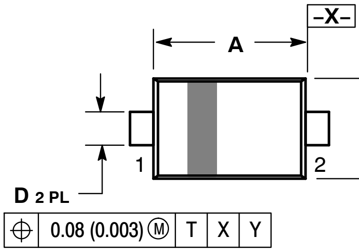
QFN10, 3x3
CASE 501−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. 501−01 OBSOLETE, NEW STANDARD IS −02.

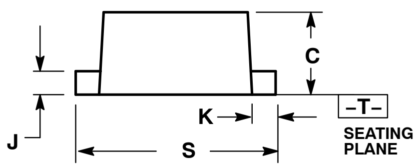
	MILLIMETERS	
DIM	MIN	MAX
A	0.800	1.000
A1	0.000	0.050
A2	0.600	0.800
A3	0.203 REF	
D	3.00 BSC	
E	3.00 BSC	
b	0.371	0.421
b1	0.498	0.548
e	0.650 BSC	
L	0.523	0.673
L1	0.000	0.127

SOD−523
SC−79
CASE 502−01
ISSUE C

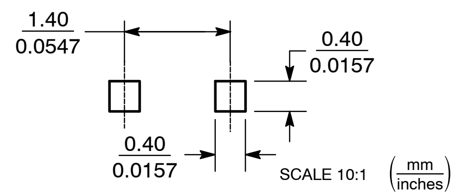


NOTES:
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: MILLIMETER.
8. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.10	1.20	1.30	0.043	0.047	0.051
B	0.70	0.80	0.90	0.028	0.032	0.035
C	0.50	0.60	0.70	0.020	0.024	0.028
D	0.25	0.30	0.35	0.010	0.012	0.014
J	0.07	0.14	0.20	0.0028	0.0055	0.0079
K	0.15	0.20	0.25	0.006	0.008	0.010
S	1.50	1.60	1.70	0.059	0.063	0.067



SOLDERING FOOTPRINT*

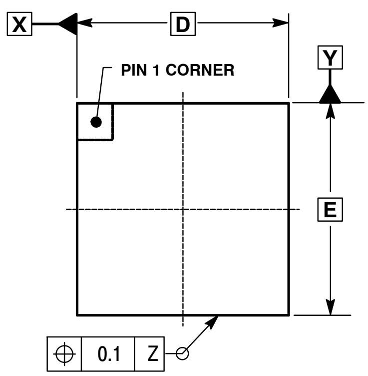


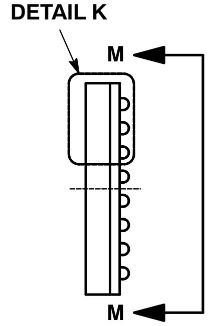
STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

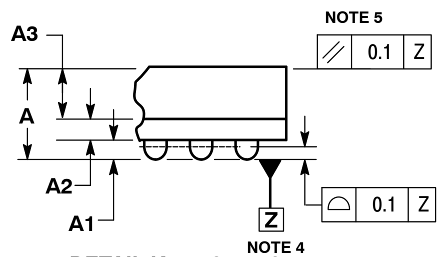
STYLE 2:
NO POLARITY

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

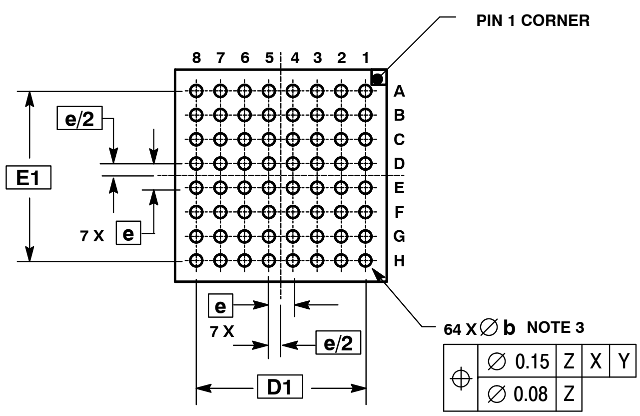
64 PIN LFBGA, 7x7
CASE 504−01
ISSUE O







DETAIL K
ROTATED 90° CLOCKWISE

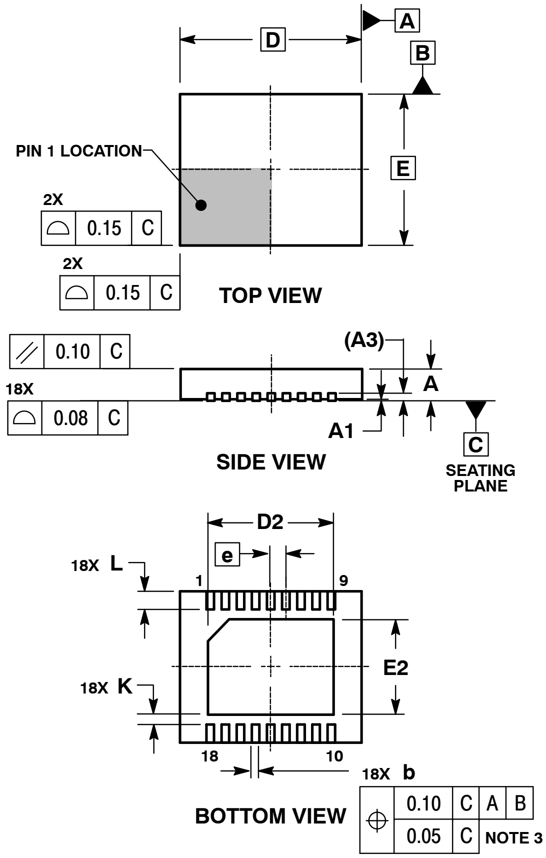


VIEW M−M

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M−1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	---	---	1.5
A1	0.27	---	0.37
A2	0.32 REF		
A3	0.8 REF		
b	0.35	0.4	0.45
D	7.0 BSC		
E	7.0 BSC		
e	0.8 BSC		
D1	5.6 BSC		
E1	5.6 BSC		

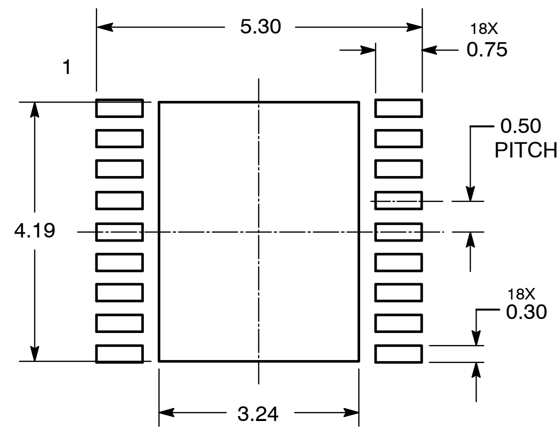
DFN18 6x5, 0.5P
CASE 505−01
ISSUE D



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

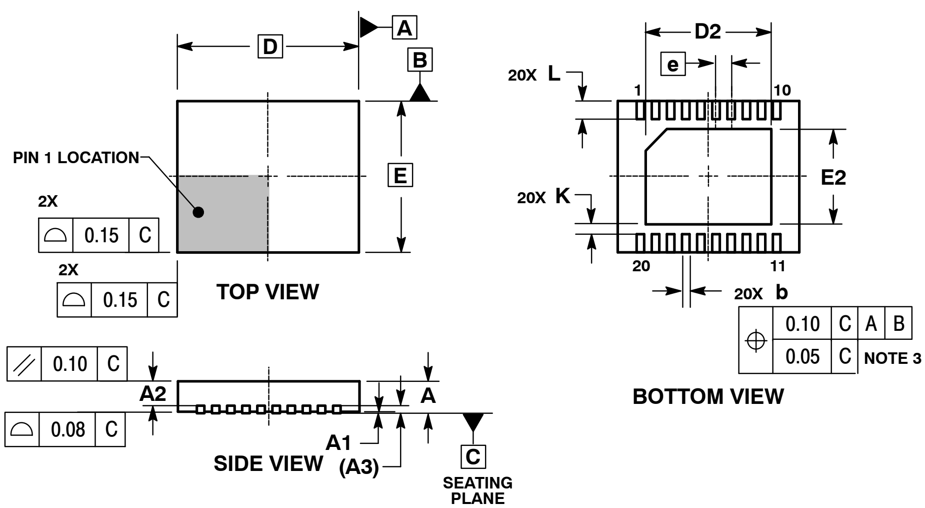
	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.45	0.65

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

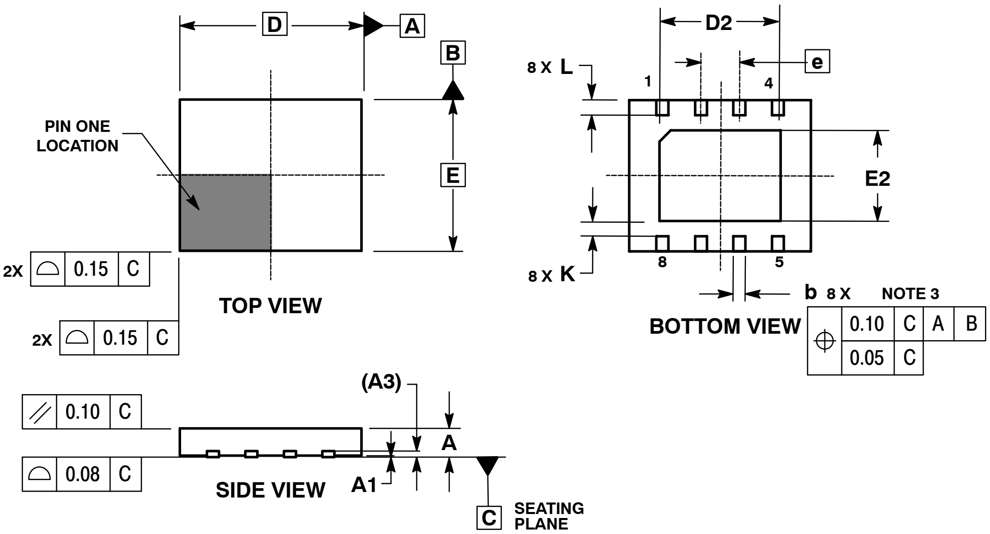
DFN20, 6x5
CASE 505AB−01
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A2	0.65	0.75
A3	0.20 REF	
b	0.23	0.28
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.50	0.60

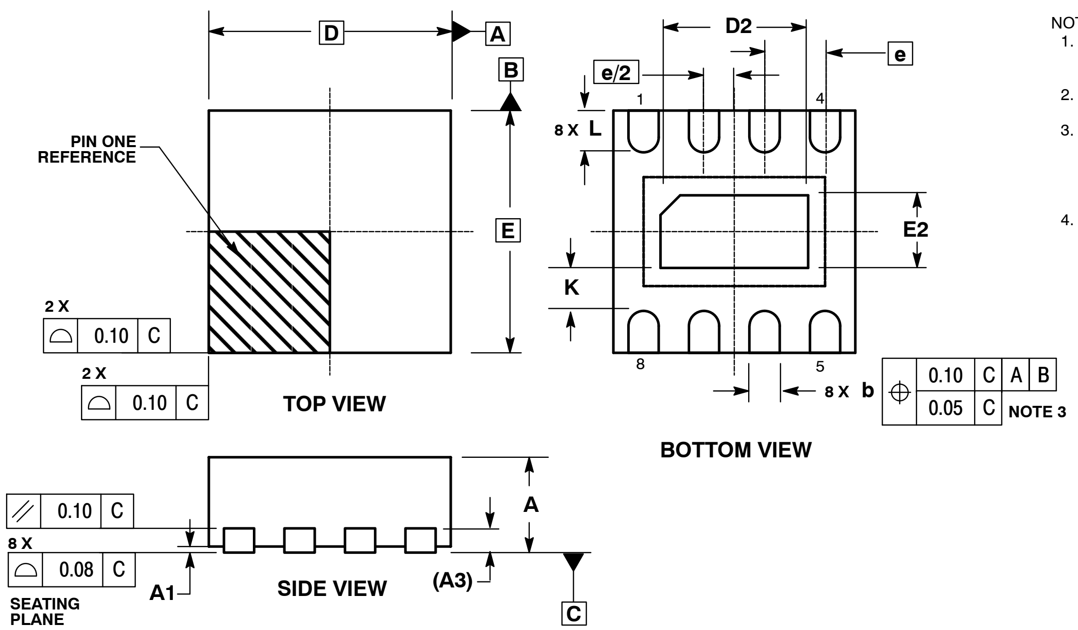
DFN8, 6x5
CASE 505AC−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.35	0.50
D	6.00 BSC	
D2	3.95	4.25
E	5.00 BSC	
E2	2.95	3.25
e	1.27 BSC	
K	0.20	−−−
L	0.45	0.65

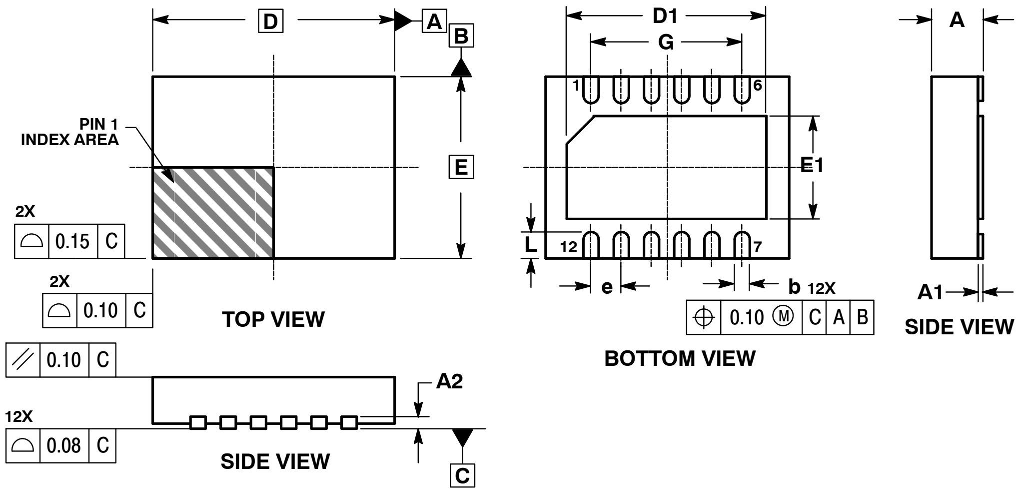
DFN8, 2x2
CASE 506AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

DFN12, 4x3
CASE 506AB−01
ISSUE O

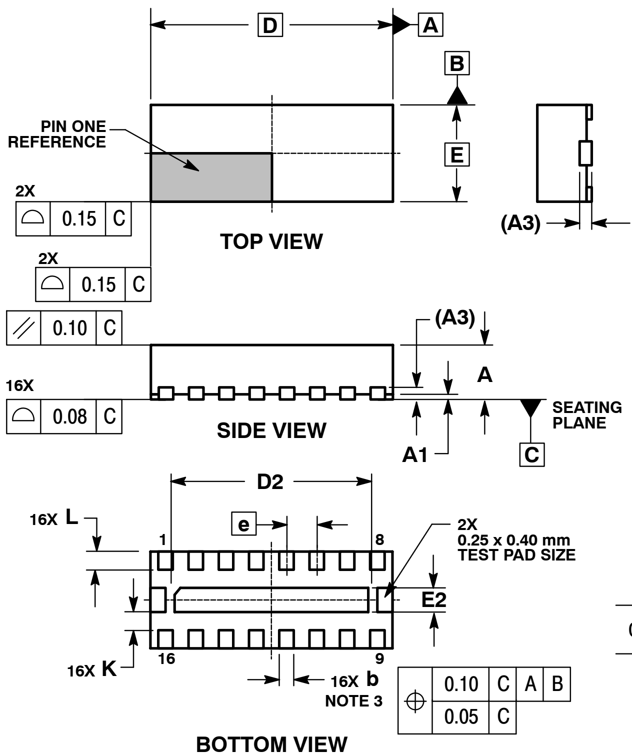


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. COPLANARITY SHALL NOT EXCEED 0.08 MM.
4. WARPAGE SHALL NOT EXCEED 0.10 MM.
5. PACKAGE LENGTH AND WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.
6. REFER TO JEDEC WD−228.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	−−−	0.05
A2	0.20 REF		
b	0.20	0.25	0.30
D	4.00 BSC		
D1	3.20	3.30	3.40
E	3.00 BSC		
E1	1.60	1.70	1.80
e	0.50 TYP		
G	2.50 REF		
L	0.30	0.40	0.50

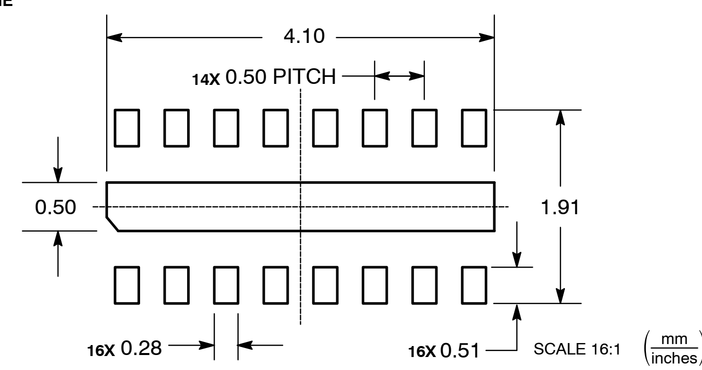
DFN16, 4x1.6
CASE 506AC−01
ISSUE B

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	4.00 BSC	
D2	3.10	3.30
E	1.60 BSC	
E2	0.30	0.50
e	0.50 BSC	
K	0.20	−−−
L	0.20	0.40

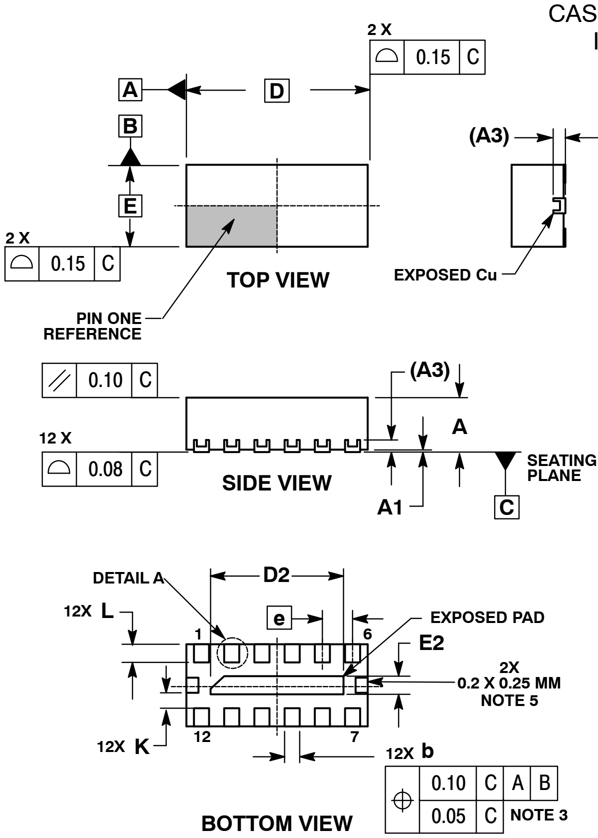
SOLDERING FOOTPRINT*



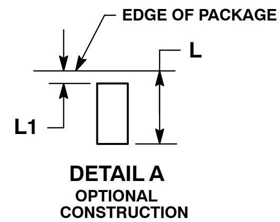
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DFN12, 3.0x1.35, 0.5P

CASE 506AD−01
ISSUE H

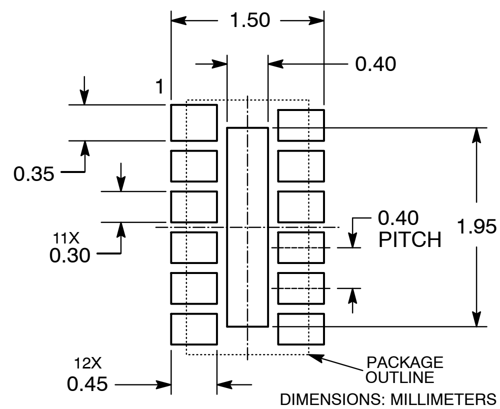


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.



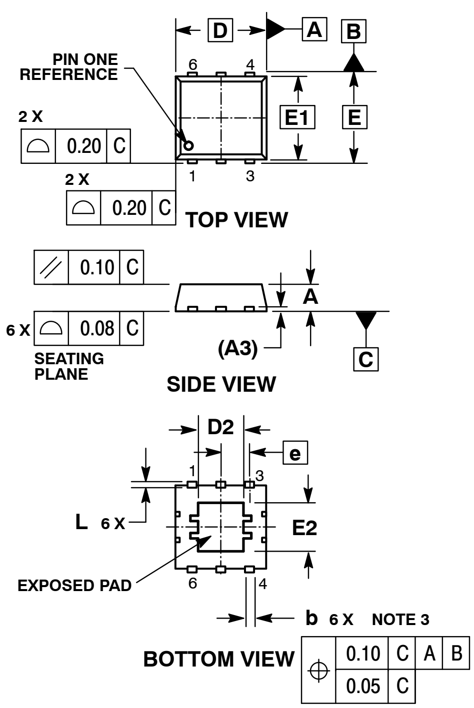
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	2.10	2.30
E	1.35 BSC	
E2	0.20	0.40
e	0.50 BSC	
K	0.20	---
L	0.20	0.40
L1	0.00	0.15

SOLDERING FOOTPRINT



HSON−6

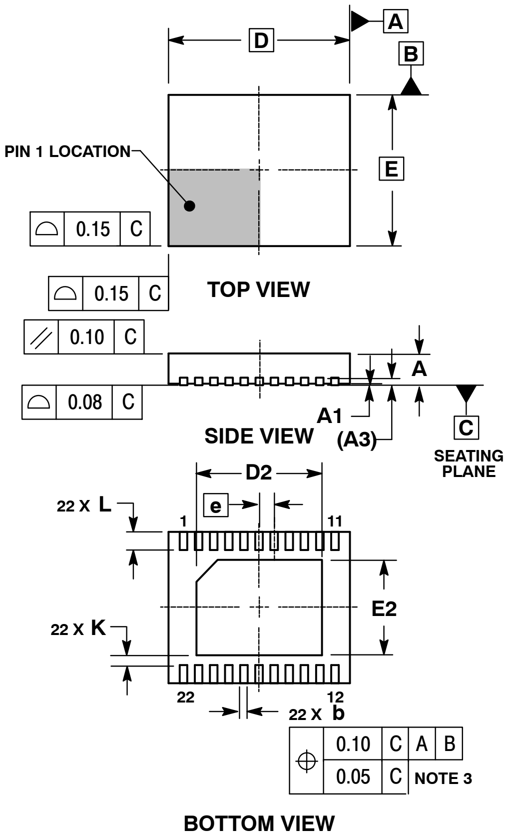
CASE 506AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.15 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.90
A3	0.15 REF	
b	0.20	0.40
D	2.90 BSC	
D2	1.40	1.60
E	3.00 BSC	
E1	2.80 BSC	
E2	1.50	1.70
e	0.95 BSC	
L	0.15	0.25

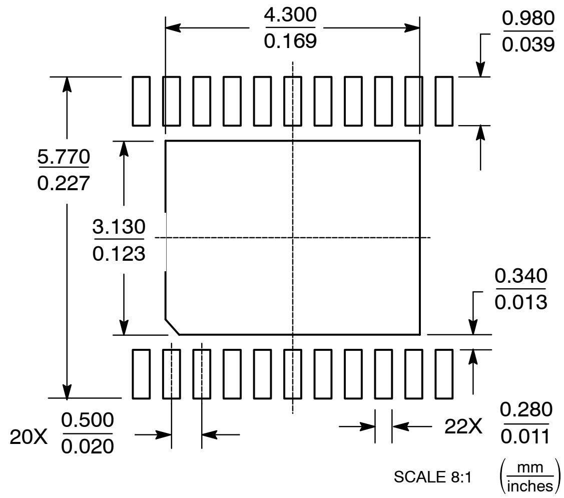
DFN22, 6x5
CASE 506AF−01
ISSUE O



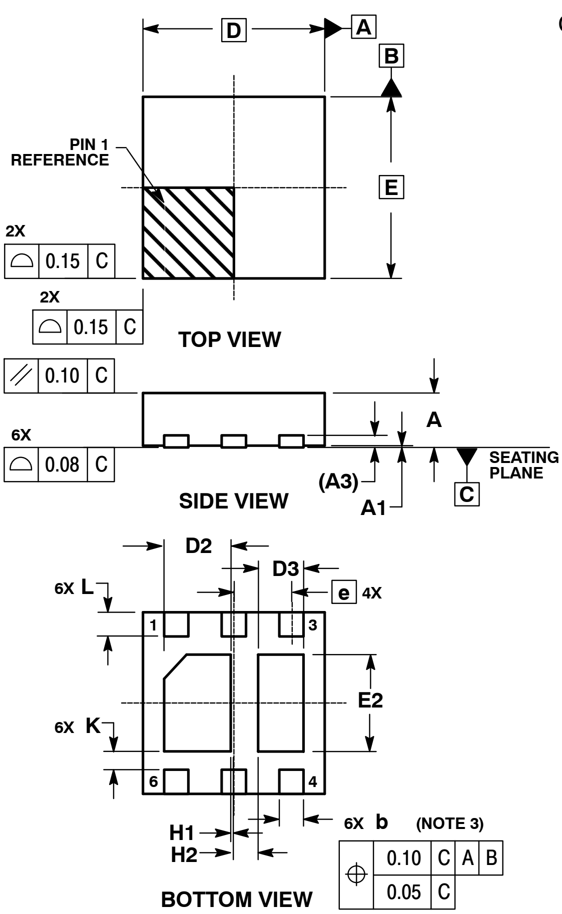
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	−−−
L	0.50	0.60

SOLDERING FOOTPRINT



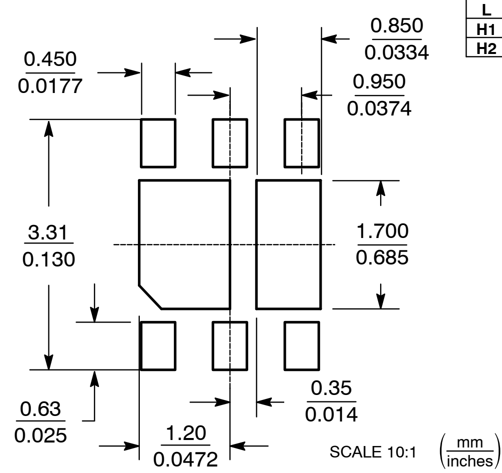
DFN6, 3x3
CASE 506AG−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

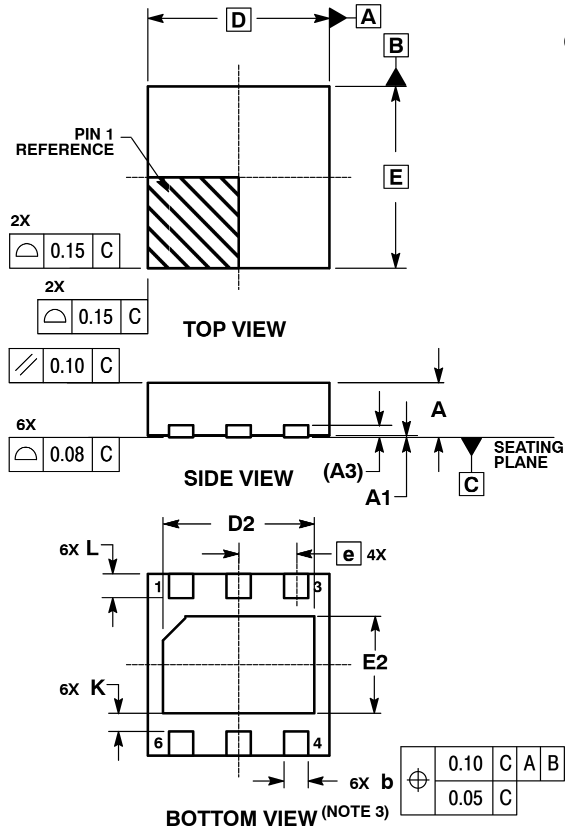
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.35	0.40	0.45
D	3.00 BSC		
D2	1.00	1.10	1.20
D3	0.65	0.75	0.85
E	3.00 BSC		
E2	1.50	1.60	1.70
e	0.95 BSC		
K	0.21	−−−	−−−
L	0.30	0.40	0.50
H1	0.05 REF		
H2	0.40 REF		

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

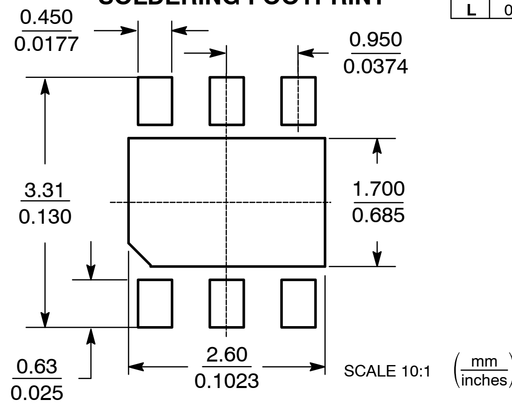
DFN6, 3x3
CASE 506AH−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

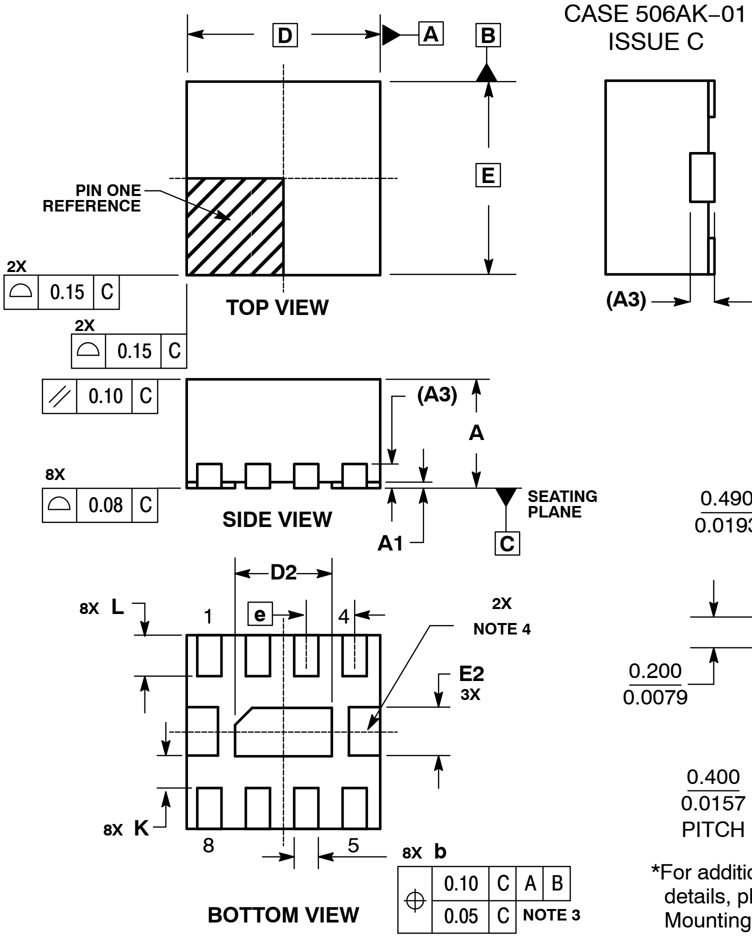
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.35	0.40	0.45
D	3.00 BSC		
D2	2.40	2.50	2.60
E	3.00 BSC		
E2	1.50	1.60	1.70
e	0.95 BSC		
K	0.21	---	---
L	0.30	0.40	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

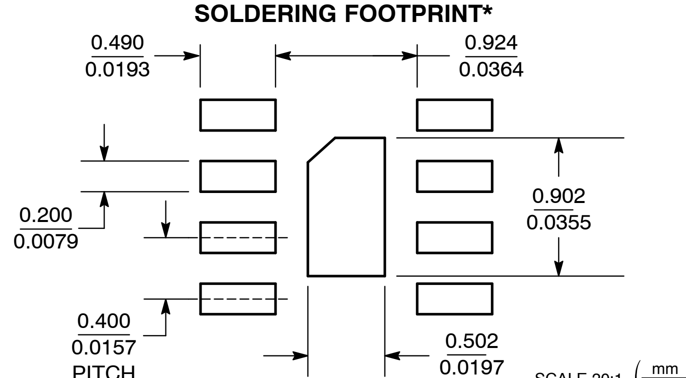
DFN8, 1.6x1.6
CASE 506AK−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

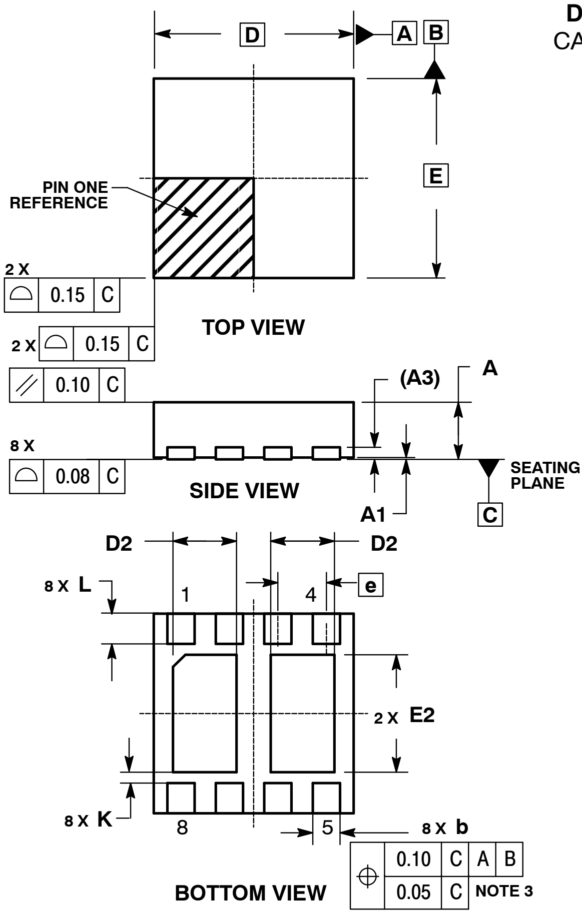
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	1.60 BSC	
D2	0.70	0.90
E	1.60 BSC	
E2	0.30	0.50
e	0.40 BSC	
K	0.20	---
L	0.20	0.40

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

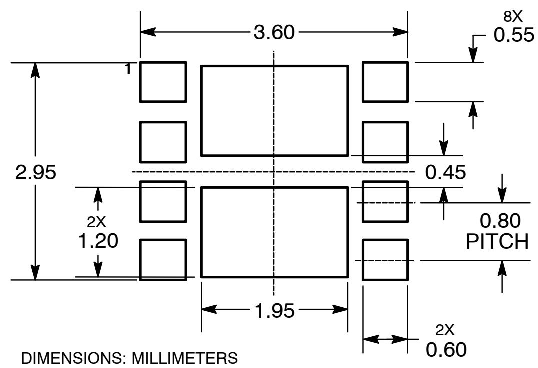
DFN8, 3.3x3.3
CASE 506AL−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

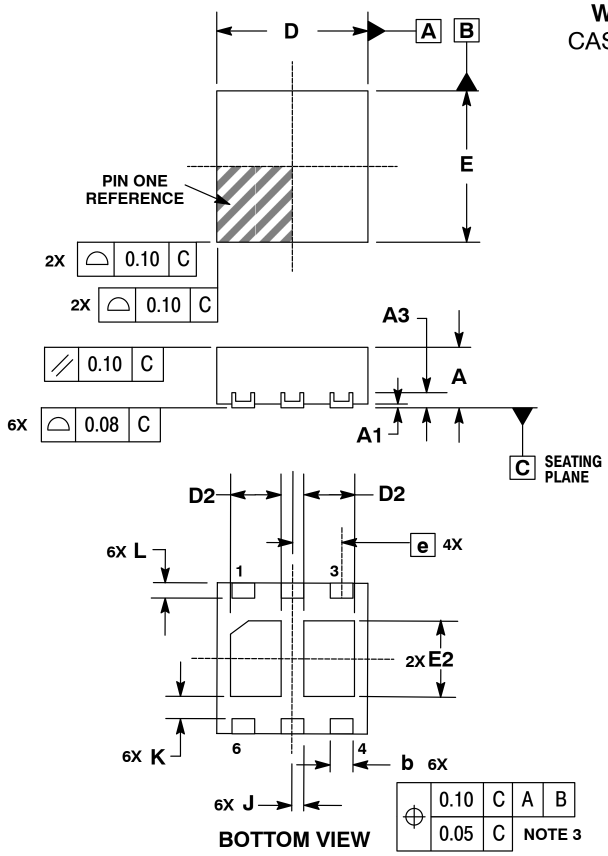
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.35	0.40	0.45
D	3.30 BSC		
D2	0.95	1.05	1.15
E	3.30 BSC		
E2	1.80	1.90	2.00
e	0.80 BSC		
K	0.21	---	---
L	0.30	0.40	0.50

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

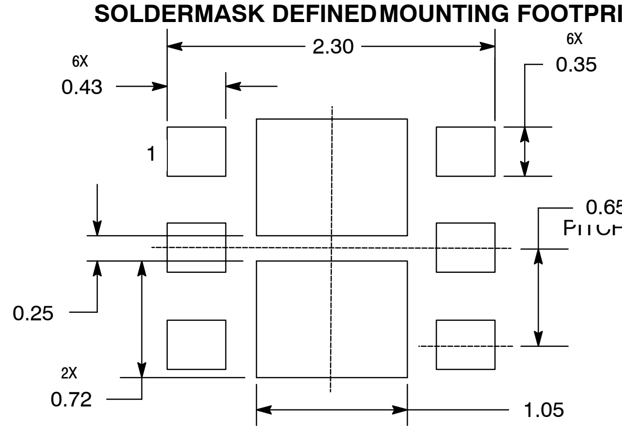
WDFN6, 2x2
CASE 506AN−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

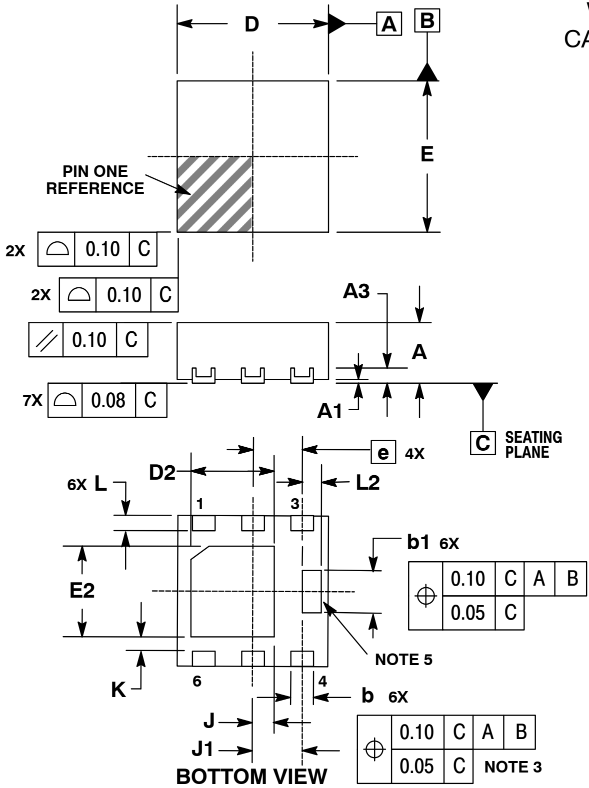
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

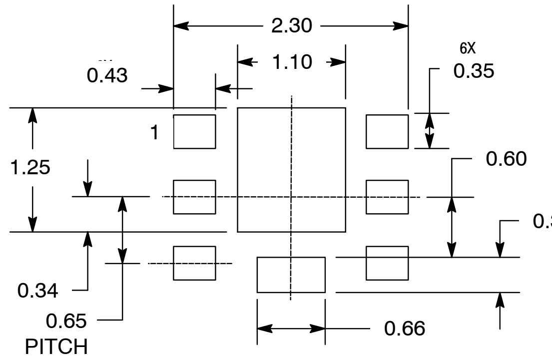
WDFN6, 2x2
CASE 506AP−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. CENTER TERMINAL LEAD IS OPTIONAL. TERMINAL LEAD IS CONNECTED TO TERMINAL LEAD # 4.
6. PINS 1, 2, 5 AND 6 ARE TIED TO THE FLAG.

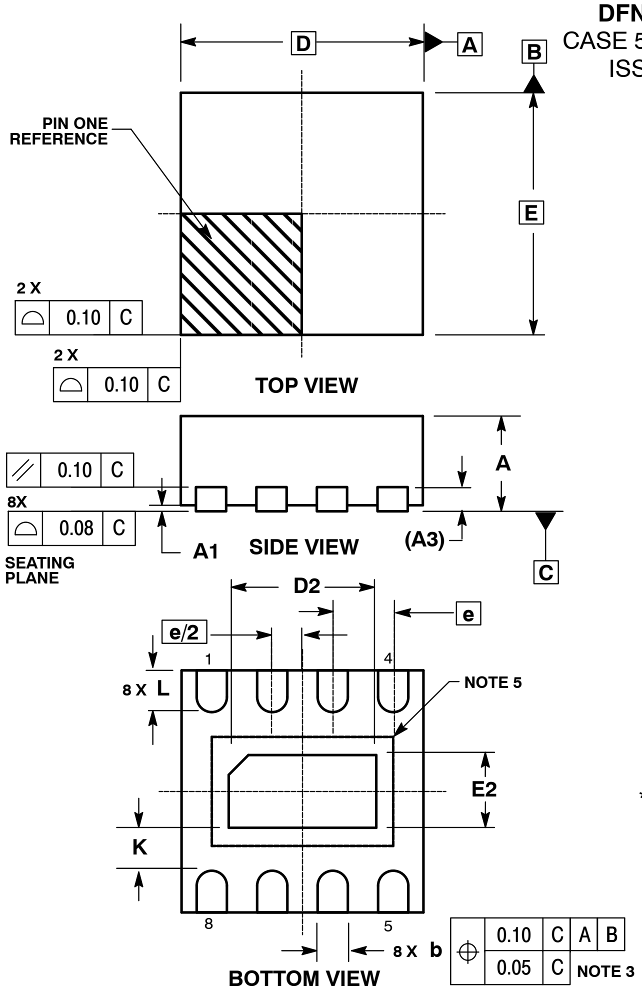
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
b1	0.51	0.61
D	2.00 BSC	
D2	1.00	1.20
E	2.00 BSC	
E2	1.10	1.30
e	0.65 BSC	
K	0.15 REF	
L	0.20	0.30
L2	0.20	0.30
J	0.27 REF	
J1	0.65 REF	

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

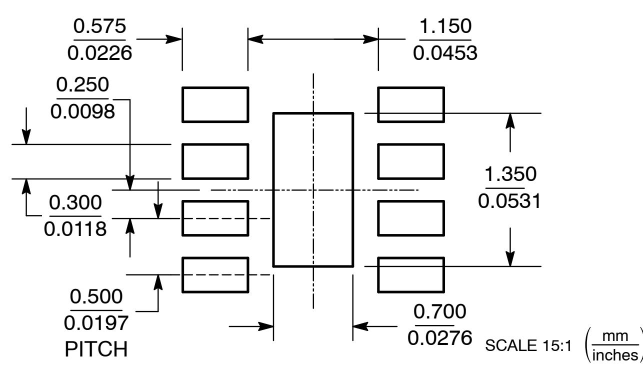
DFN8, 2x2
CASE 506AQ−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. INTERNAL PAD SIZE: 1.5 X 0.9 MM.

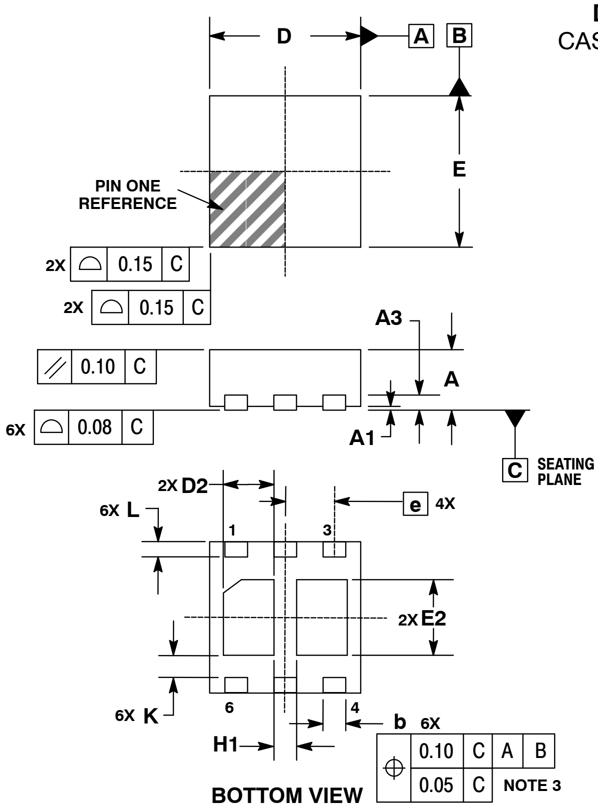
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.50	0.70
e	0.50 BSC	
K	0.20	---
L	0.25	0.45

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

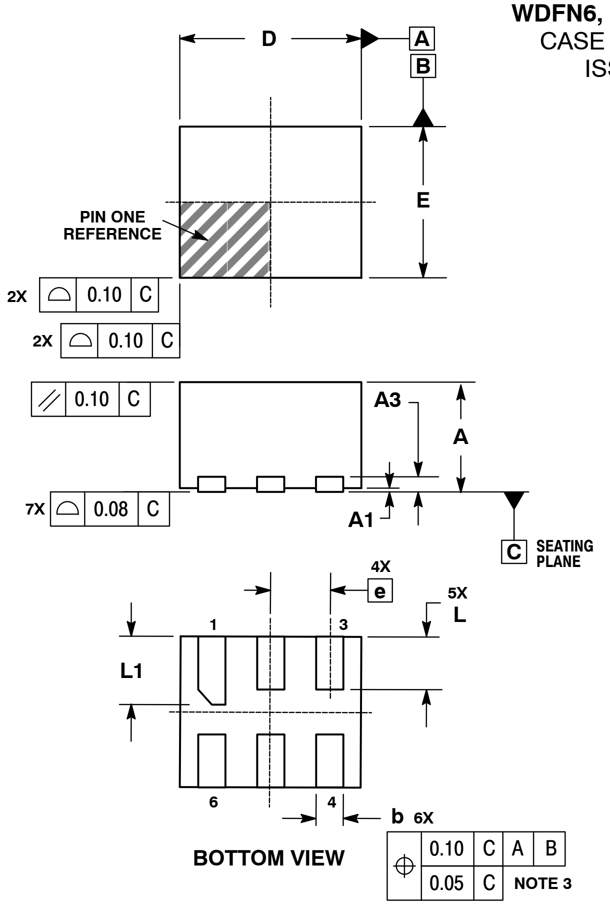
DFN6, 3x3
CASE 506AR−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.05	0.05
A3	0.20 REF		
b	0.35	0.40	0.45
D	3.00 BSC		
D2	1.025	1.125	1.225
E	3.00 BSC		
E2	1.60	1.70	1.80
e	0.95 BSC		
K	0.15	---	---
L	0.30	0.40	0.50
H1	0.30 REF		

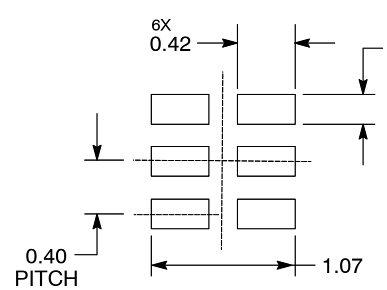
WDFN6, 1.2x1.0, 0.4P
CASE 506AS−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.40	0.50

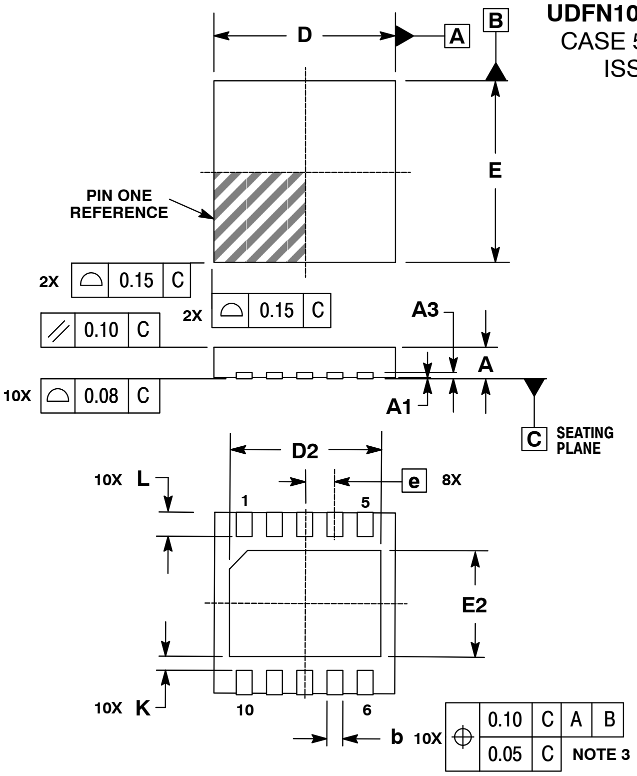
MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

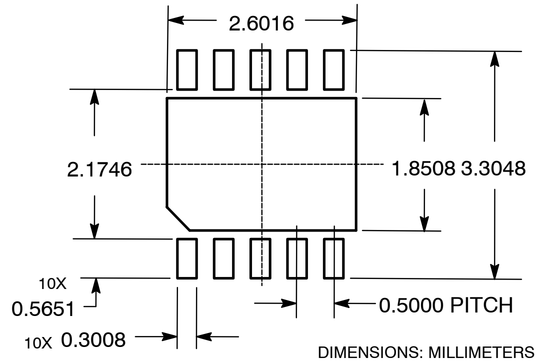
UDFN10, 3x3, 0.5P
CASE 506AT−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

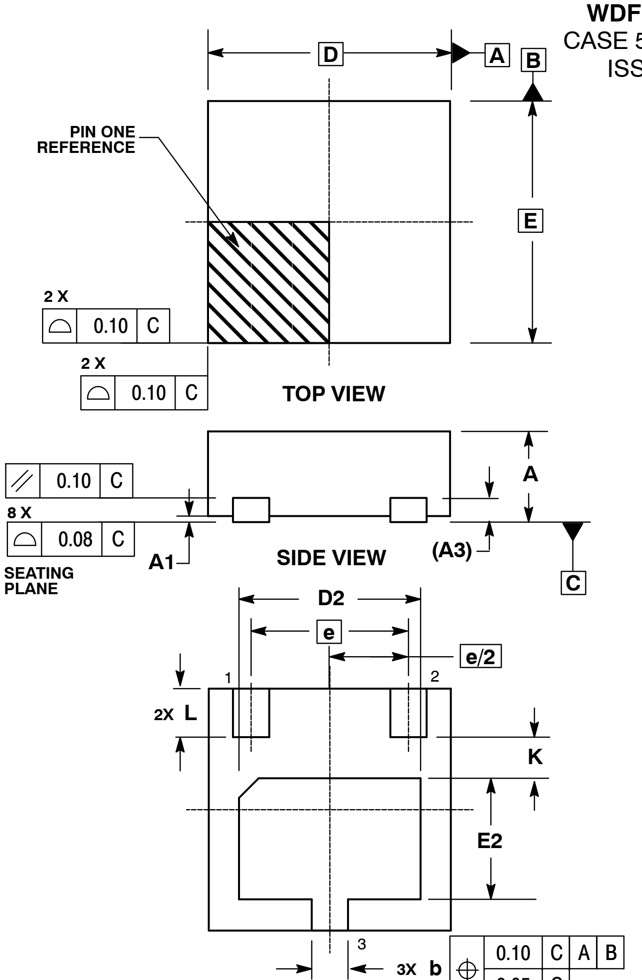
DIM	MILLIMETERS MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3		0.127 REF	
b	0.18	0.25	0.30
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.19 TYP	
L	0.30	0.40	0.50

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

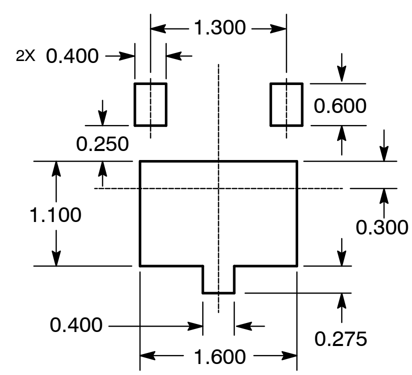
WDFN3, 2x2
CASE 506AU−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

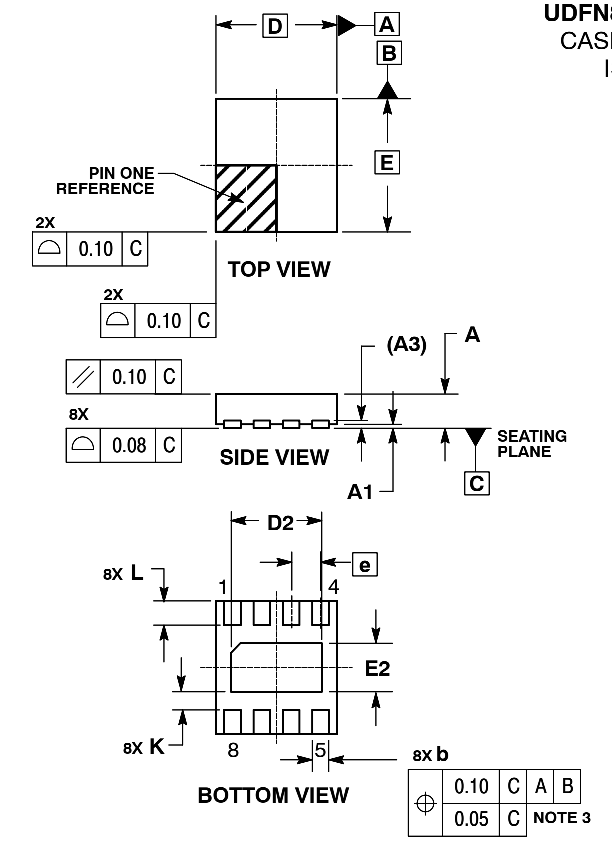
DIM	MILLIMETERS MIN	NOM	MAX	INCHES MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00		0.05	0.000		0.002
A3		0.20 REF			0.008 REF	
b	0.25	0.30	0.35	0.010	0.012	0.014
D		2.00 BSC			0.079 BSC	
D2	1.40	1.50	1.60	0.055	0.059	0.063
E		2.00 BSC			0.079 BSC	
E2	0.90	1.00	1.10	0.035	0.039	0.043
e		1.30 BSC			0.051 BSC	
K		0.35 REF			0.014 REF	
L	0.35	0.40	0.45	0.014	0.016	0.018

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

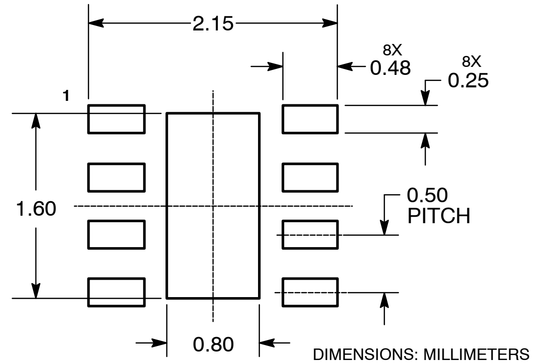
UDFN8, 2x2.2, 0.5P
CASE 506AV−01
ISSUE B



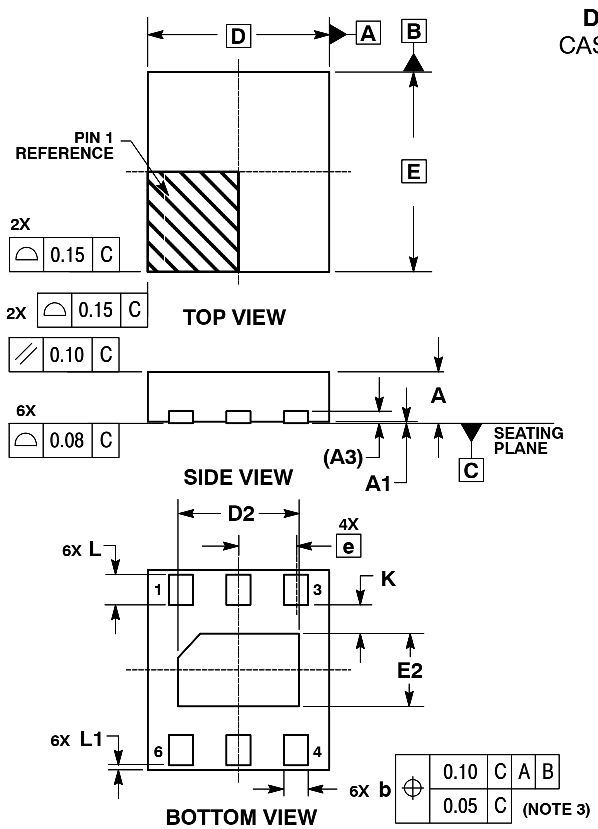
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3	0.127 REF		
b	0.20	0.25	0.30
D	2.00 BSC		
D2	1.40	1.50	1.60
E	2.20 BSC		
E2	0.70	0.80	0.90
e	0.50 BSC		
K	0.20	−−−	−−−
L	0.35	0.40	0.45

SOLDERING FOOTPRINT



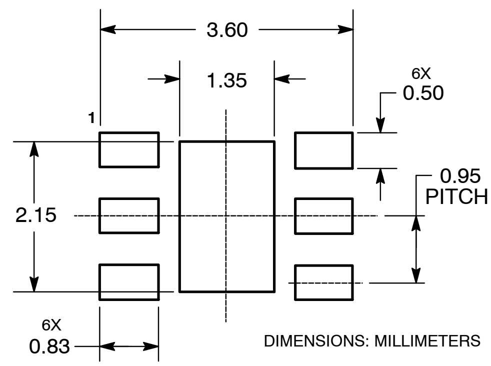
DFN6, 3x3.3
CASE 506AX−01
ISSUE O



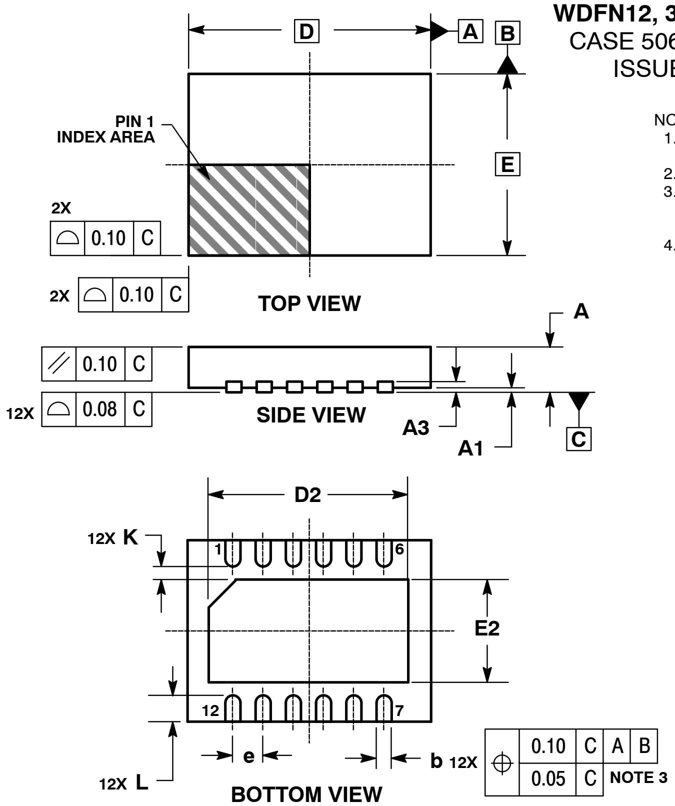
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	−−−	0.90
A1	0.00	−−−	0.05
A3	0.20 REF		
b	0.30	−−−	0.40
D	3.00 BSC		
D2	1.90	−−−	2.10
E	3.30 BSC		
E2	1.10	−−−	1.30
e	0.95 BSC		
K	0.20	−−−	−−−
L	0.40	−−−	0.60
L1	0.00	−−−	0.15

SOLDERING FOOTPRINT



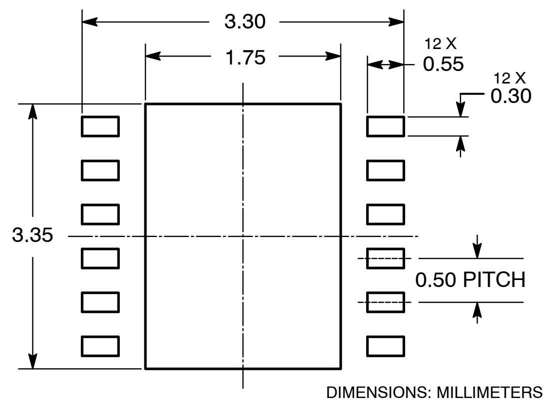
WDFN12, 3x4, 0.5P
CASE 506AY−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

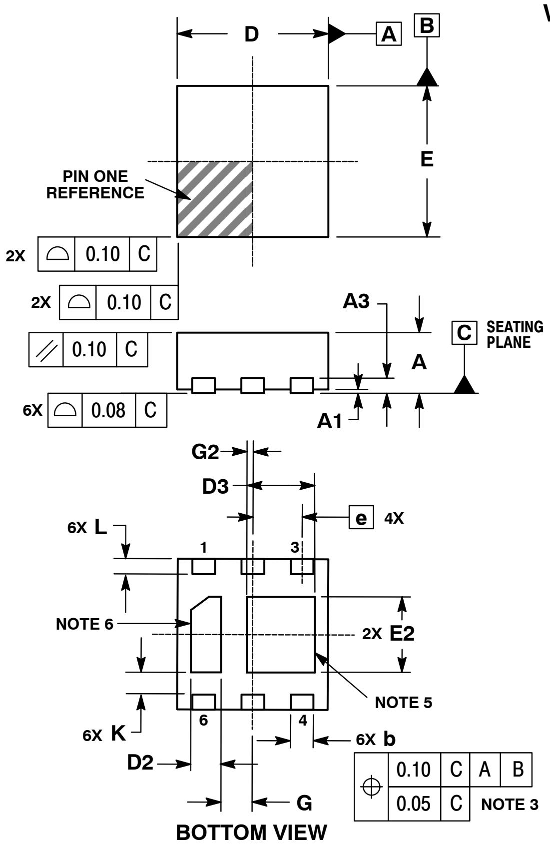
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	3.20	3.40
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

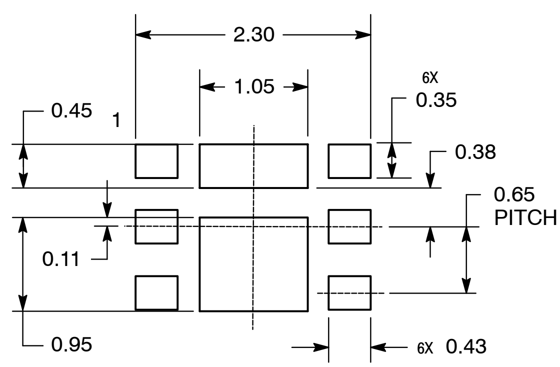
WDFN6, 2x2, 0.65P
CASE 506AZ−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. PINS 2 & 3 CONNECTED TO LARGE FLAG.
6. PIN 6 CONNECTED TO SMALL FLAG.

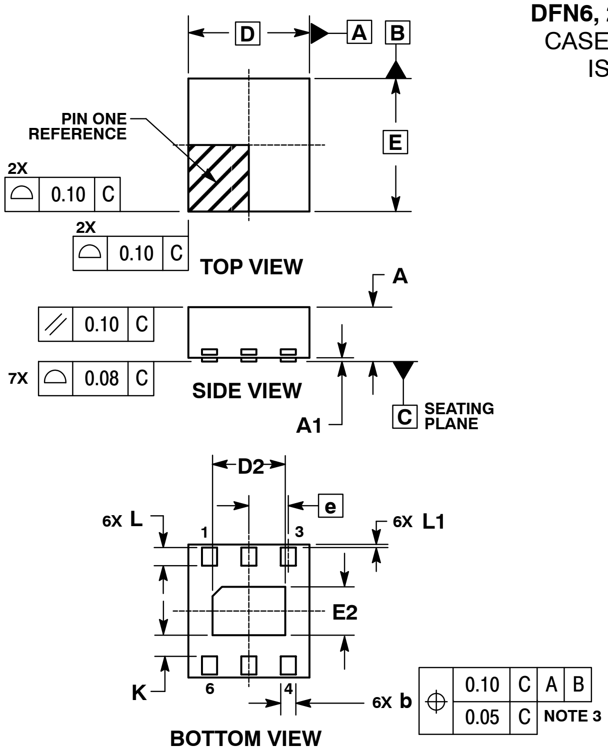
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.30	0.50
D3	0.80	1.00
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
G	0.41 REF	
G2	0.085 REF	
K	0.25 REF	
L	0.20	0.30

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

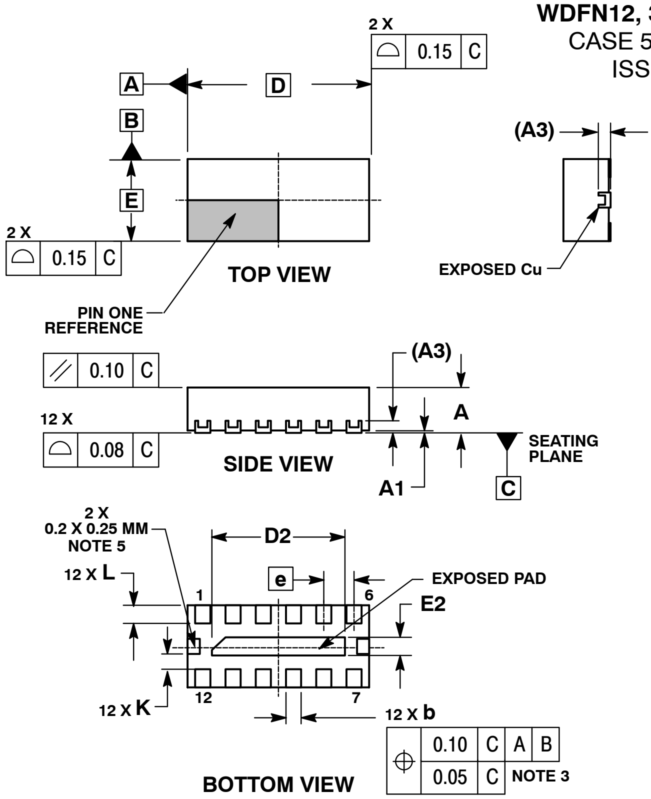
DFN6, 2x2.2, 0.65P
CASE 506BA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.20 BSC	
E2	0.70	0.90
e	0.65 BSC	
K	0.20	---
L	0.25	0.35
L1	0.00	0.10

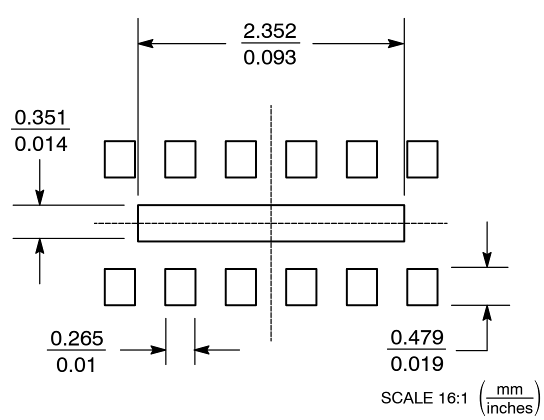
WDFN12, 3x1.35, 0.5P
CASE 506BB−01
ISSUE O



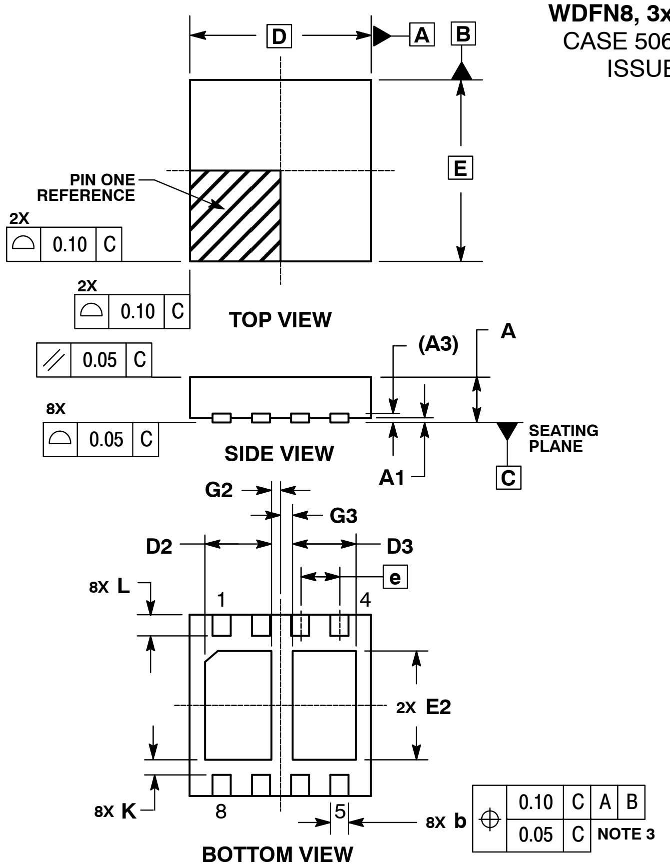
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	2.10	2.30
E	1.35 BSC	
E2	0.20	0.40
e	0.50 BSC	
K	0.20	---
L	0.20	0.40

SOLDERING FOOTPRINT



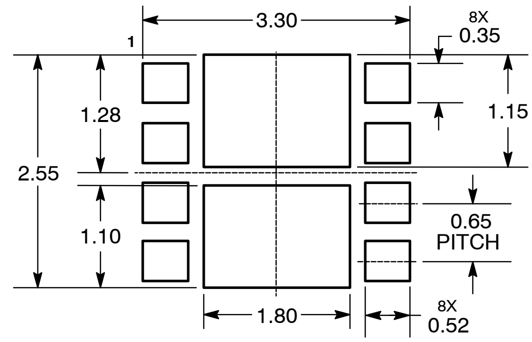
WDFN8, 3x3, 0.65P
CASE 506BC−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

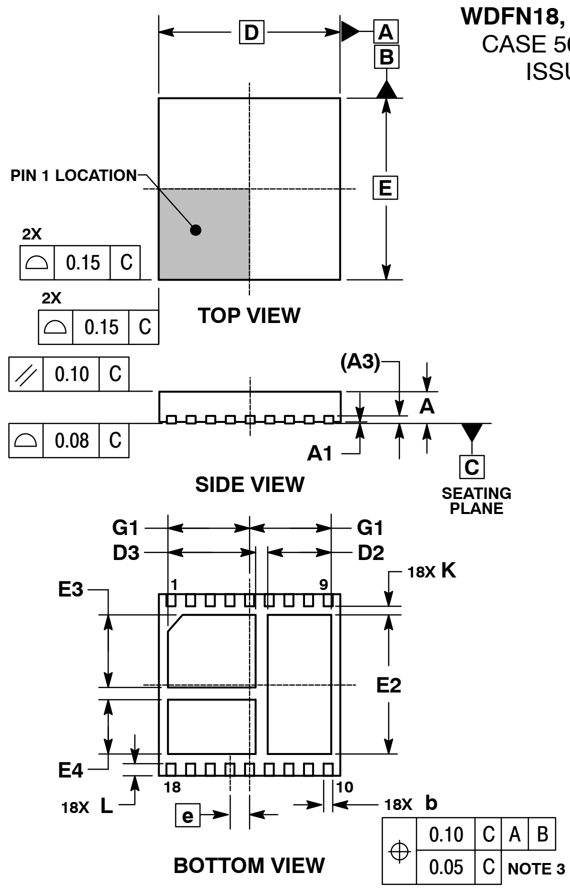
	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	1.00	1.20
D3	0.95	1.15
E	3.00 BSC	
E2	1.70	1.90
e	0.65 BSC	
G2	0.15 REF	
G3	0.20 REF	
K	0.20	---
L	0.25	0.45

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

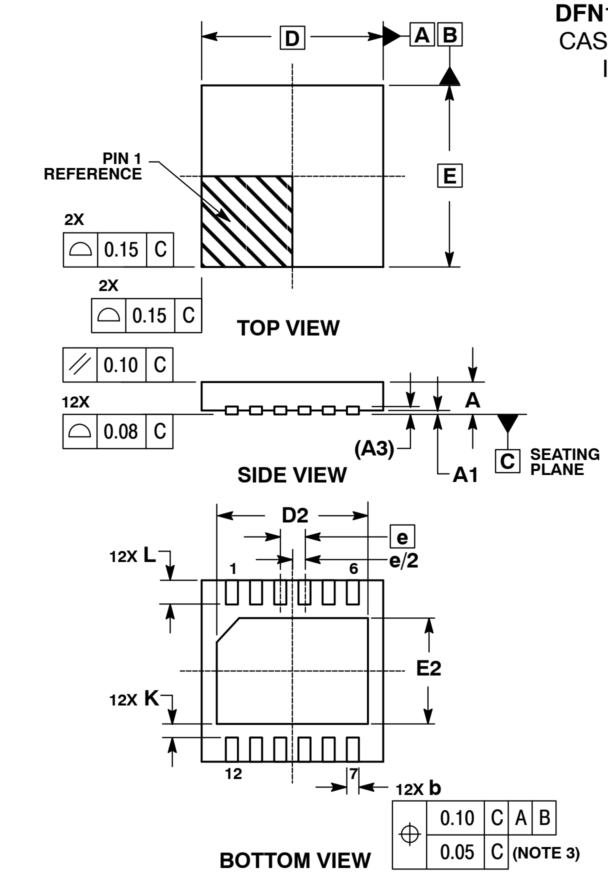
WDFN18, 6x6, 0.65P
CASE 506BD−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	6.00 BSC	
D2	2.05	2.15
D3	2.85	2.95
E	6.00 BSC	
E2	4.55	4.65
E3	2.35	2.45
E4	1.80	1.90
e	0.65 BSC	
G1	2.65	2.75
K	0.20 MIN	
L	0.35	0.45

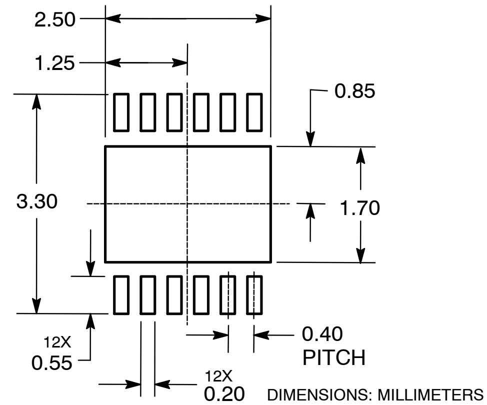
DFN12, 3x3, 0.4P
CASE 506BE−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

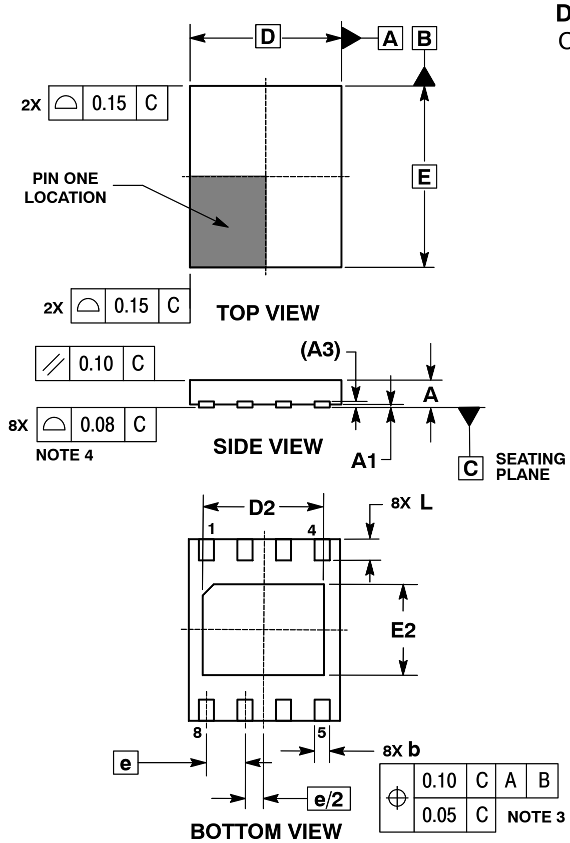
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF	
b	0.15	0.25
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.70	1.80
e	0.40 BSC	
K	0.15	−−−
L	0.30	0.50

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

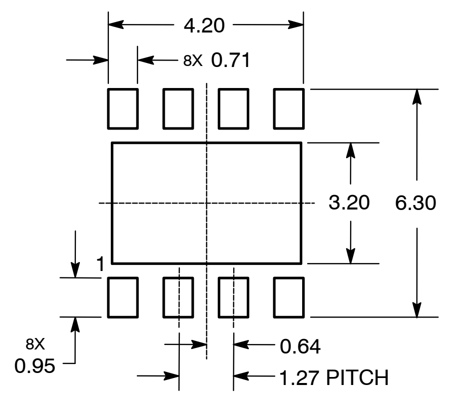
DFN8, 5x6, 1.27P
CASE 506BG−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

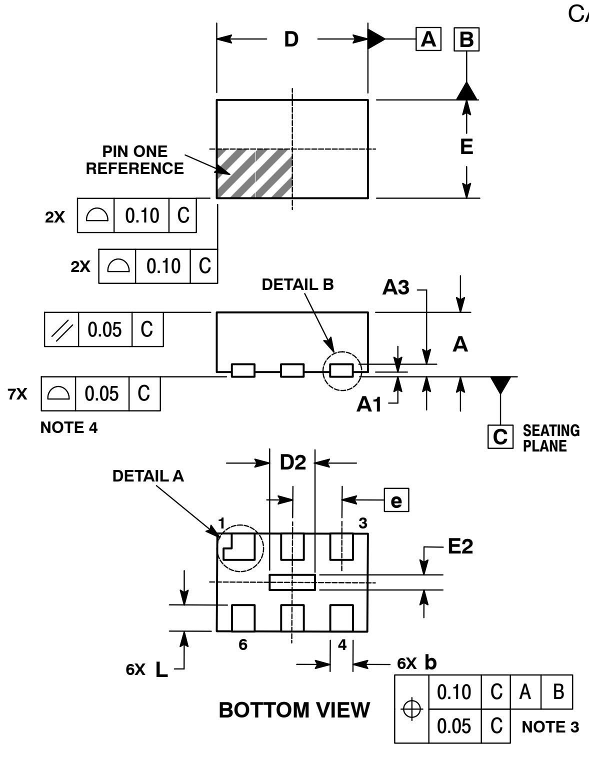
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.45	0.55
D	5.00 BSC	
D2	3.90	4.10
E	6.00 BSC	
E2	2.90	3.10
e	1.27 BSC	
L	0.60	0.80

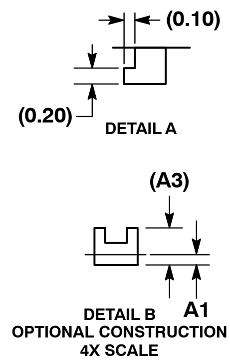
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DFN6, 2x1.3, 0.65P
CASE 506BH−01
ISSUE O

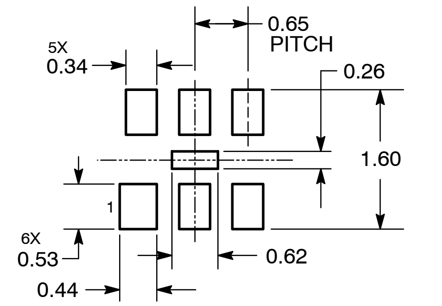




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

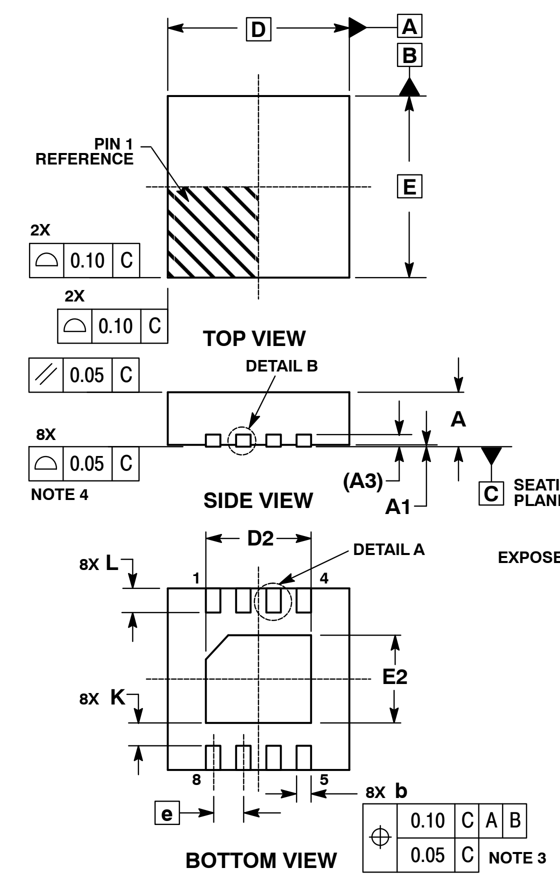
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	----	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	2.00 BSC		
D2	0.55	0.60	0.65
E	1.30 BSC		
E2	0.15	0.20	0.25
e	0.65 BSC		
L	0.25	0.35	0.45

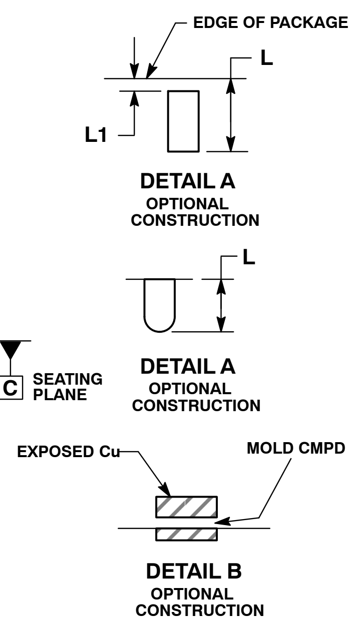
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DFN8, 3x3, 0.5P
CASE 506BJ−01
ISSUE O

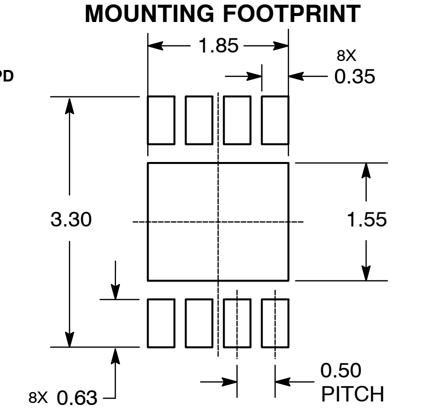




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

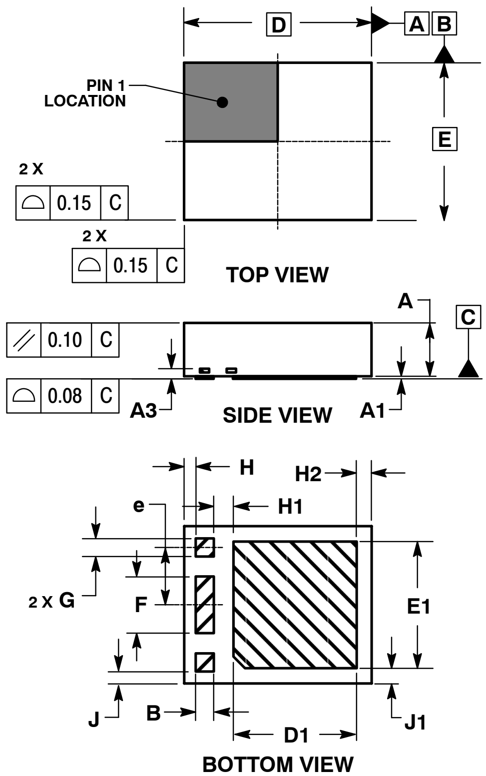
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.64	1.84
E	3.00 BSC	
E2	1.35	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

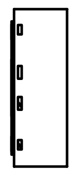
MOUNTING FOOTPRINT



DIMENSION: MILLIMETERS

PLLP−4
CASE 508AA−01
ISSUE O

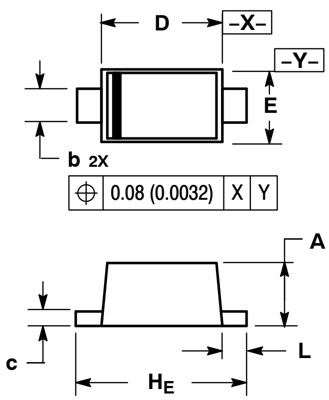




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOLERANCES: ±0.10 MM.

	MILLIMETERS	
DIM	MIN	MAX
A	1.750	1.950
A1	0.000	0.050
A3	0.254 REF	
B	0.500	0.700
D	6.200 BSC	
D1	3.979	4.179
E	5.200 BSC	
E1	4.087	4.287
e	1.905 BSC	
F	1.860	1.880
G	0.500	0.700
H	0.379 REF	
H1	0.635 REF	
H2	0.507 REF	
J	0.404 REF	
J1	0.507 REF	

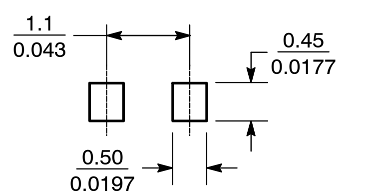
SOD−723
CASE 509AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.49	0.52	0.55	0.019	0.020	0.022
b	0.25	0.28	0.32	0.0098	0.011	0.013
c	0.08	0.12	0.15	0.0032	0.0047	0.0059
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.55	0.60	0.65	0.022	0.024	0.026
H_E	1.35	1.40	1.45	0.053	0.055	0.057
L	0.15	0.20	0.25	0.006	0.0079	0.010

SOLDERING FOOTPRINT

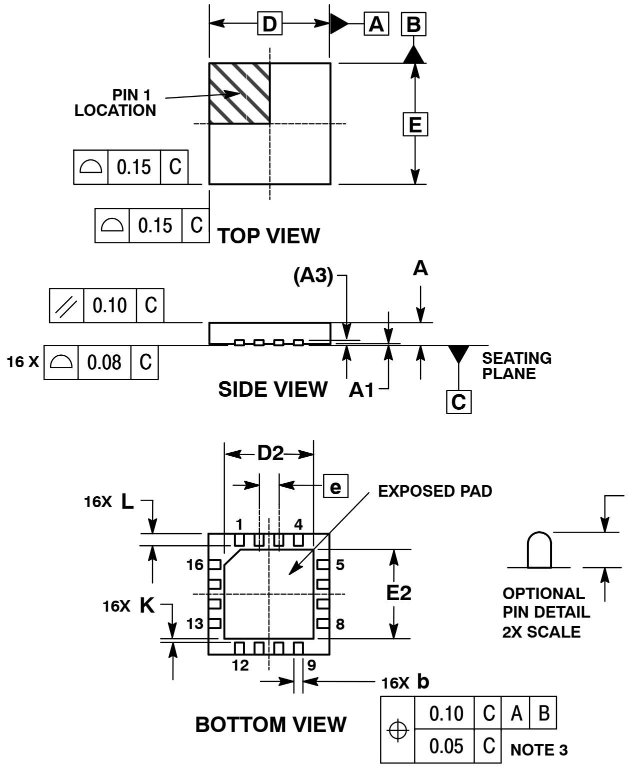


SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

WQFN16, 4x4

CASE 510AB−01

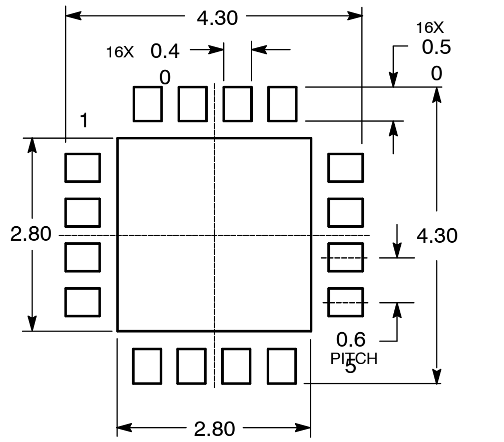
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.65 BSC	
K	0.20	---
L	0.30	0.50

SOLDERMASK DEFINED SOLDERING FOOTPRINT*

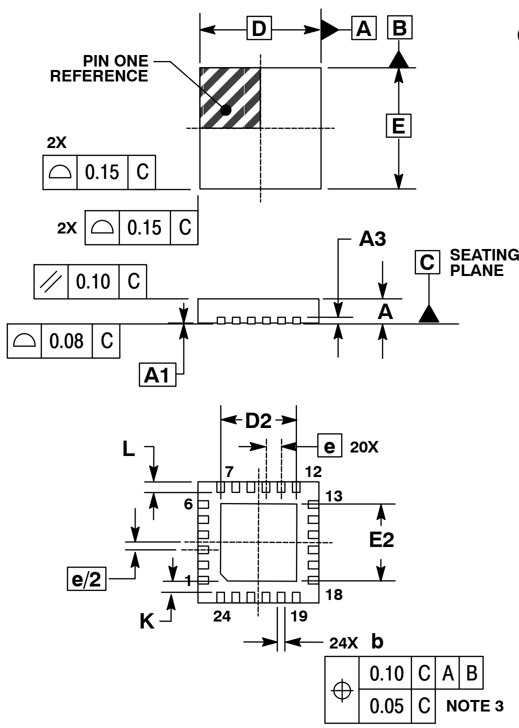


DIMENSIONS: MILLIMETERS

QFN24, 4x4

CASE 511AA−01

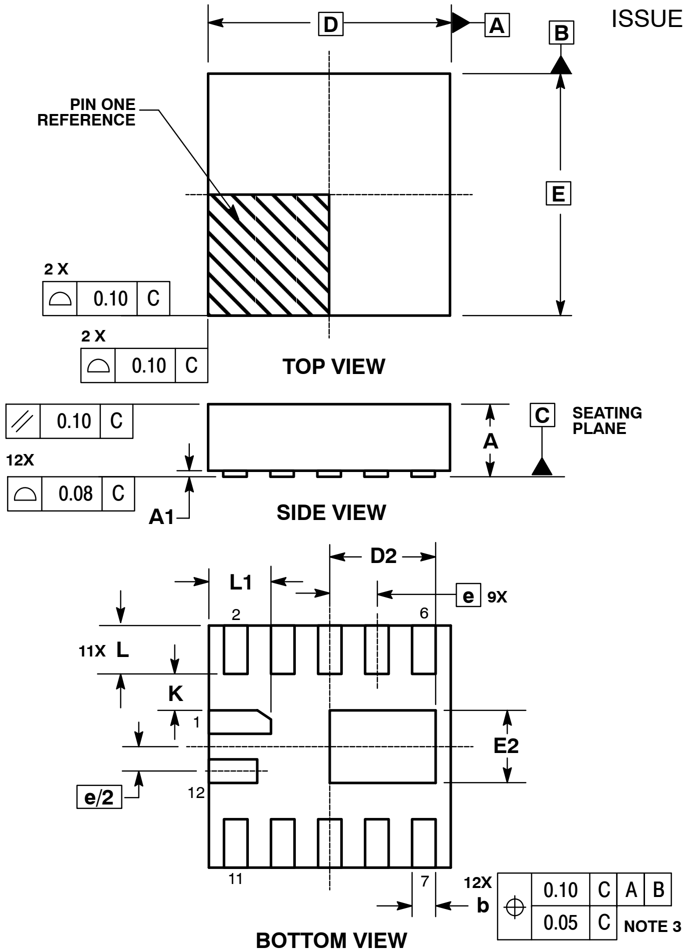
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.40	2.50	2.60
E	4.00 BSC		
E2	2.40	2.50	2.60
e	0.50 BSC		
K	0.20	---	---
L	0.30	0.40	0.50

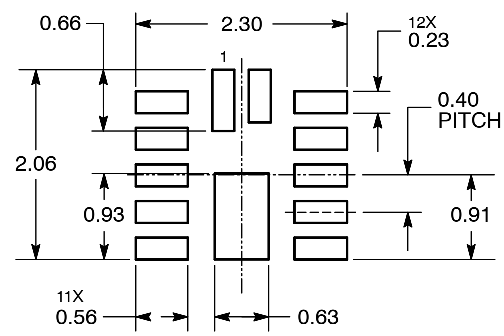
LLGA12, 2x2
CASE 513AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

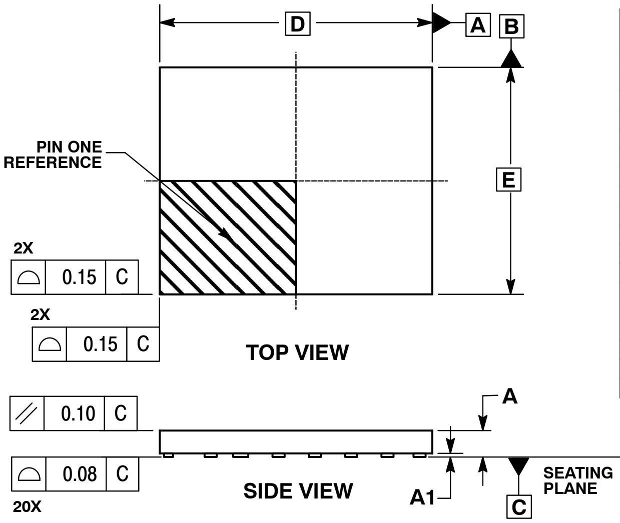
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.15	0.25
D	2.00 BSC	
D2	0.80	1.00
E	2.00 BSC	
E2	0.55	0.65
e	0.40 BSC	
K	0.25	---
L	0.30	0.50
L1	0.40	0.60

SOLDERING FOOTPRINT



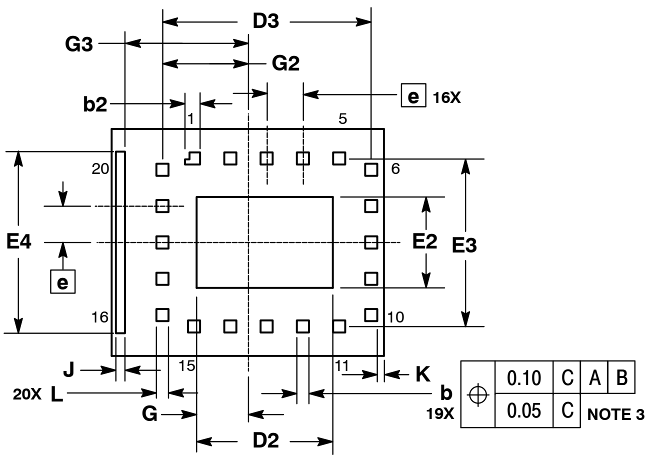
DIMENSIONS: MILLIMETERS

TLLGA20, 6x5
CASE 513AC−01
ISSUE A

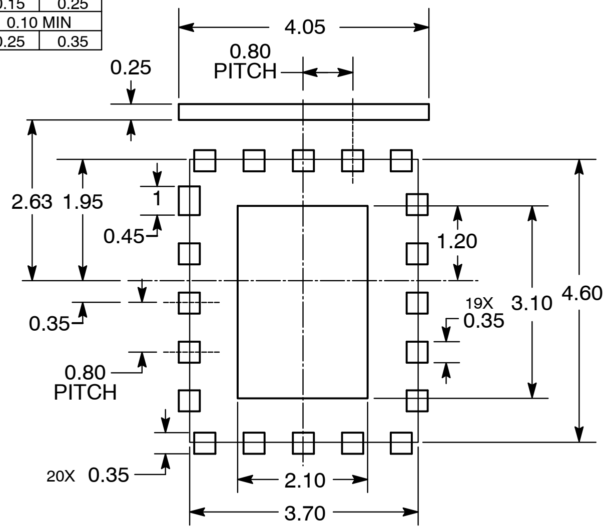


DIM	MILLIMETERS MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.25	0.35
b2	0.35	0.45
D	6.00 BSC	
D2	2.90	3.10
D3	4.60 BSC	
E	5.00 BSC	
E2	1.90	2.10
E3	3.70 BSC	
E4	3.90	4.10
e	0.80 BSC	
G	1.05	1.25
G2	1.95 BSC	
G	2.55	2.75
J	0.15	0.25
K	0.10 MIN	
L	0.25	0.35

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

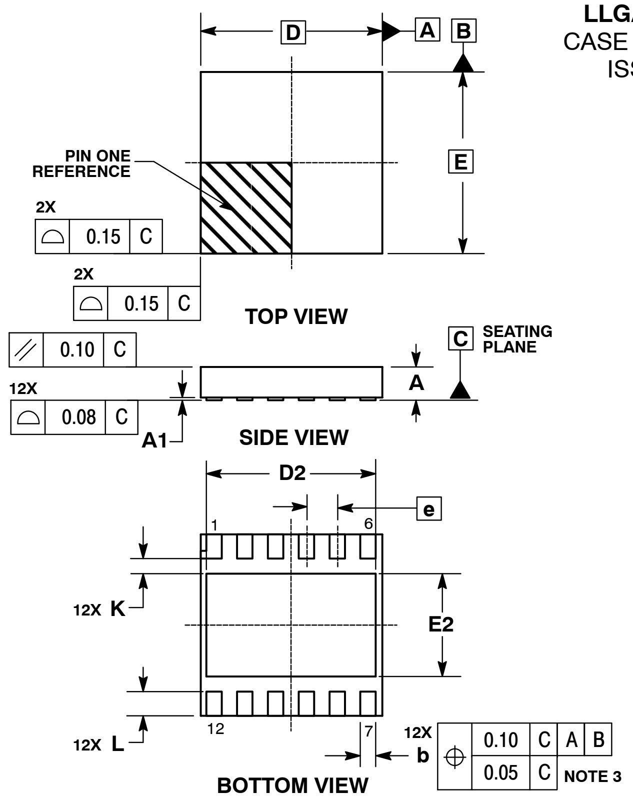


SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

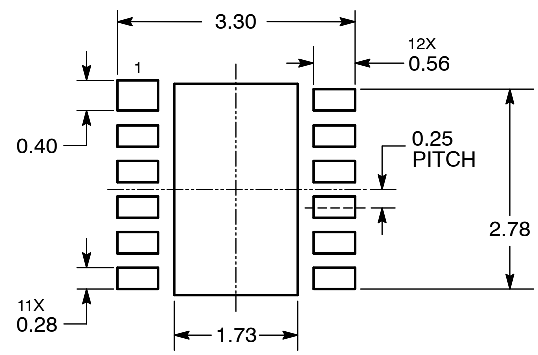
LLGA12, 3x3
CASE 513AD−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

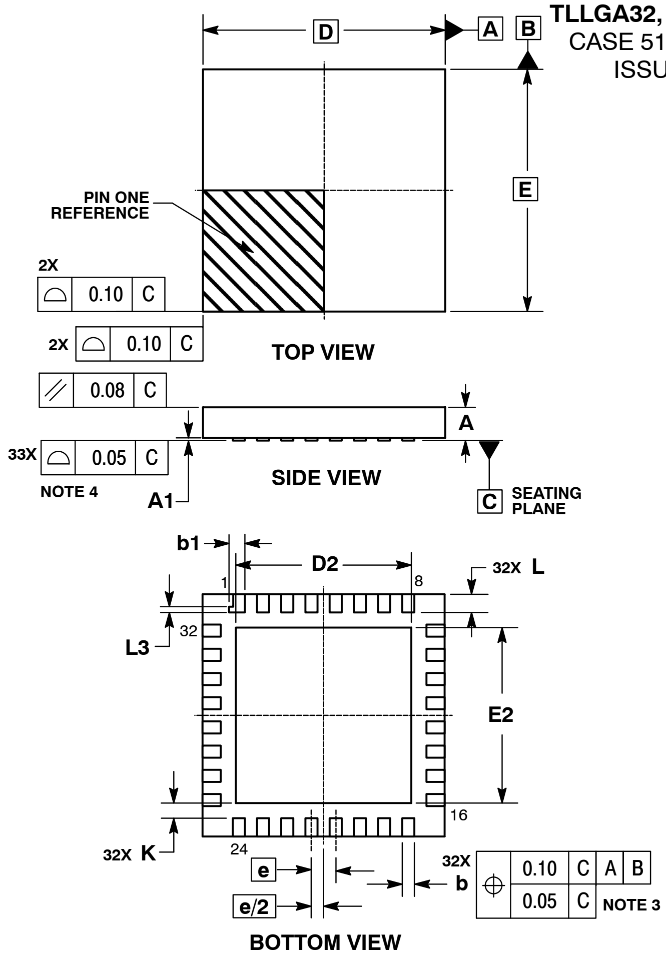
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	2.75	2.85
E	3.00 BSC	
E2	1.65	1.75
e	0.50 BSC	
K	0.20	−−−
L	0.35	0.45

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

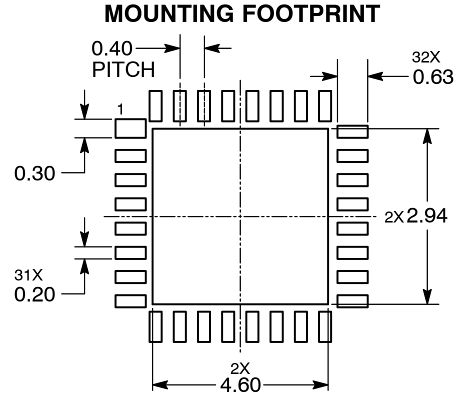
TLLGA32, 4x4, 0.4P
CASE 513AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

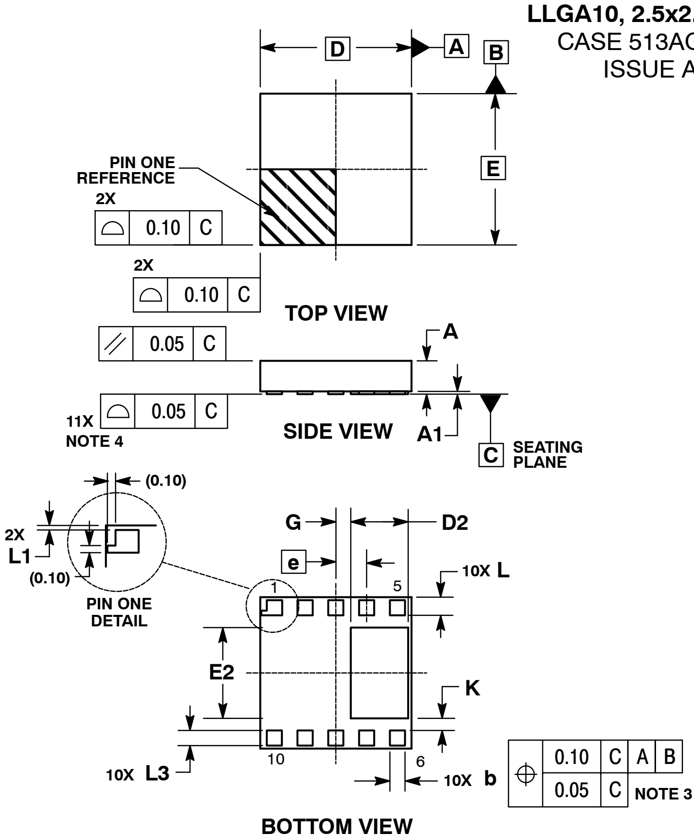
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.15	0.25
b1	0.30 REF	
D	4.00 BSC	
D2	2.80	3.00
E	4.00 BSC	
E2	2.80	3.00
e	0.40 BSC	
K	0.20	−−−
L	0.20	0.40
L3	0.10 REF	

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

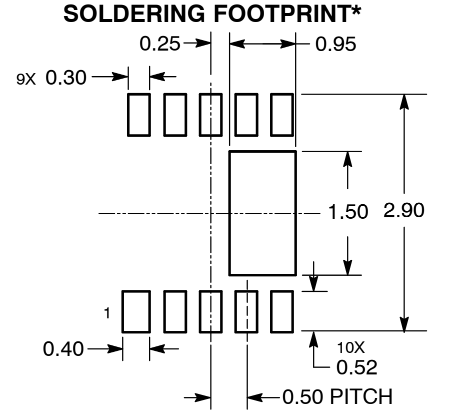
LLGA10, 2.5x2.5, 0.5P
CASE 513AG−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

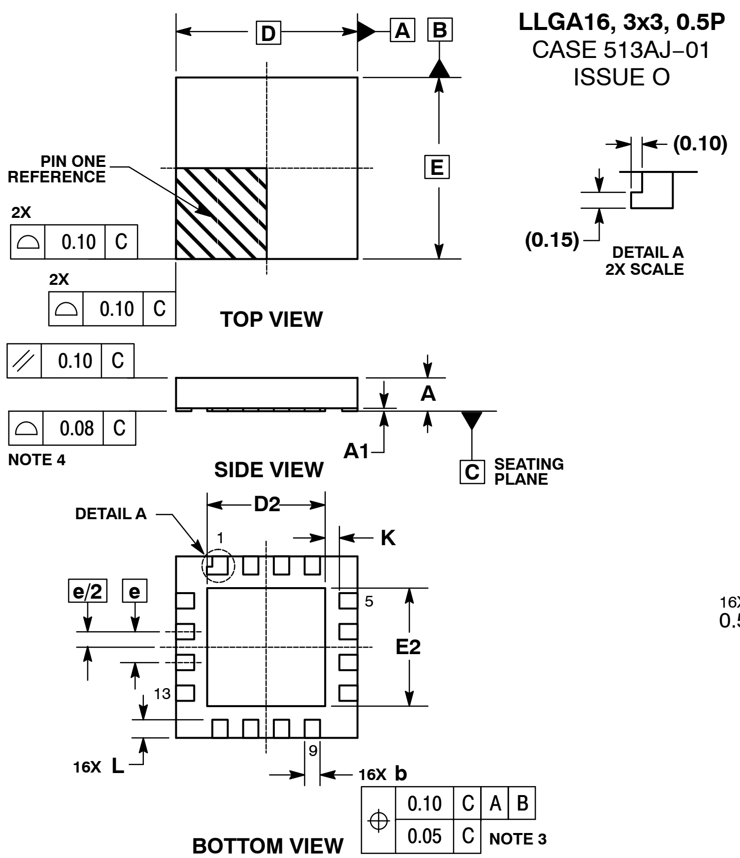
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	2.50 BSC	
D2	0.90	1.00
E	2.50 BSC	
E2	1.45	1.55
e	0.50 BSC	
G	0.20	0.30
K	0.20	−−−
L	0.30 REF	
L1	0.05 BSC	
L3	0.20	0.30

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

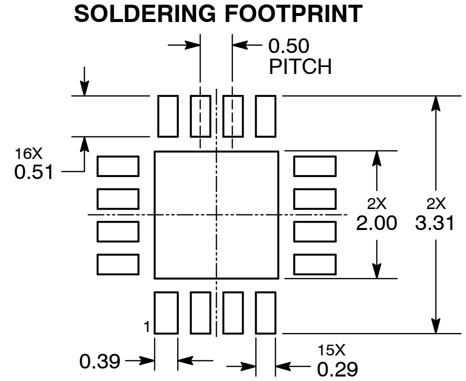
LLGA16, 3x3, 0.5P
CASE 513AJ−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

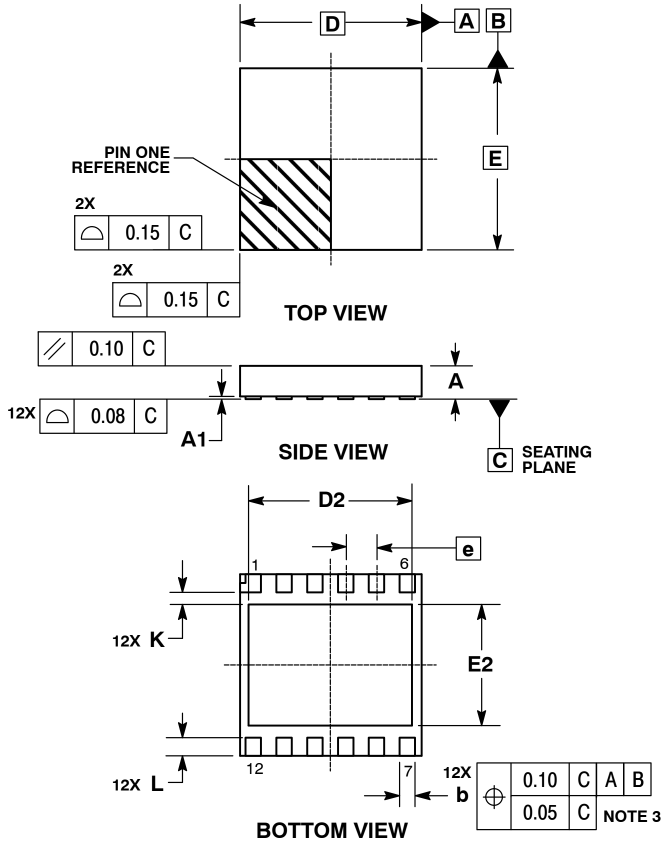
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	1.90	2.00
E	3.00 BSC	
E2	1.90	2.00
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

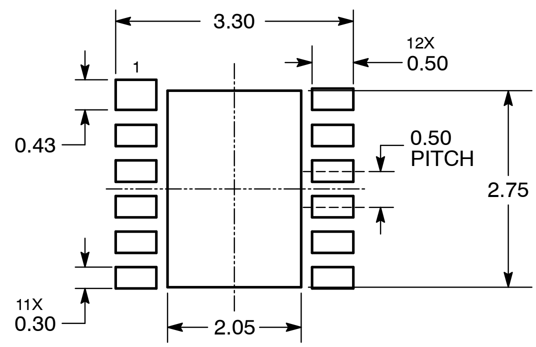
LLGA12, 3x3, 0.5P
CASE 513AK−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

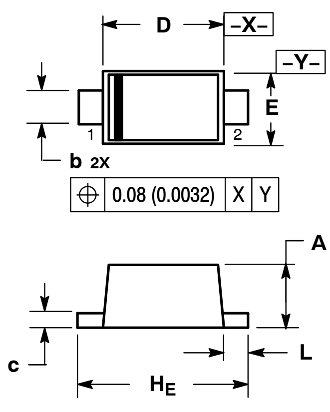
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.20	0.30
D	3.00 BSC	
D2	2.60	2.80
E	3.00 BSC	
E2	1.90	2.10
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

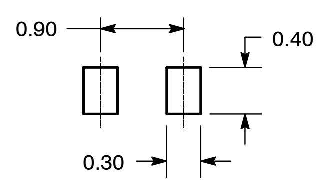
SOD−923
CASE 514AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

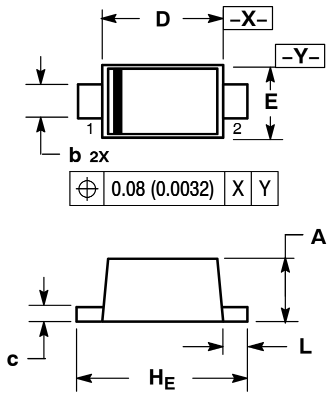
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.39	0.43	0.013	0.015	0.017
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H_E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

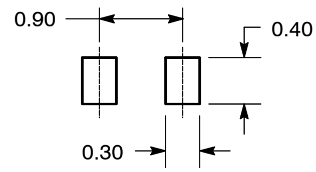
SOD−923
CASE 514AB−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

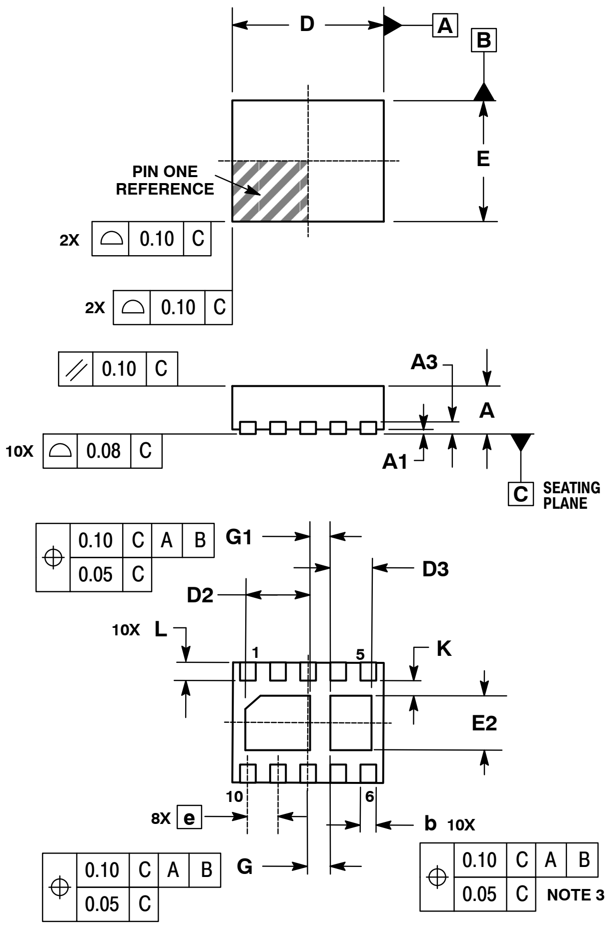
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
H_E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

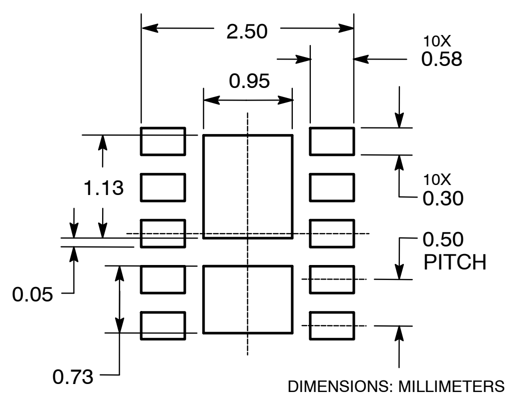
WDFN10, 2.5x2, 0.5P
CASE 516AA−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

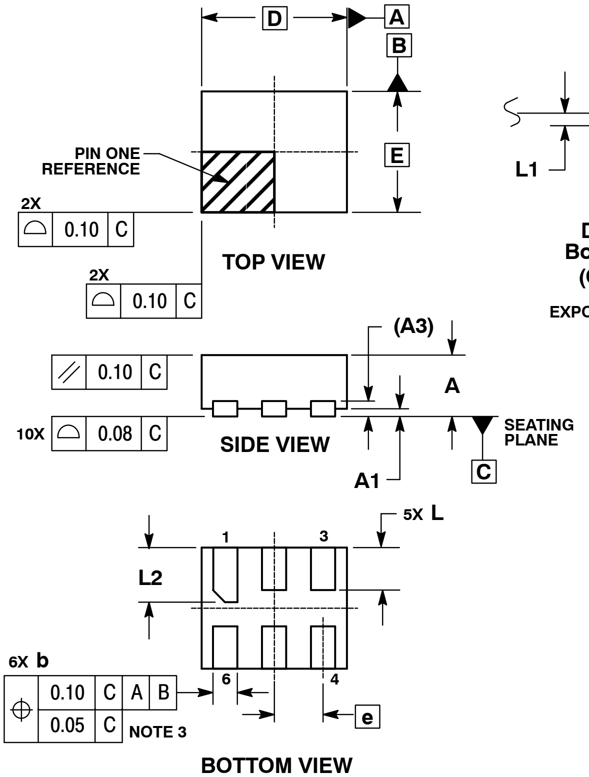
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.50 BSC		
D2	0.97	1.08	1.18
D3	0.57	0.68	0.78
e	0.50 BSC		
E	2.00 BSC		
E2	0.80	0.90	1.00
G	0.375 BSC		
G1	0.35 BSC		
K	0.20	---	---
L	0.20	0.30	0.40

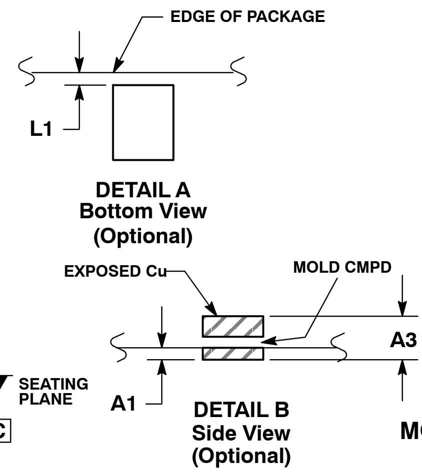
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

UDFN6, 1.2x1.0, 0.4P
CASE 517AA−01
ISSUE C

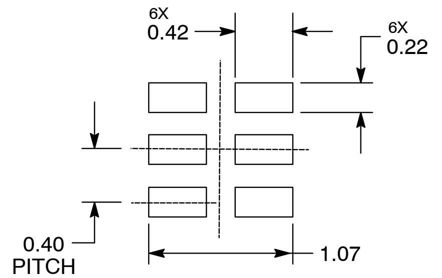




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

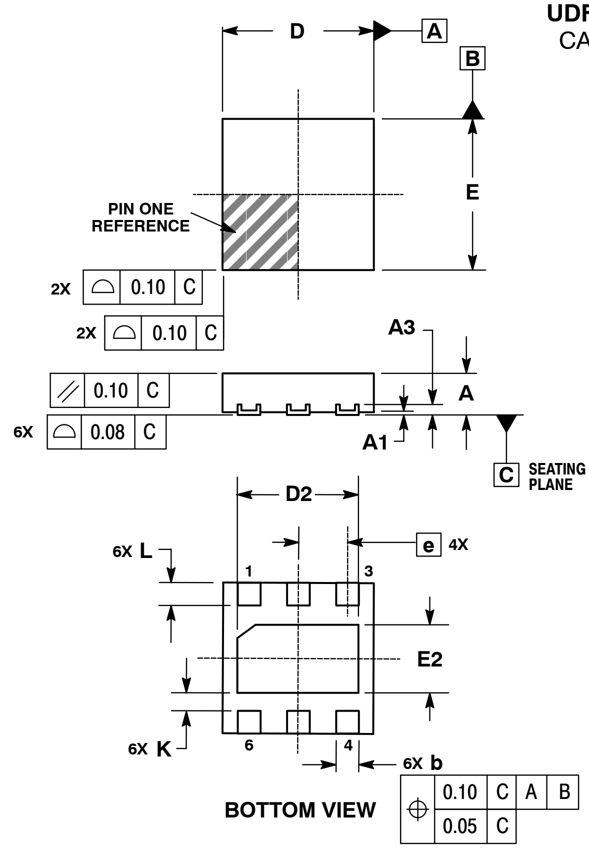
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.30	0.40
L1	0.00	0.15
L2	0.40	0.50

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

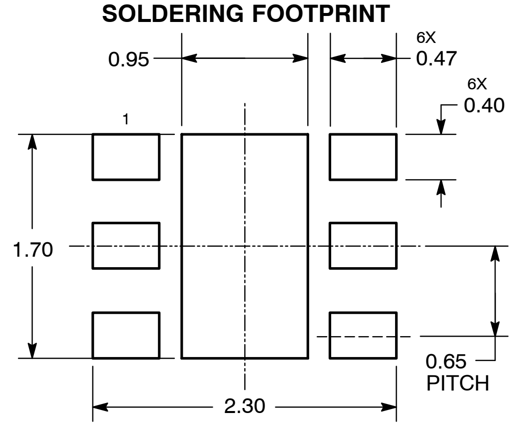
UDFN6, 2x2, 0.65P
CASE 517AB−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

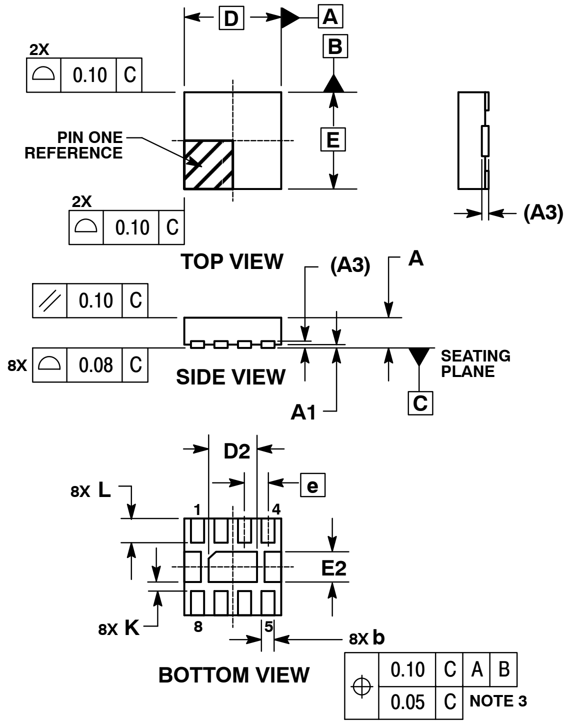
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.25	0.35
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.65 BSC	
K	0.20	---
L	0.25	0.35

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

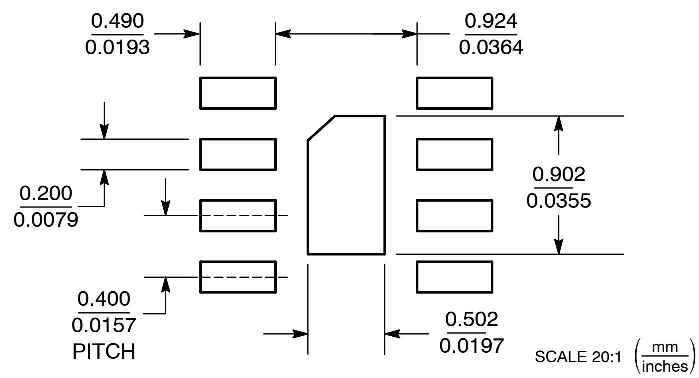
UDFN8, 1.6x1.6
CASE 517AC−01
ISSUE A



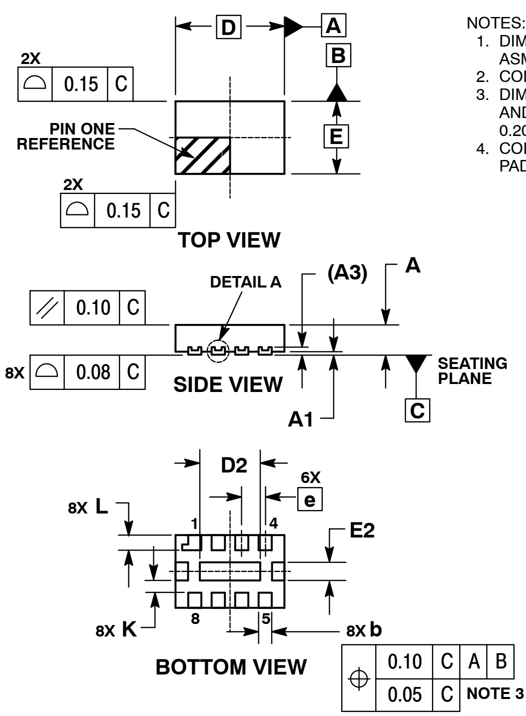
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3		0.127 REF	
b	0.15	0.20	0.25
D		1.60 BSC	
D2	0.70	0.80	0.90
E		1.60 BSC	
E2	0.40	0.50	0.60
e		0.40 BSC	
K	0.20	−−−	−−−
L	0.20	0.30	0.40

SOLDERING FOOTPRINT

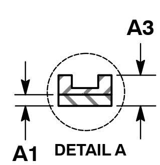


UDFN8, 1.8x1.2, 0.4P
CASE 517AD−01
ISSUE A

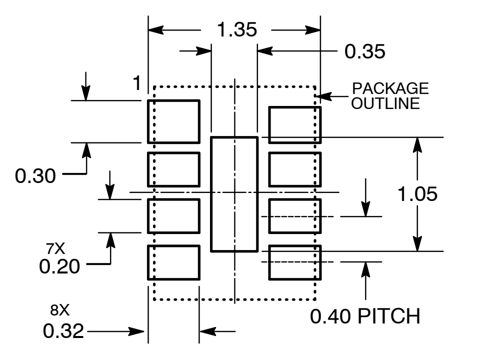


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3		0.127 REF	
b	0.15	0.20	0.25
D		1.80 BSC	
D2	0.90	1.00	1.10
E		1.20 BSC	
E2	0.20	0.30	0.40
e		0.40 BSC	
K	0.20	−−−	−−−
L	0.20	0.25	0.30

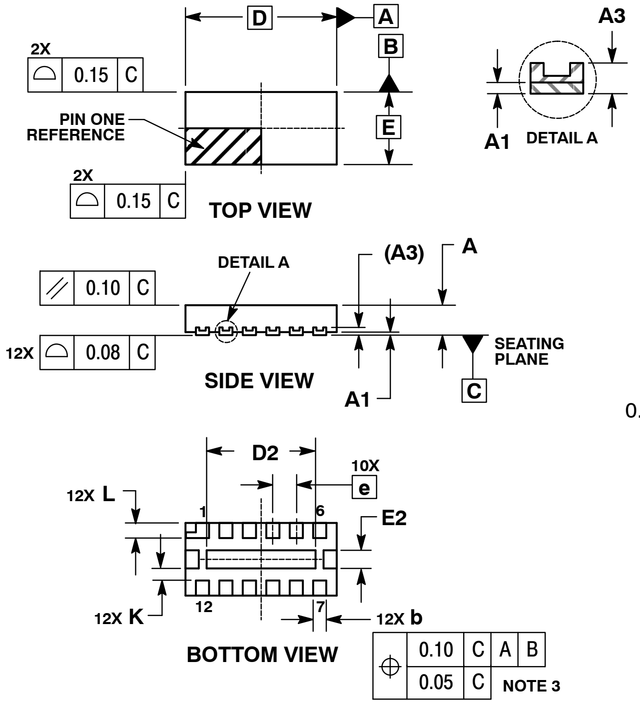


SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

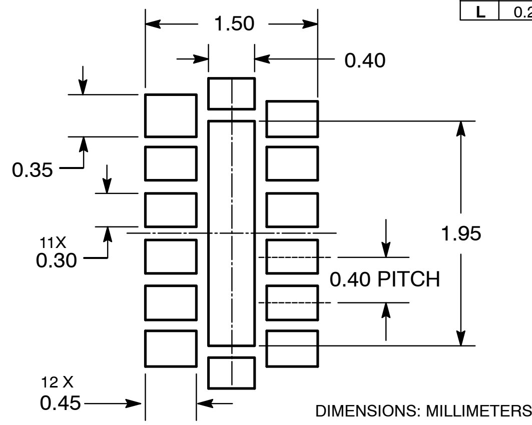
UDFN12, 2.5x1.2
CASE 517AE−01
ISSUE O



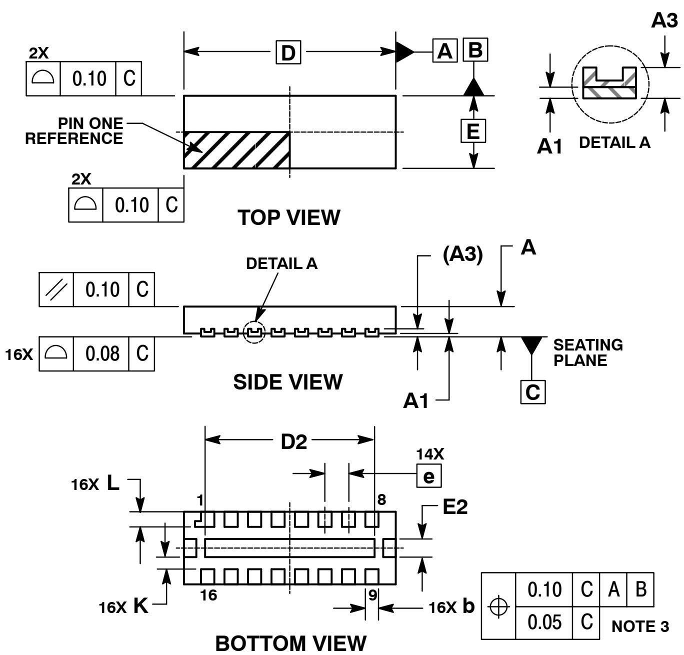
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3	0.127 REF		
b	0.15	0.20	0.25
D	2.50 BSC		
D2	1.70	1.80	1.90
E	1.20 BSC		
E2	0.20	0.30	0.40
e	0.40 BSC		
K	0.20	---	---
L	0.20	0.25	0.30

SOLDERING FOOTPRINT



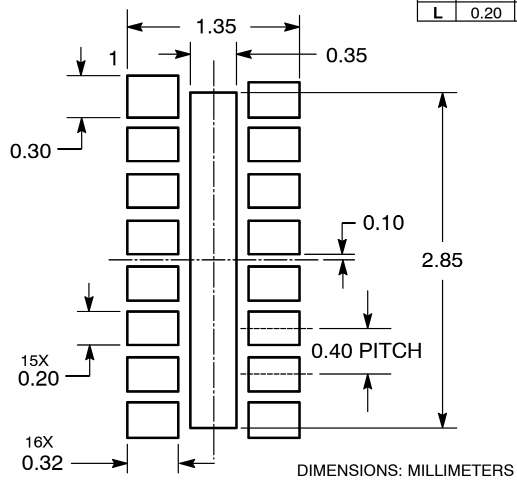
UDFN16, 3.5x1.2
CASE 517AF−01
ISSUE B



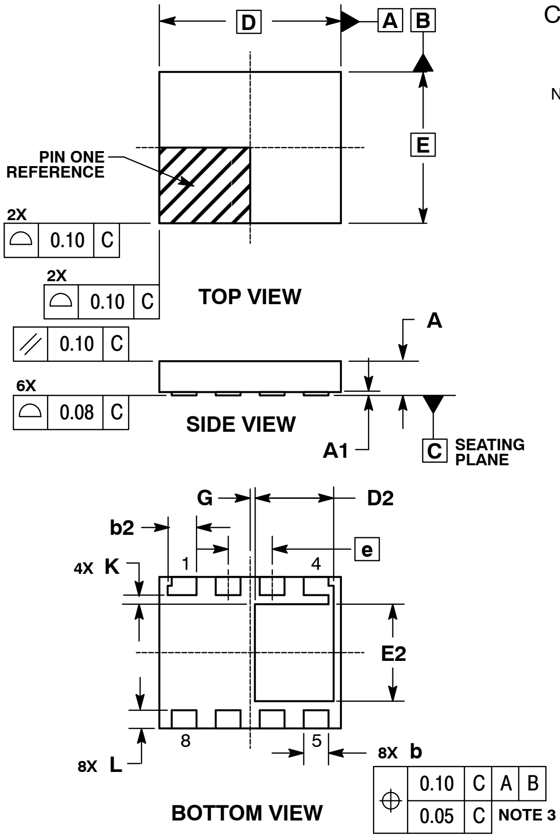
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.00	0.03	0.05
A3	0.127 REF		
b	0.15	0.20	0.25
D	3.50 BSC		
D2	2.70	2.80	2.90
E	1.20 BSC		
E2	0.20	0.30	0.40
e	0.40 BSC		
K	0.20	---	---
L	0.20	0.25	0.30

SOLDERING FOOTPRINT



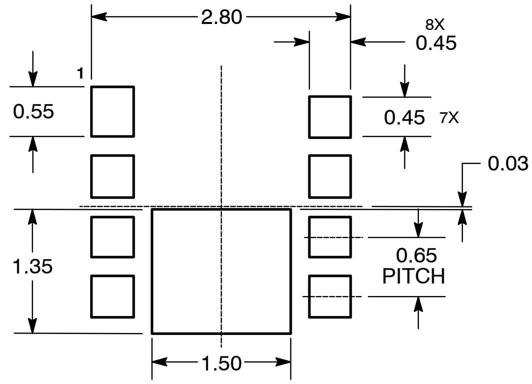
LLGA8, 3x2.5, 0.5P
CASE 517AH−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

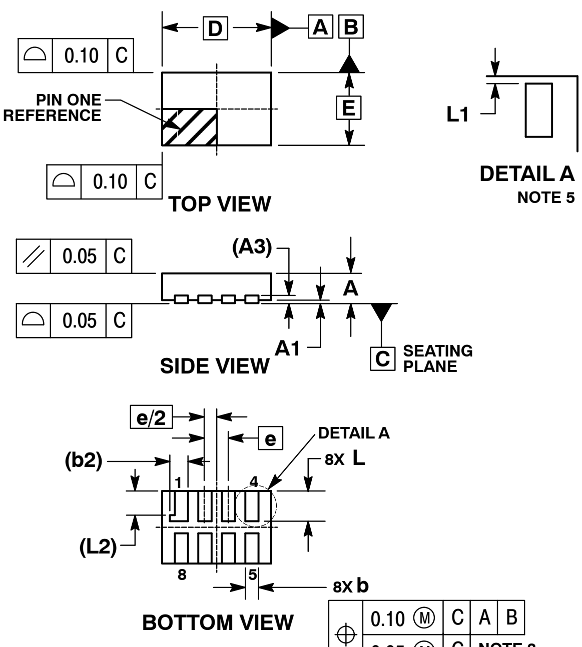
	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.35	0.45
b2	0.45	0.55
D	3.00 BSC	
D2	1.25	1.35
E	2.50 BSC	
E2	1.55	1.65
e	0.65 BSC	
G	0.05 REF	
K	0.15 REF	
L	0.35	0.45

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

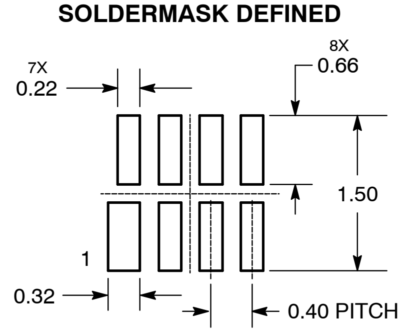
UDFN8, 1.8x1.2, 0.4P
CASE 517AJ−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

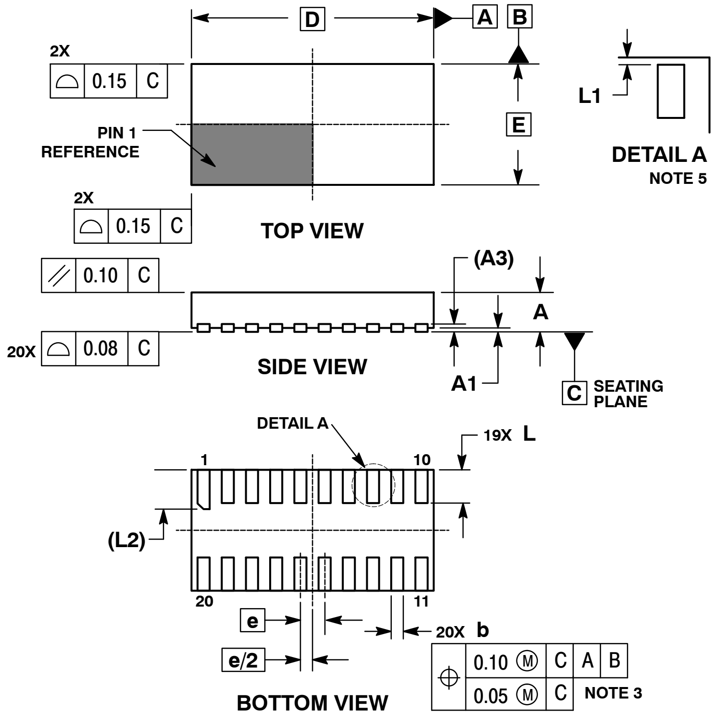
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
b2	0.30 REF	
D	1.80 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.45	0.55
L1	0.00	0.03
L2	0.40 REF	

MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

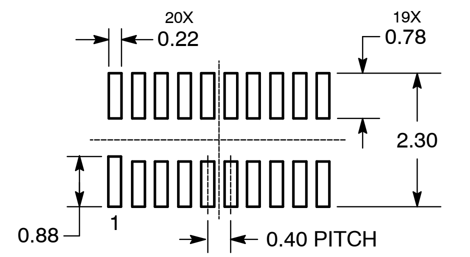
UDFN20, 4x2, 0.4P
CASE 517AK−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH MAY NOT EXCEED 0.03 ONTO BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

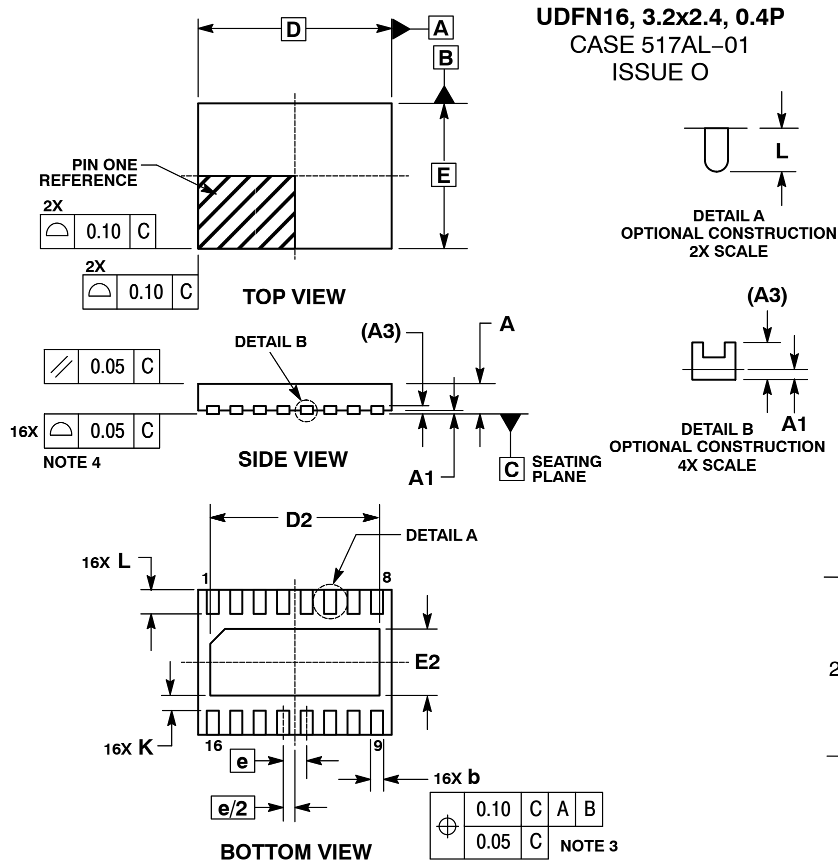
DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	4.00 BSC	
E	2.00 BSC	
e	0.40 BSC	
L	0.50	0.60
L1	0.00	0.03
L2	0.60	0.70

MOUNTING FOOTPRINT SOLDERMASK DEFINED



DIMENSIONS: MILLIMETERS

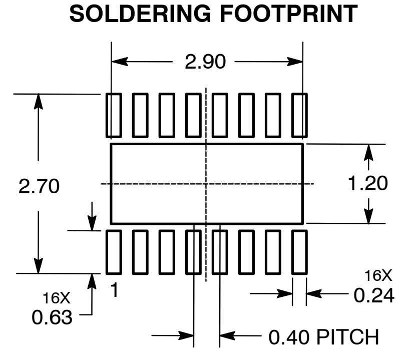
UDFN16, 3.2x2.4, 0.4P
CASE 517AL−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.20 BSC	
D2	2.70	2.90
E	2.40 BSC	
E2	1.00	1.20
e	0.40 BSC	
K	0.20	−−−
L	0.30	0.50

SOLDERING FOOTPRINT

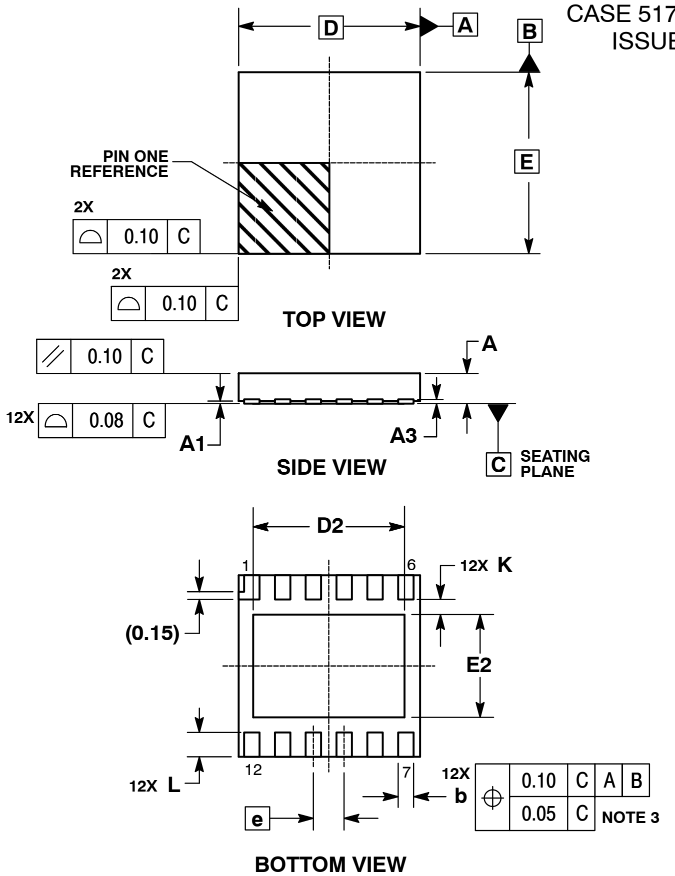


DIMENSIONS: MILLIMETERS

UDFN12, 3x3, 0.5P

CASE 517AM−01

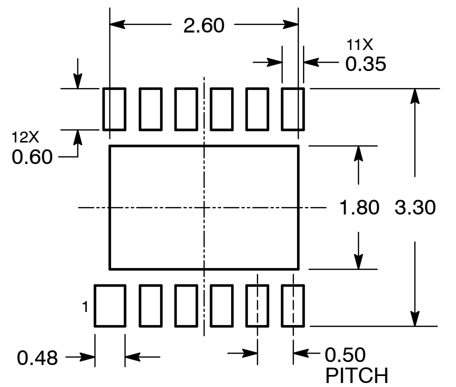
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.07 REF	
b	0.20	0.30
D	3.00 BSC	
D2	2.40	2.60
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

SOLDERING FOOTPRINT

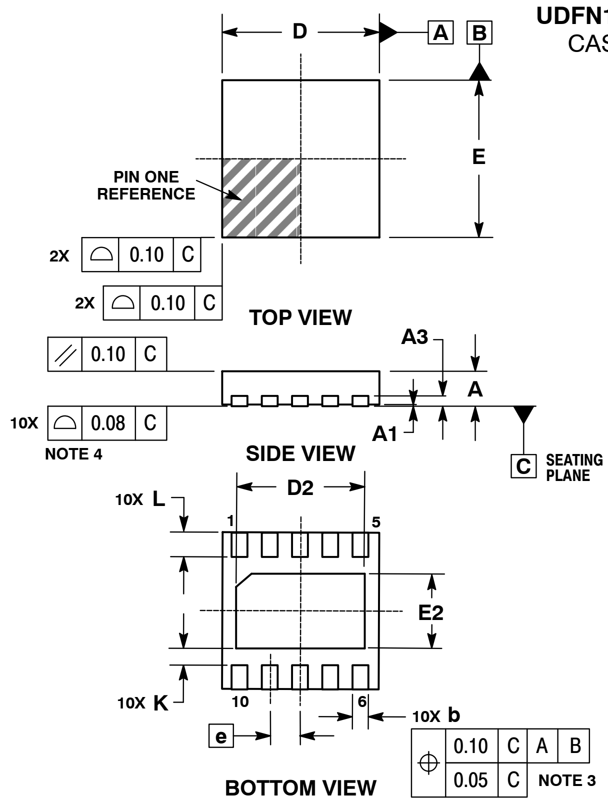


DIMENSIONS: MILLIMETERS

UDFN10, 2.6x2.6, 0.5P

CASE 517AN−01

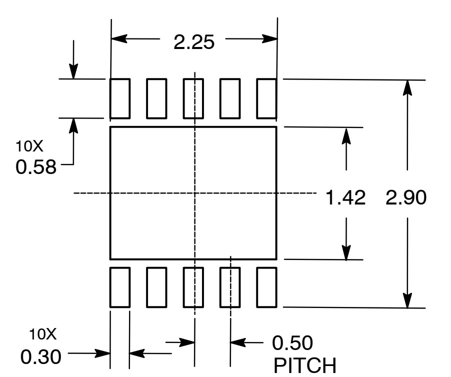
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

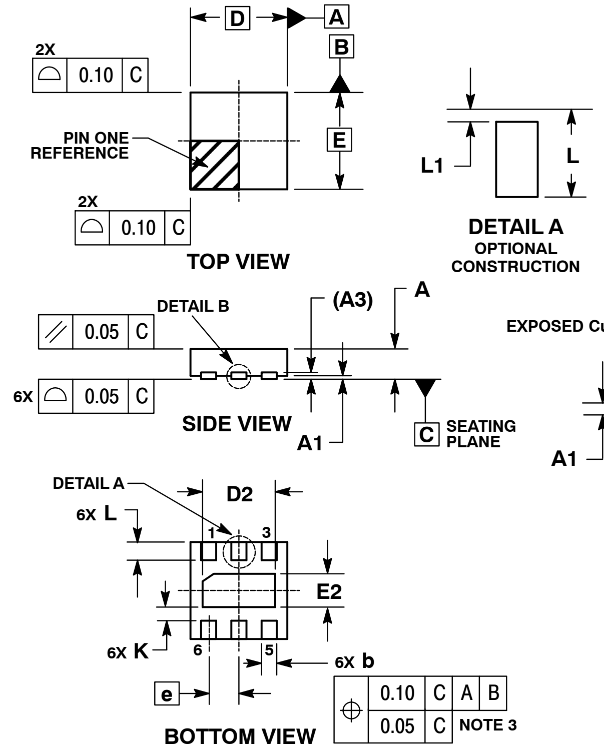
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	2.60 BSC	
D2	2.00	2.25
E	2.60 BSC	
E2	1.11	1.36
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.40

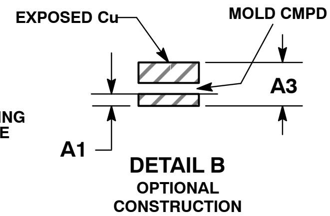
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

UDFN6, 1.6x1.6, 0.5P
CASE 517AP−01
ISSUE O

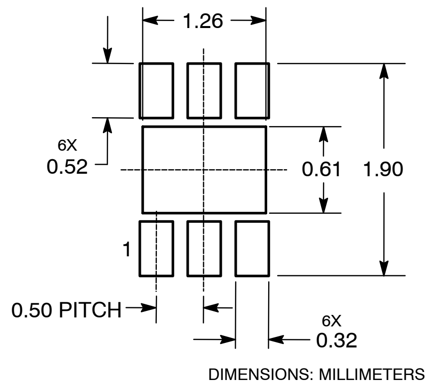




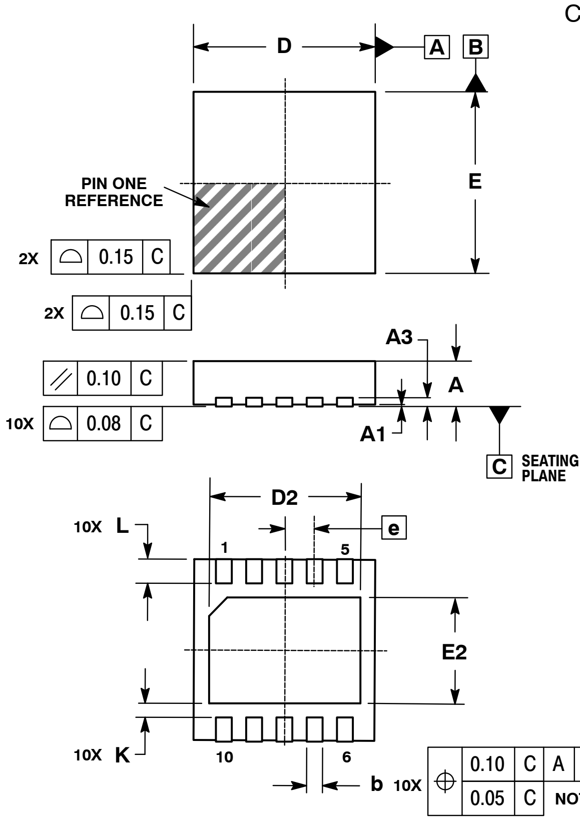
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
D2	1.10	1.30
E2	0.45	0.65
K	0.20	−−−
L	0.20	0.40
L1	0.00	0.15

MOUNTING FOOTPRINT*



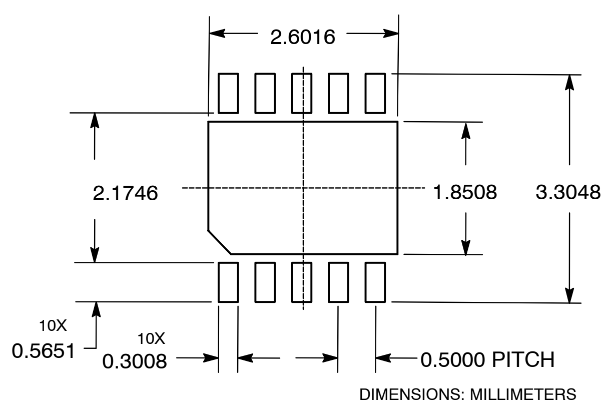
WDFN10, 3x3
CASE 522AA−01
ISSUE A



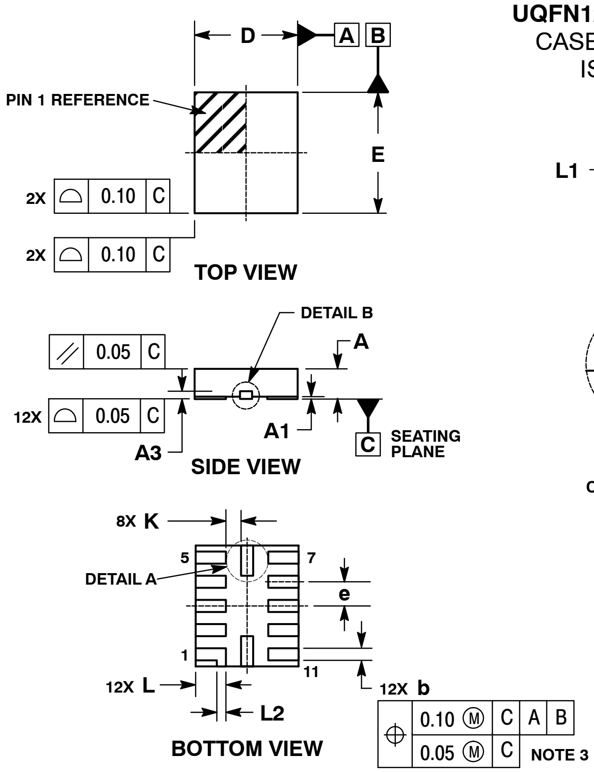
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

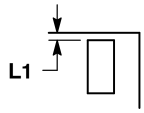
DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX
A	0.70	0.75	0.80
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	2.45	2.50	2.55
E	3.00 BSC		
E2	1.75	1.80	1.85
e	0.50 BSC		
K	0.19 TYP		
L	0.35	0.40	0.45

SOLDERING FOOTPRINT

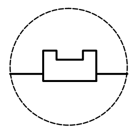


UQFN12, 1.7x2, 0.4P
CASE 523AE−01
ISSUE A





DETAIL A
NOTE 5

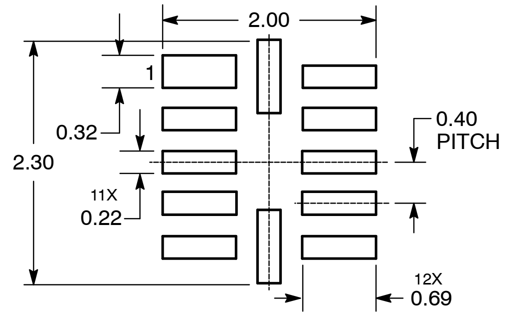


DETAIL B
OPTIONAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

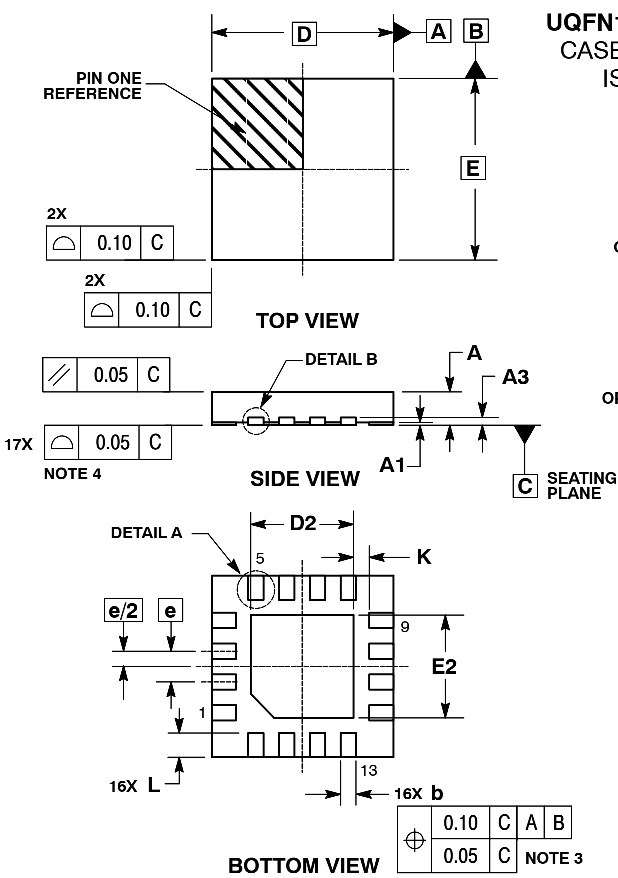
DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

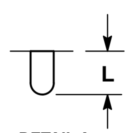
MOUNTING FOOTPRINT



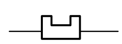
DIMENSIONS: MILLIMETERS

UQFN16, 3x3, 0.5P
CASE 523AF−01
ISSUE O





DETAIL A
OPTIONAL CONSTRUCTION
2X SCALE

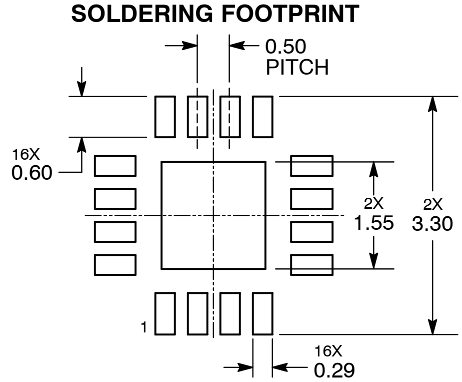


DETAIL B
OPTIONAL CONSTRUCTION
4X SCALE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

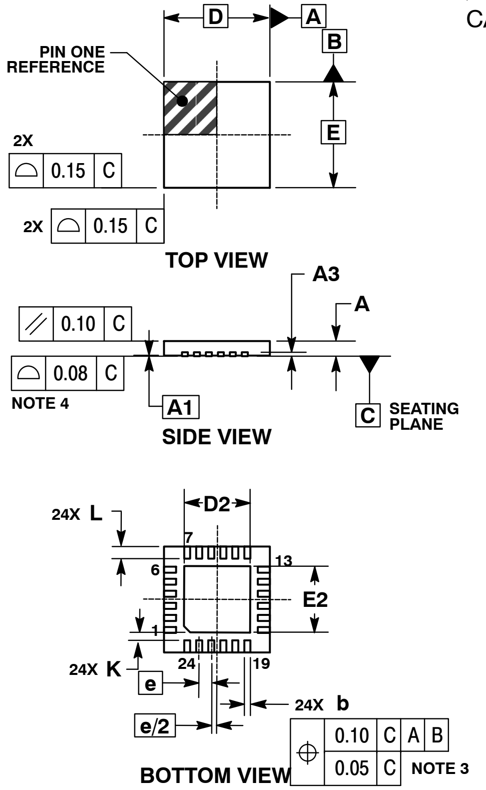
DIM	MILLIMETERS MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

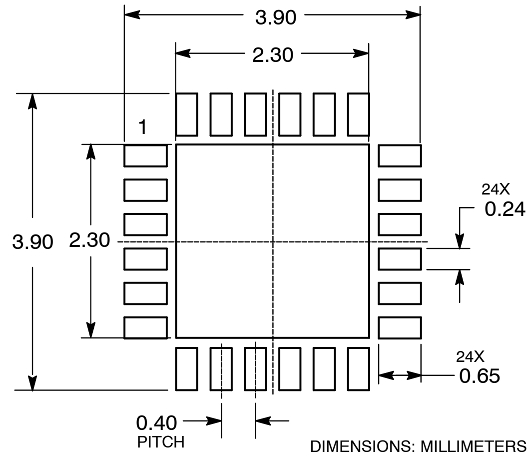
UQFN24, 3.5x3.5, 0.4P
CASE 523AG−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

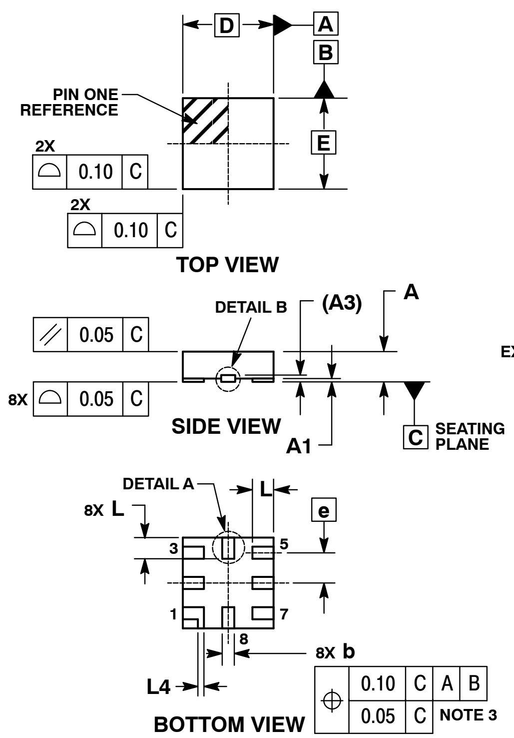
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.50 BSC	
D2	2.10	2.30
E	3.50 BSC	
E2	2.10	2.30
e	0.40 BSC	
L	0.30	0.50
K	0.20	---

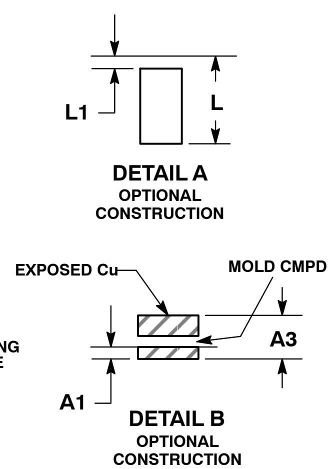
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

UQFN8, 1.5x1.5, 0.5P
CASE 523AH−01
ISSUE O

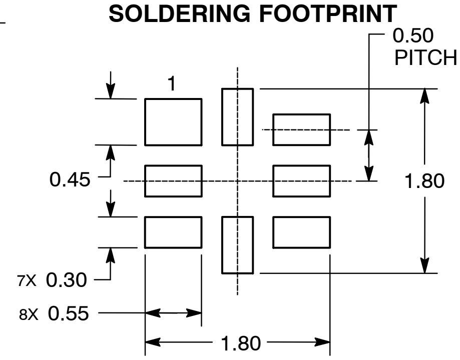




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.

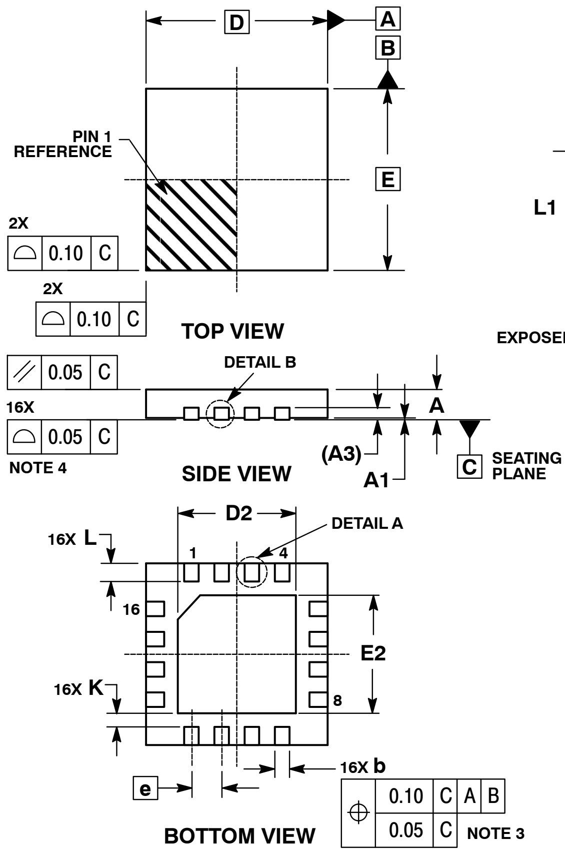
	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	0.00	0.03
L4	0.10 REF	

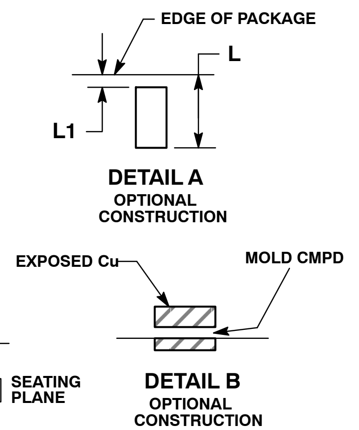
SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

UQFN16, 3x3, 0.5P
CASE 523AJ−01
ISSUE O

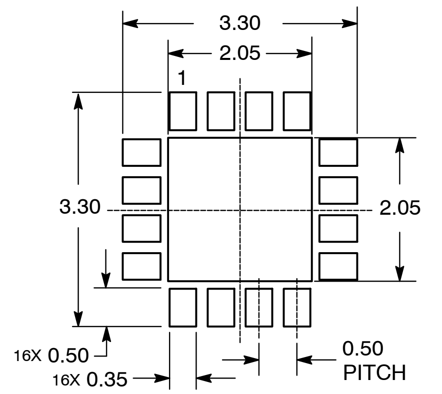




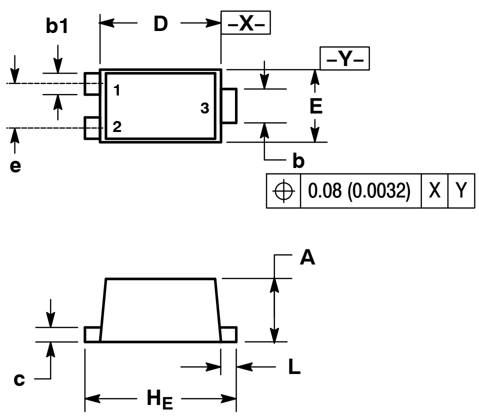
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.85	2.05
E	3.00 BSC	
E2	1.85	2.05
e	0.50 BSC	
K	0.20	−−−
L	0.20	0.40
L1	0.00	0.03

MOUNTING FOOTPRINT



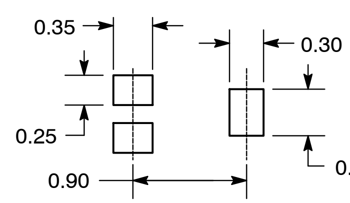
SOT−1123
CASE 524AA−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

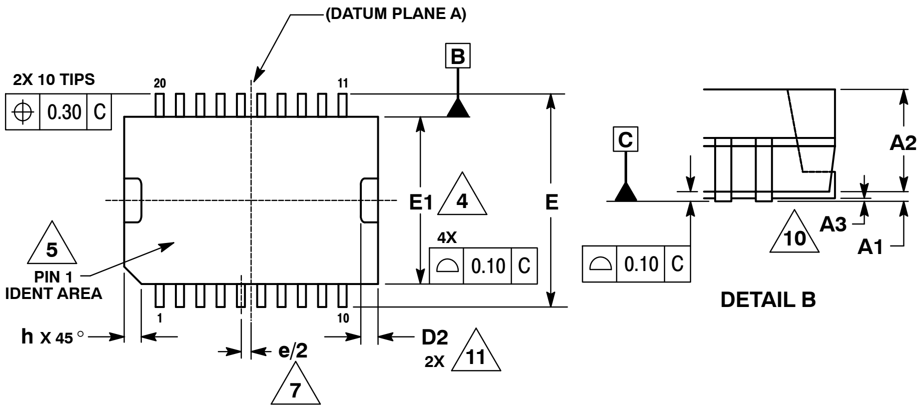
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.34	0.37	0.40	0.013	0.015	0.016
b	0.15	0.22	0.28	0.006	0.009	0.011
b1	0.10	0.15	0.20	0.004	0.006	0.008
c	0.07	0.12	0.17	0.003	0.005	0.007
D	0.75	0.80	0.85	0.030	0.031	0.033
E	0.55	0.60	0.65	0.022	0.024	0.026
e	0.35	−−−	0.40	0.014	−−−−	0.016
H_E	0.95	1.00	1.05	0.037	0.039	0.041
L	0.05	0.10	0.15	0.002	0.004	0.006

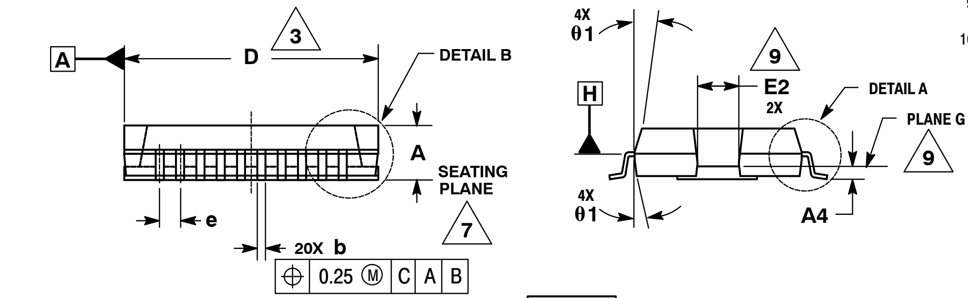
SOLDERING FOOTPRINT

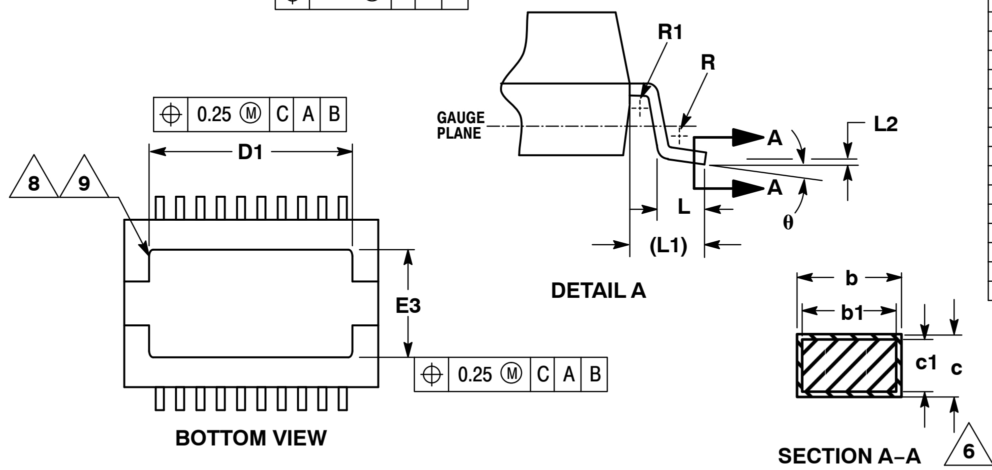


DIMENSIONS: MILLIMETERS

PSOP−20
CASE 525AA−01
ISSUE O



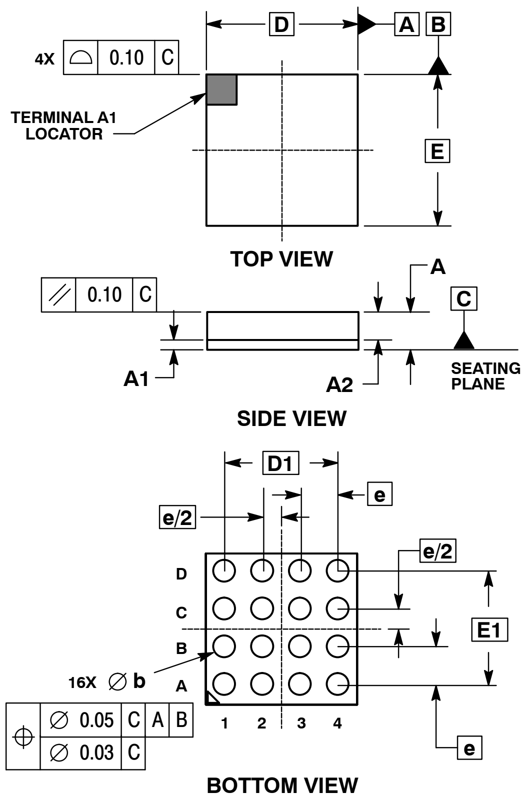




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. D IS DETERMINED AT DATUM H.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH PROTRUSION. INTERLEAD FLASH PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. E1 IS DETERMINED AT DATUM H.
5. A VISUAL IDENTIFIER IS LOCATED WITHIN THE CROSS−HATCHED AREA.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM THE TIP.
7. SEATING PLANE IS DEFINED BY THE LEAD TIP ONLY.
8. MOLDING COMPOUND, 0.15 ±0.05, IS ALLOWED AROUND EXPOSED SLUG EDGES EXCEPT ON BOTH ENDS WHERE ANY AMOUNT IS NOT ALLOWED.
9. DIMENSIONS E2 AND D2 ARE MEASURED AT PLANE G.
10. SLUG LENGTH IS FLUSH WITH PARTING LINE AT DATUM H AND COINCIDENT WITH DIMENSION D.

	MILLIMETERS	
DIM	MIN	MAX
A	---	3.60
A1	0.10	---
A2	3.00	3.30
A4	0.80	1.00
b	0.40	0.53
b1	0.40	0.50
c	0.23	0.32
c1	0.23	0.29
e	1.270 BSC	
D	15.90 BSC	
D1	---	1.10
D2	0.45	0.75
E	14.20 BSC	
E1	11.00 BSC	
E2	---	2.90
E3	5.60	6.20
h	---	1.10
L	0.80	1.10
L1	1.60 REF	
L2	0.35 BSC	
R	0.20	---
R1	0.20	---
θ	0 °	8 °
θ1	5 °	15 °

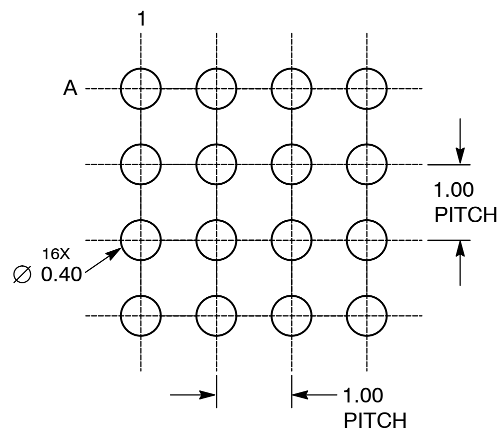
16 PIN LGA 4x4, 1.0P
CASE 526AB−01
ISSUE C



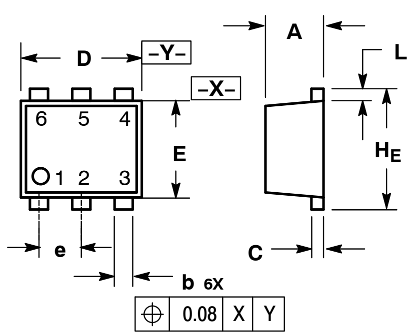
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	TYP	MAX
A	0.89	0.96	1.03
A1	0.22	0.26	0.30
A2	0.67	0.70	0.73
b	0.30	0.40	0.50
D		4.00 BSC	
D1		3.00 BSC	
E		4.00 BSC	
E1		3.00 BSC	
e		1.00 BSC	

SOLDERING FOOTPRINT



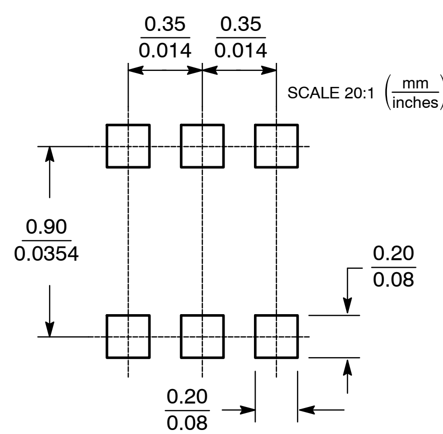
SOT−963
CASE 527AA−01
ISSUE B



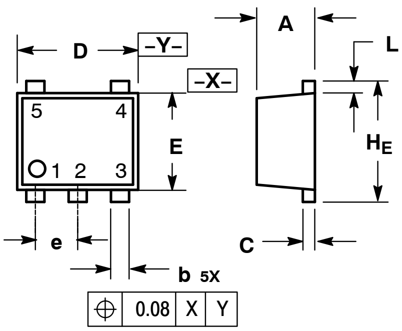
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.40	0.45	0.50	0.016	0.018	0.020
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.05	0.10	0.15	0.002	0.004	0.006
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e		0.35 BSC			0.014 BSC	
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT



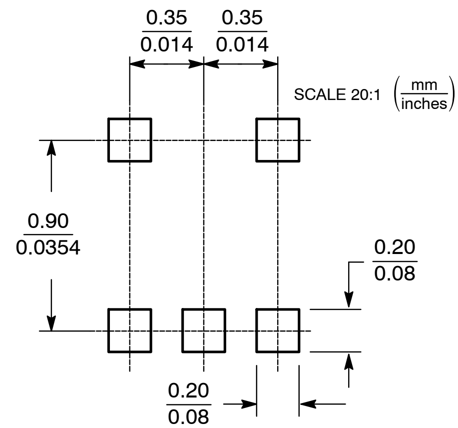
SOT−953
CASE 527AB−01
ISSUE O



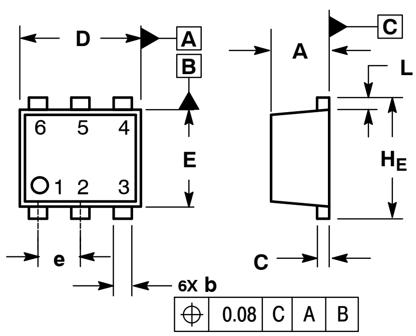
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.40	0.45	0.50	0.016	0.018	0.020
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.05	0.10	0.15	0.002	0.004	0.006
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT



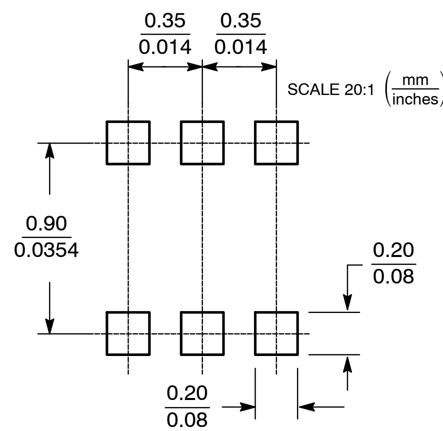
SOT−963
CASE 527AD−01
ISSUE B



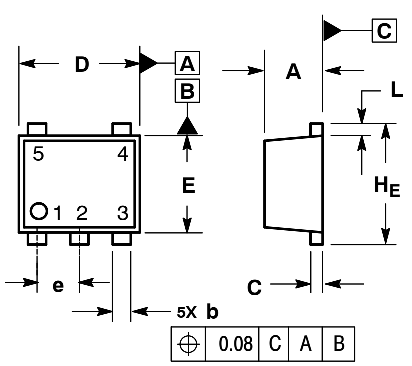
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.34	0.37	0.40			
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.07	0.12	0.17	0.003	0.005	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT



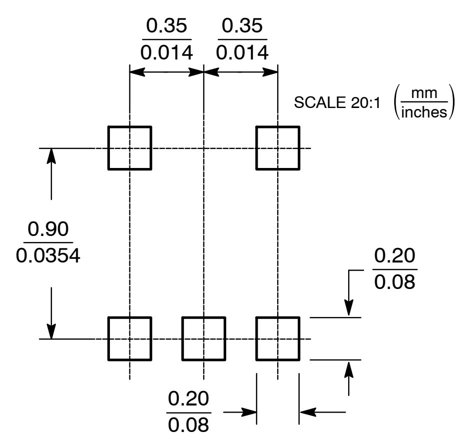
SOT−953
CASE 527AE−01
ISSUE B



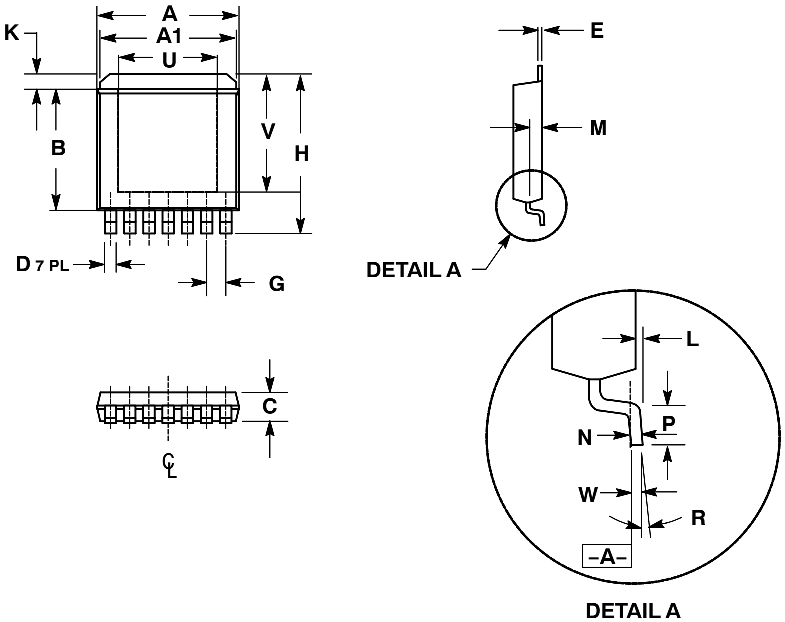
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.34	0.37	0.40			
b	0.10	0.15	0.20	0.004	0.006	0.008
C	0.07	0.12	0.17	0.003	0.005	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.35 BSC			0.014 BSC		
L	0.05	0.10	0.15	0.002	0.004	0.006
H_E	0.95	1.00	1.05	0.037	0.039	0.041

SOLDERING FOOTPRINT



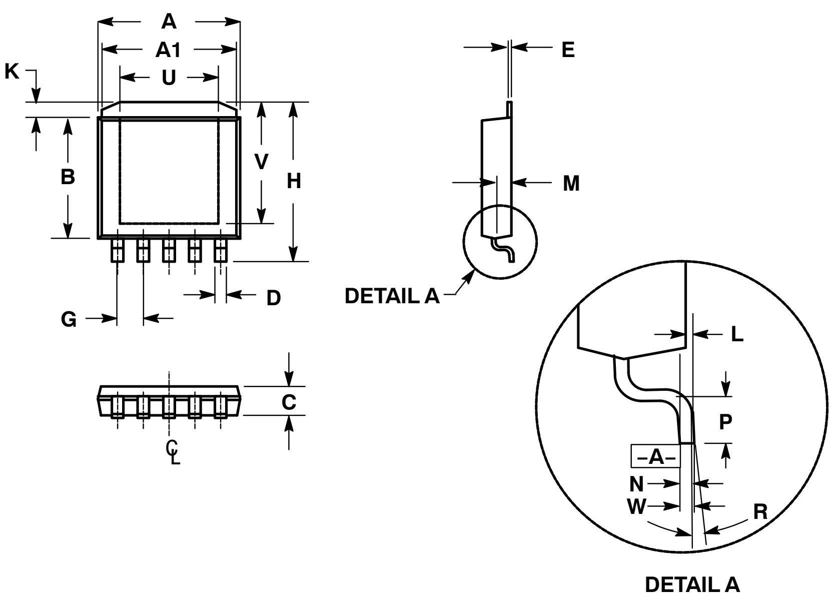
SPAK, 7−LEAD
CASE 553AA−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010 BSC		0.25 BSC	
G	0.050 BSC		1.27 BSC	
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010 BSC		0.25 BSC	
P	0.031	0.041	0.79	1.04
R	0 °	6 °	0 °	6 °
U	0.256 BCS		6.50 BSC	
V	0.316 BSC		8.03 BSC	
W	0.010 BSC		0.25 BSC	

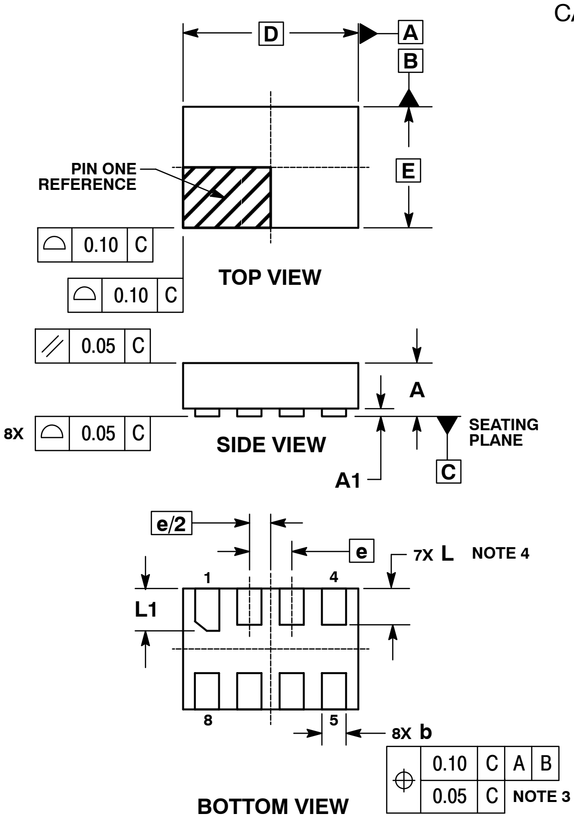
SPAK, 5−LEAD
CASE 553AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.365	0.375	9.27	9.52
A1	0.350	0.360	8.89	9.14
B	0.310	0.320	7.87	8.13
C	0.070	0.080	1.78	2.03
D	0.025	0.031	0.63	0.79
E	0.010 BSC		0.25 BSC	
G	0.067 BSC		1.70 BSC	
H	0.410	0.420	10.41	10.67
K	0.030	0.050	0.76	1.27
L	0.001	0.005	0.03	0.13
M	0.035	0.045	0.89	1.14
N	0.010 BSC		0.25 BSC	
P	0.031	0.041	0.79	1.04
R	0°	6°	0°	6°
U	0.256 BSC		6.50 BSC	
V	0.316 BSC		8.03 BSC	
W	0.010 BSC		0.25 BSC	

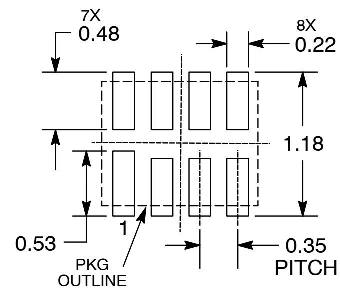
ULLGA8, 1.45x1.0, 0.35P
CASE 613AA−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

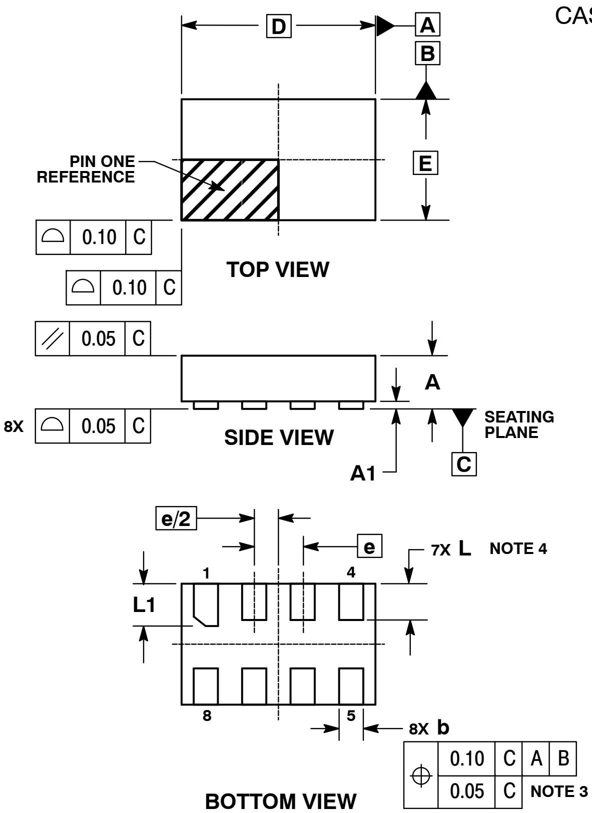
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

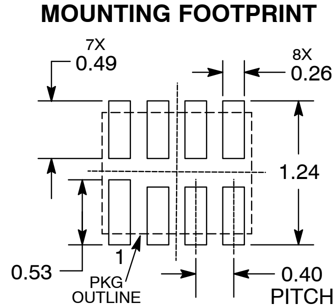
ULLGA8, 1.6x1.0, 0.4P
CASE 613AB−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

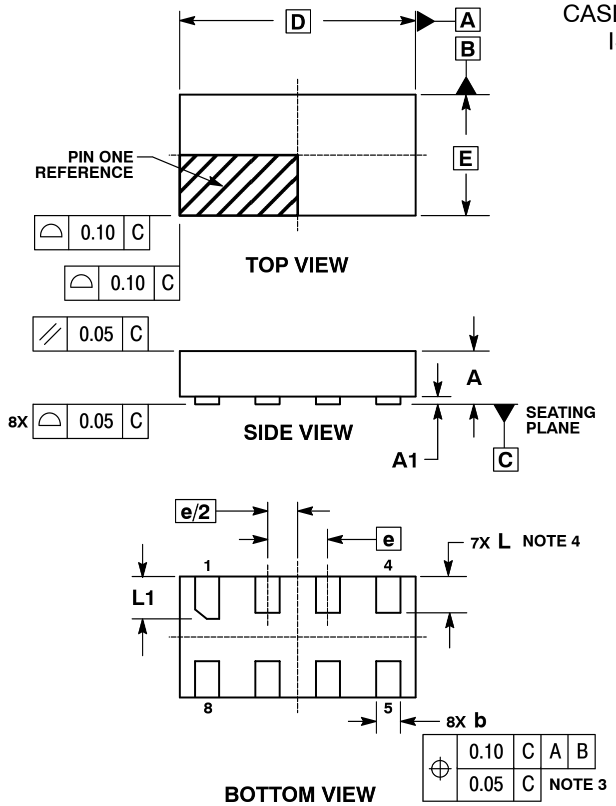
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.60 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

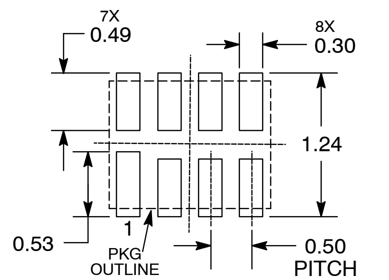
ULLGA8, 1.95x1.0, 0.5P
CASE 613AC−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

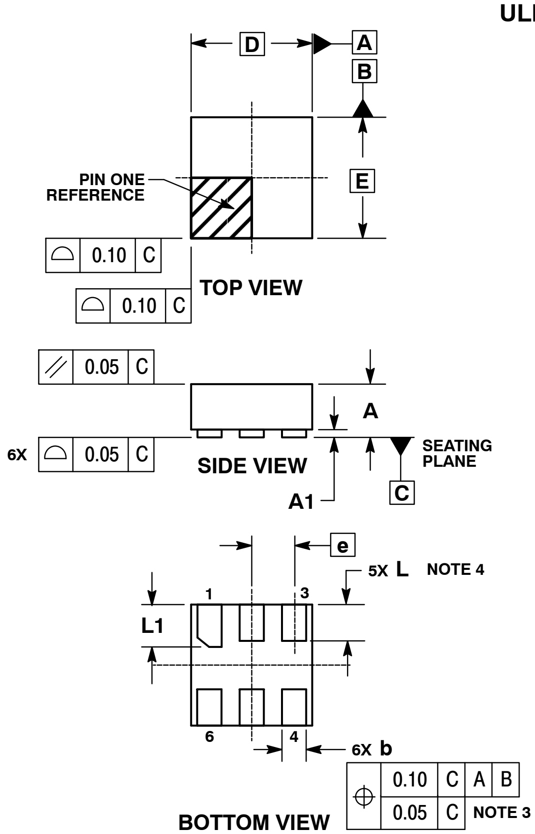
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.95 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

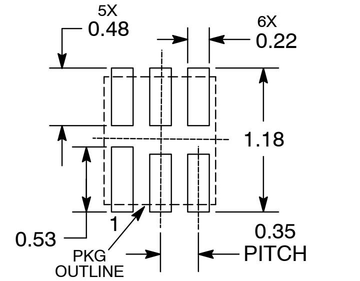
ULLGA6, 1.0x1.0, 0.35P
CASE 613AD−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

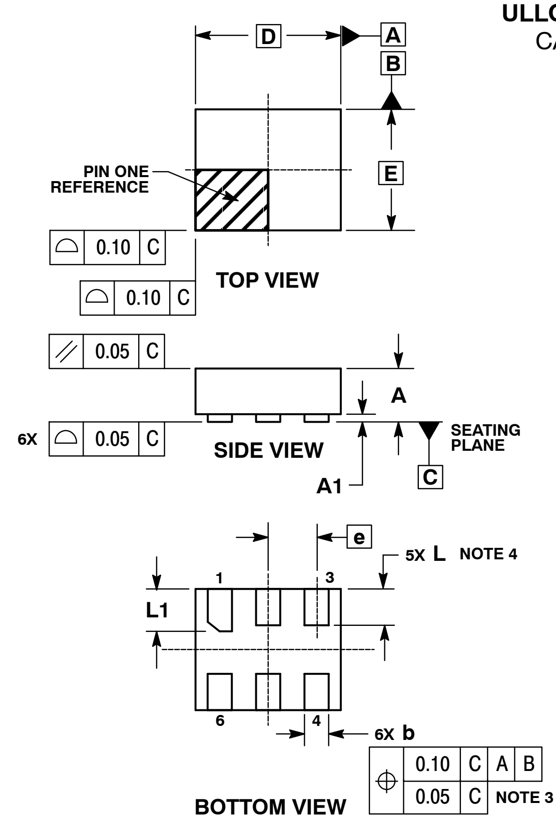
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

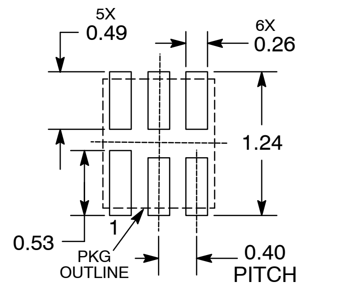
ULLGA6, 1.2x1.0, 0.4P
CASE 613AE−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

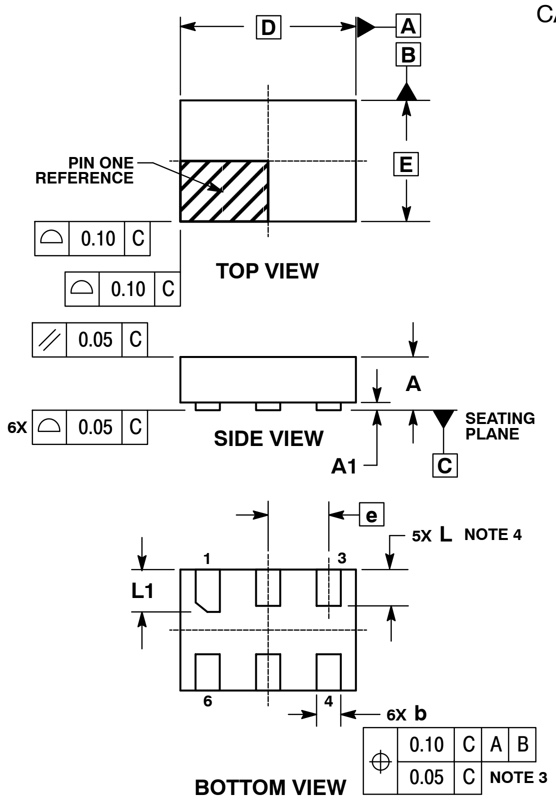
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

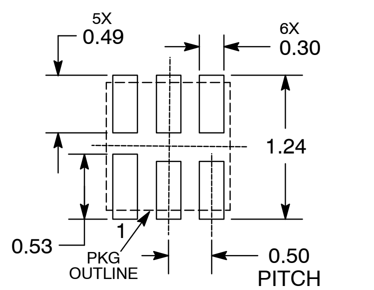
ULLGA6, 1.45x1.0, 0.5P
CASE 613AF−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

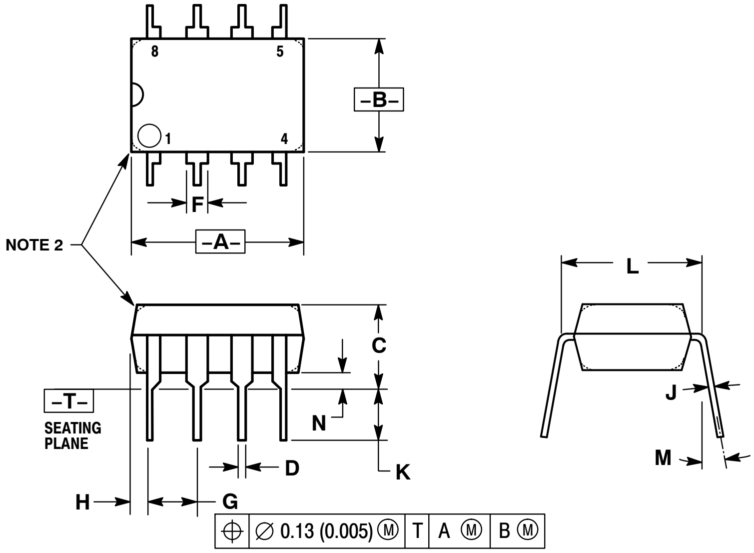
	MILLIMETERS	
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

DIP−8
CASE 626−05
ISSUE L

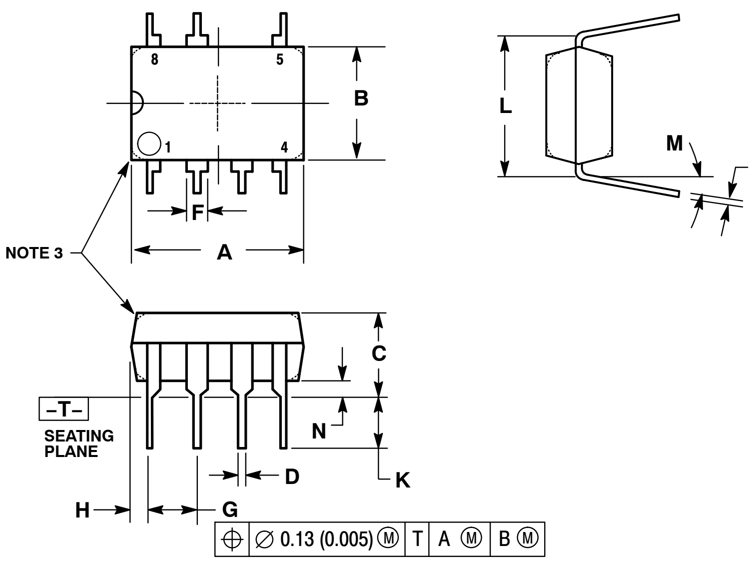


NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

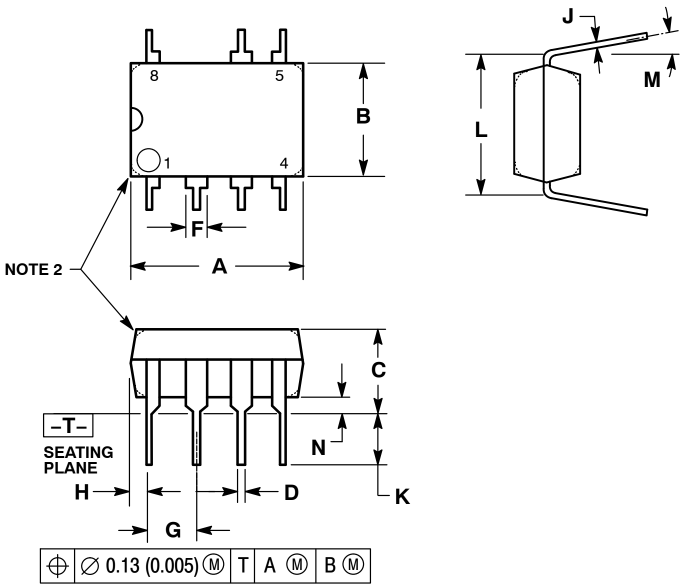
PDIP−8
CASE 626A−01
ISSUE O



NOTES:
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: MILLIMETER.
7. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
8. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
9. DIMENSIONS A AND B ARE DATUMS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PDIP−7
CASE 626B−01
ISSUE A

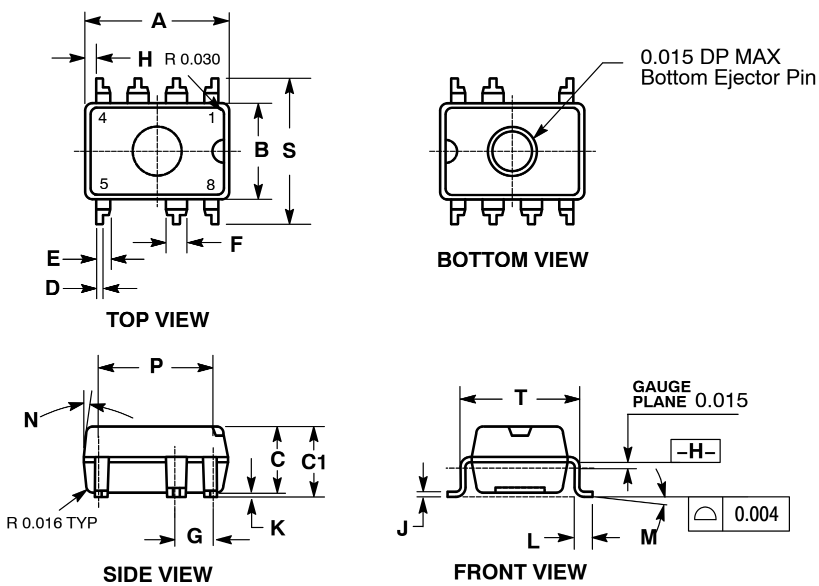


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
5. DIMENSIONS A AND B ARE DATUMS.

	MILLIMETERS	
DIM	MIN	MAX
A	9.40	10.16
B	6.10	6.60
C	3.94	4.45
D	0.38	0.51
F	1.02	1.78
G	2.54 BSC	
H	0.76	1.27
J	0.20	0.30
K	2.92	3.43
L	7.62 BSC	
M	−−−	10 °
N	0.76	1.01

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

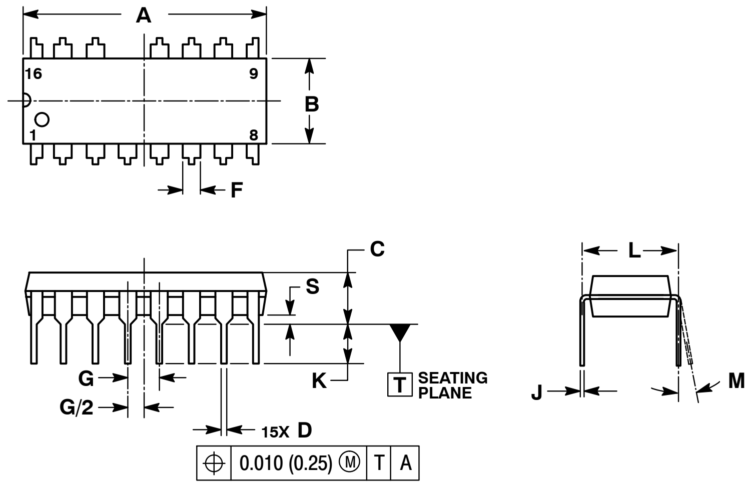
PDIP−7, GULL WING
CASE 626AA−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN INCHES.

	INCHES	
DIM	MIN	MAX
A	0.365	0.385
B	0.240	0.260
C	0.120	0.150
C1	0.124	0.162
D	0.018 TYP	
E	0.039 TYP	
F	0.045	0.065
G	0.100 BSC	
H	0.023	0.033
J	0.010 TYP	
K	0.004	0.012
L	0.036	0.044
M	0 °	8 °
N	12 ° TYP	
P	0.300 BSC	
S	0.372	0.388

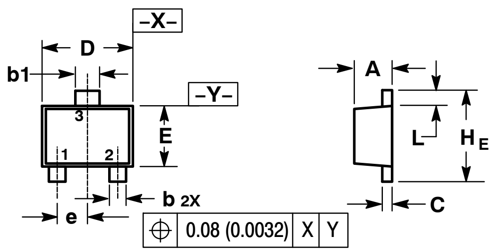
PDIP−16 LESS PIN 13
CASE 626AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SOT−723
CASE 631AA−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
b	0.15	0.21	0.27	0.0059	0.0083	0.0106
b1	0.25	0.31	0.37	0.010	0.012	0.015
C	0.07	0.12	0.17	0.0028	0.0047	0.0067
D	1.15	1.20	1.25	0.045	0.047	0.049
E	0.75	0.80	0.85	0.03	0.032	0.034
e	0.40 BSC			0.016 BSC		
H_E	1.15	1.20	1.25	0.045	0.047	0.049
L	0.15	0.20	0.25	0.0059	0.0079	0.0098

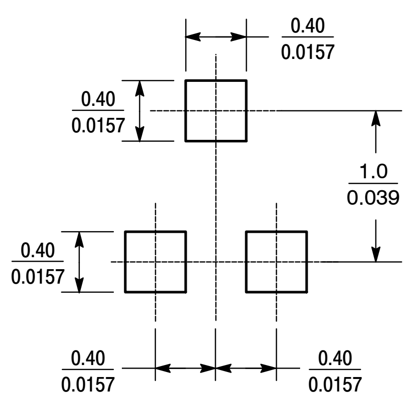
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

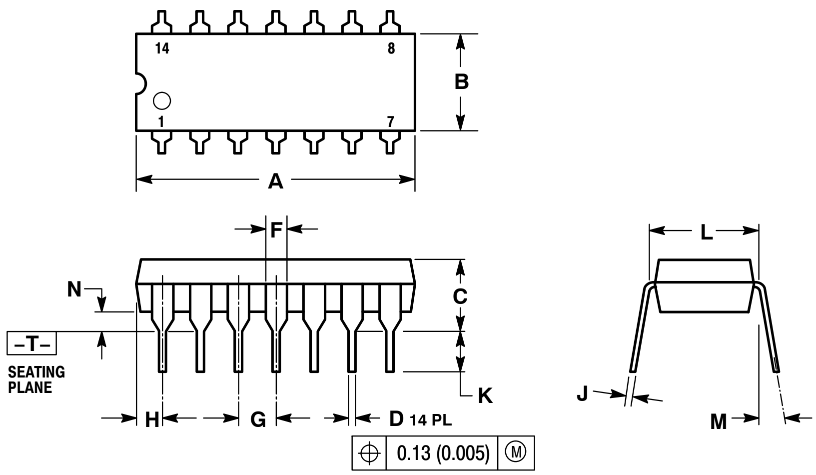
STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

SOLDERING FOOTPRINT



SCALE 20:1 $\left(\frac{mm}{inches}\right)$

PDIP−14
CASE 646−06
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. NO CONNECTION
5. GATE
6. SOURCE
7. DRAIN
8. DRAIN
9. SOURCE
10. GATE
11. NO CONNECTION
12. GATE
13. SOURCE
14. DRAIN

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. NO CONNECTION
5. SOURCE
6. DRAIN
7. GATE
8. GATE
9. DRAIN
10. SOURCE
11. NO CONNECTION
12. SOURCE
13. DRAIN
14. GATE

STYLE 6:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 7:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 8:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

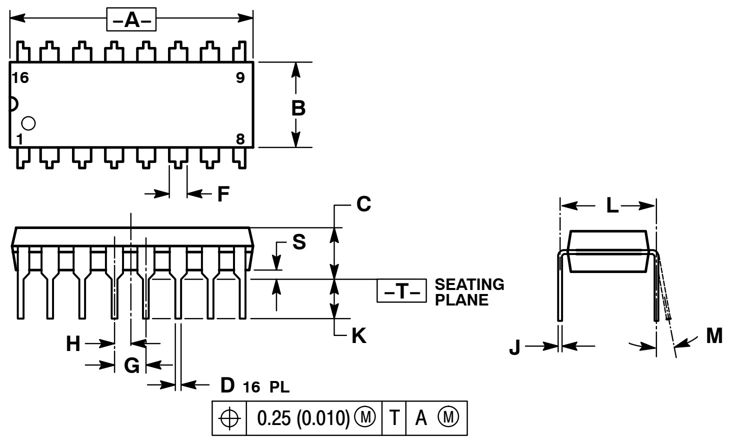
STYLE 9:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

STYLE 10:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 12:
PIN 1. COMMON CATHODE
2. COMMON ANODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. COMMON ANODE
7. COMMON CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. ANODE/CATHODE
14. ANODE/CATHODE

DIP−16
CASE 648−08
ISSUE T



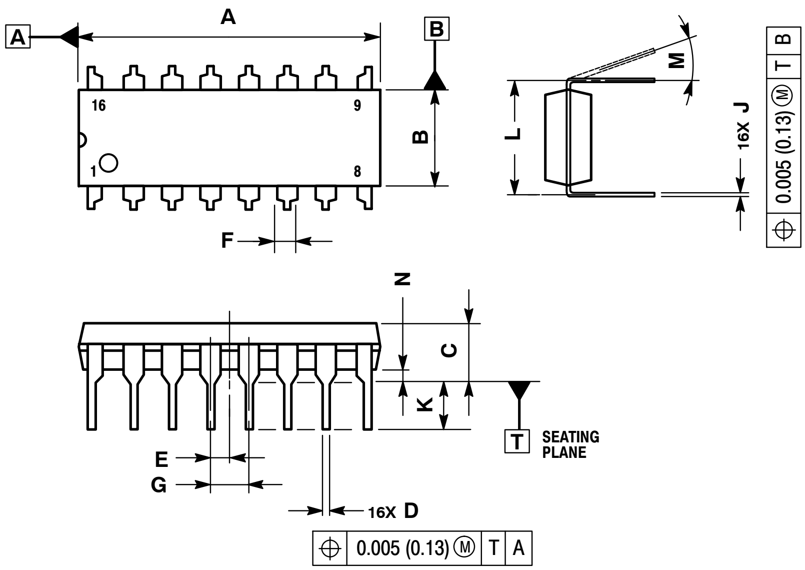
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

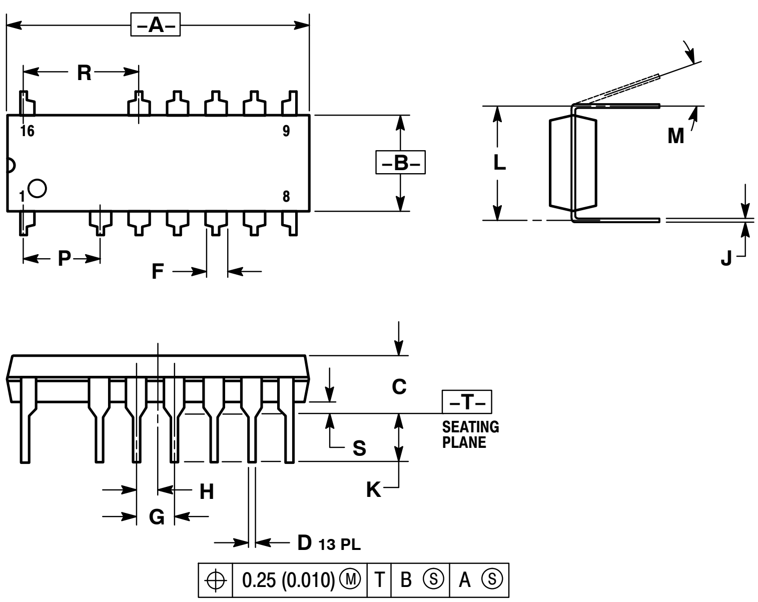
PDIP−16
CASE 648C−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.744	0.783	18.90	19.90
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
E	0.050 BSC		1.27 BSC	
F	0.040	0.70	1.02	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.040	0.39	1.01

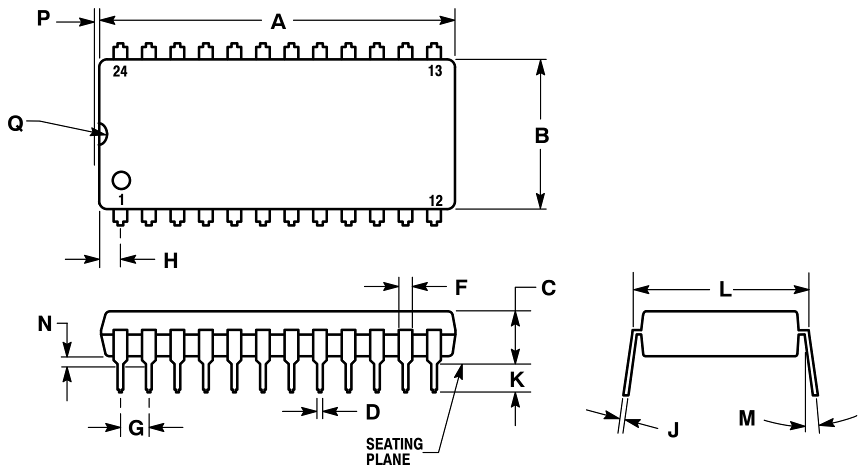
PDIP−16
CASE 648E−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNER OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.760	18.80	19.30
B	0.245	0.260	6.23	6.60
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.120	0.140	3.05	3.55
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
P	0.200 BSC		5.08 BSC	
R	0.300 BSC		7.62 BSC	
S	0.015	0.035	0.39	0.88

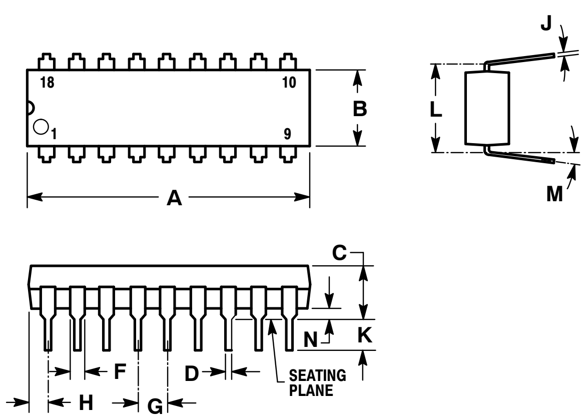
DIP−24 WIDE BODY
CASE 649−03
ISSUE D



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. CONTROLLING DIMENSION:INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.240	1.265	31.50	32.13
B	0.520	0.540	13.21	13.72
C	0.185	0.205	4.70	5.21
D	0.015	0.020	0.38	0.51
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.590	0.610	14.99	15.49
M	---	10°	---	10°
N	0.020	0.040	0.51	1.02
P	0.005	0.015	0.13	0.38
Q	0.020	0.030	0.51	0.76

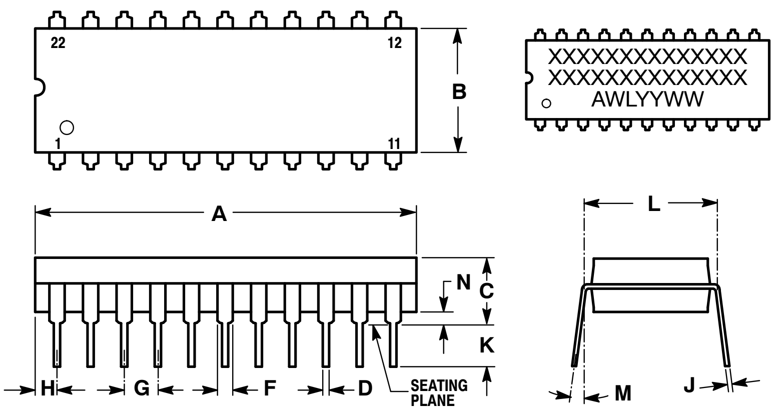
DIP−18
CASE 707−02
ISSUE D



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

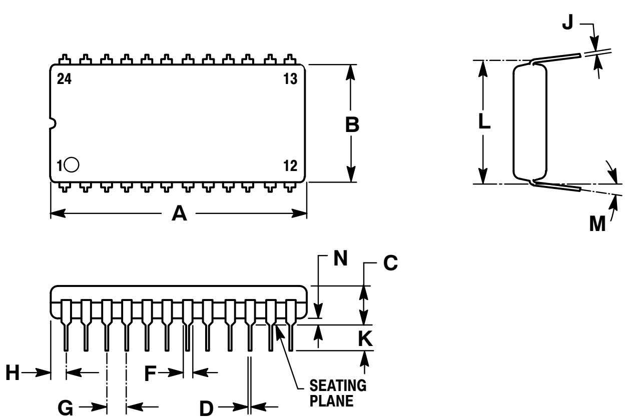
PDIP−22
CASE 708−04
ISSUE E



NOTES:
1. CONTROLLING DIMENSION: INCH.
2. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

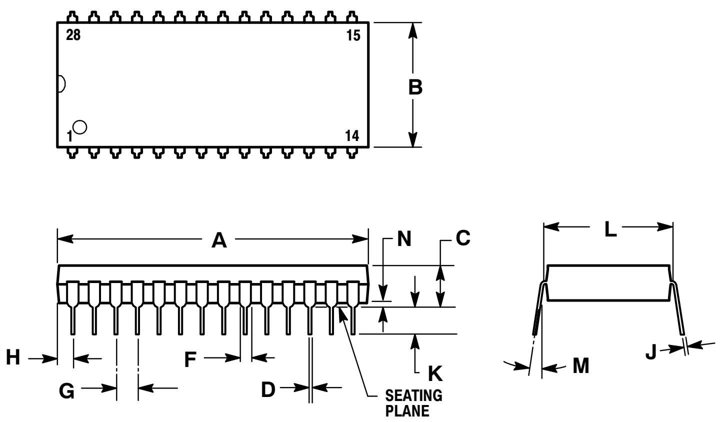
PDIP−24
CASE 709−02
ISSUE D



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.235	1.265	31.37	32.13
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.080	1.65	2.03
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

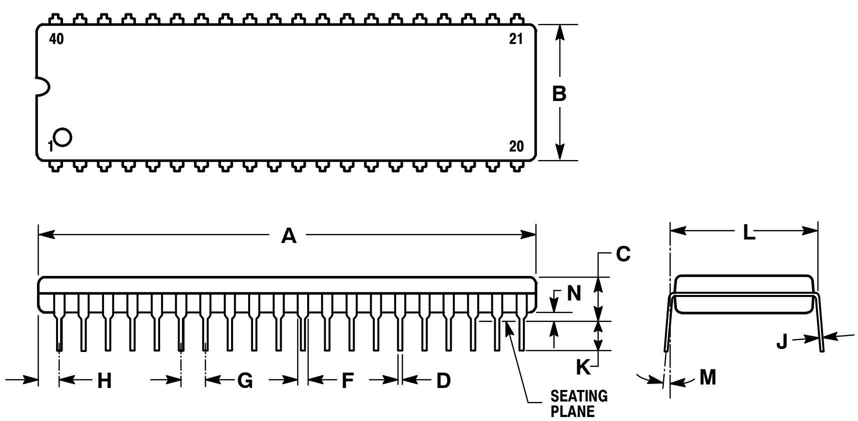
DIP−28 WIDE BODY
CASE 710−02
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
H	0.065	0.085	1.65	2.16
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

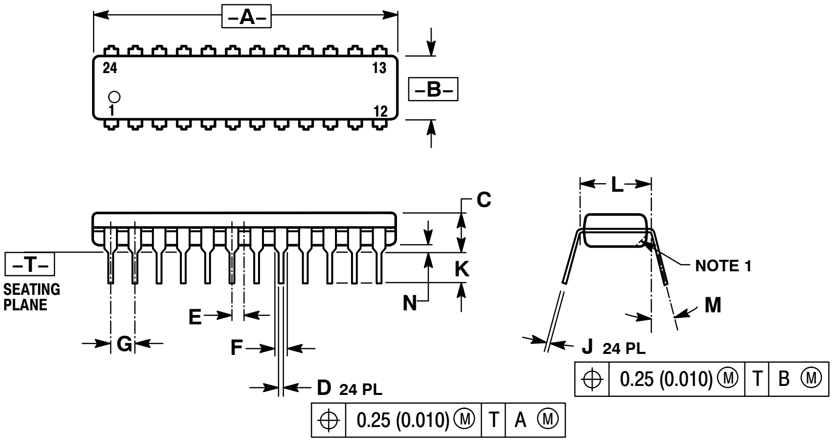
DIP−40 WIDE BODY
CASE 711−03
ISSUE D



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

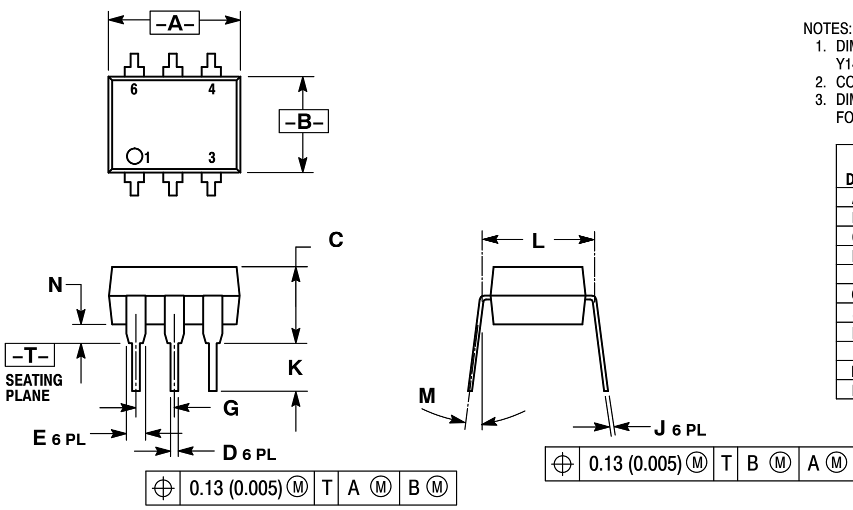
DIP−24
CASE 724−03
ISSUE D



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

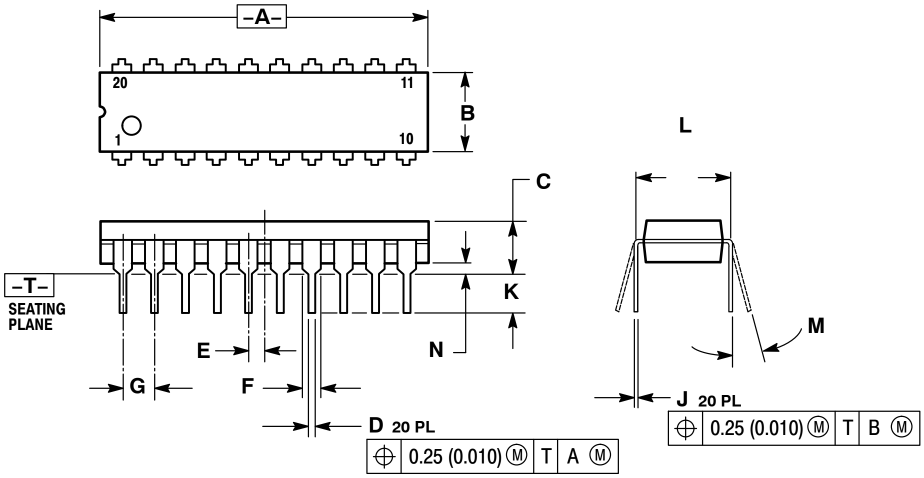
PDIP−6
CASE 730N−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.330	0.350	8.38	8.89
B	0.240	0.270	6.10	6.86
C	---	0.209	---	5.30
D	0.016	0.022	0.41	0.56
E	0.049	0.059	1.24	1.50
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.20	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.035	0.055	0.90	1.40

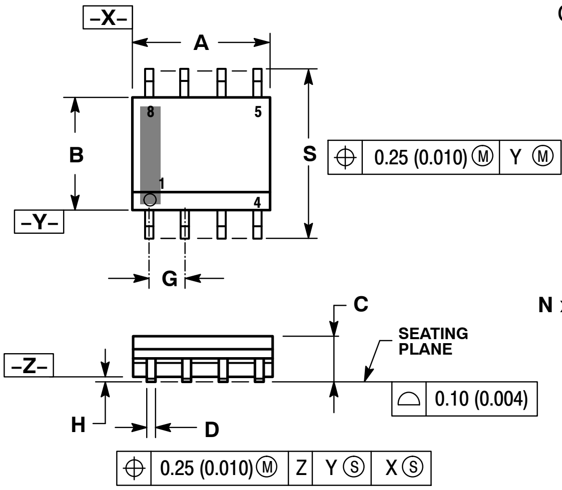
DIP−20
CASE 738−03
ISSUE E

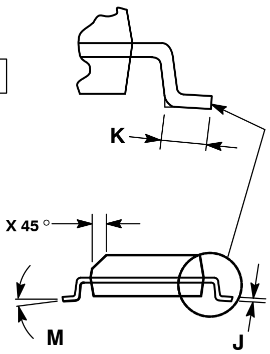


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO−8
CASE 751−07
ISSUE AJ





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

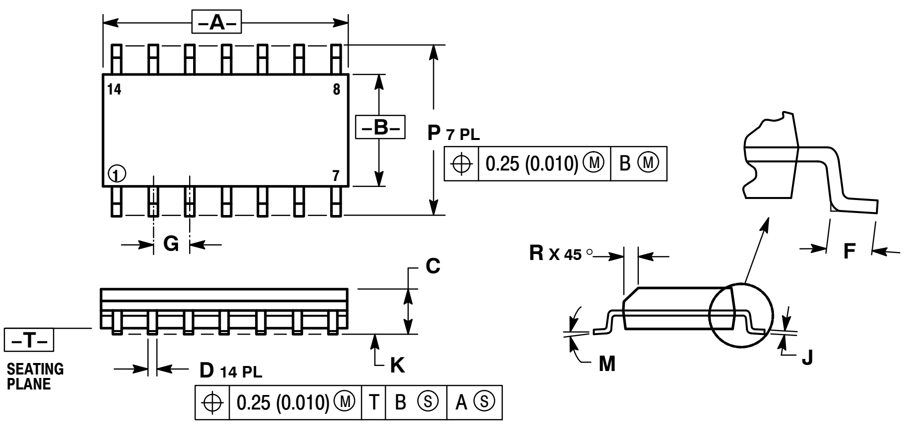
STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

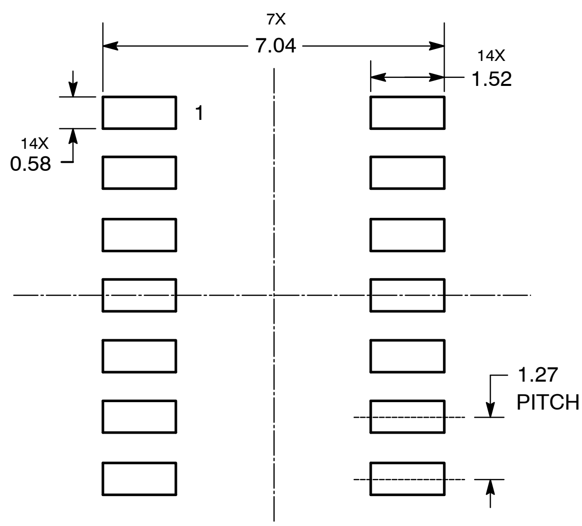
SO−14
CASE 751A−03
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

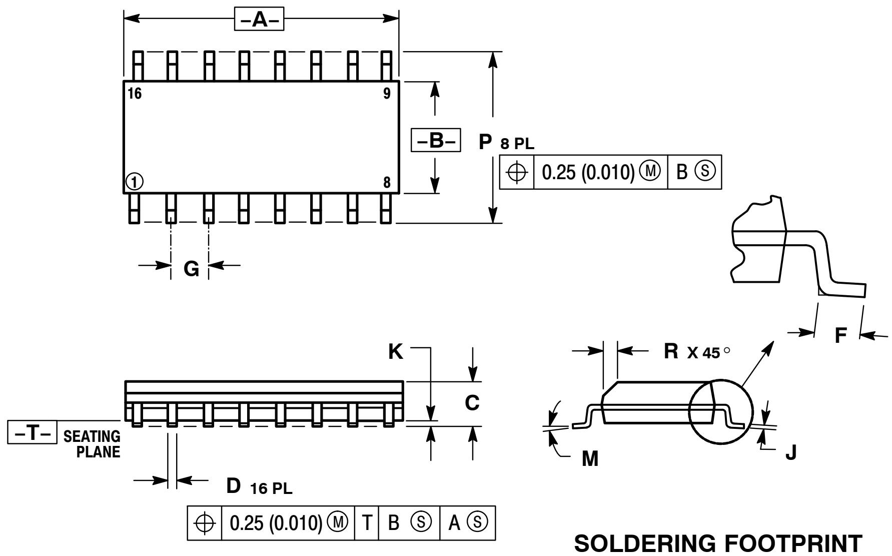
STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

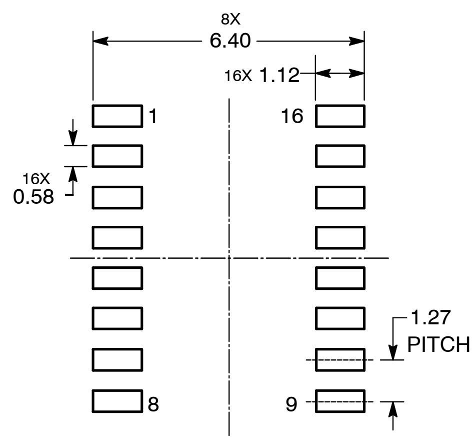
SO−16
CASE 751B−05
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

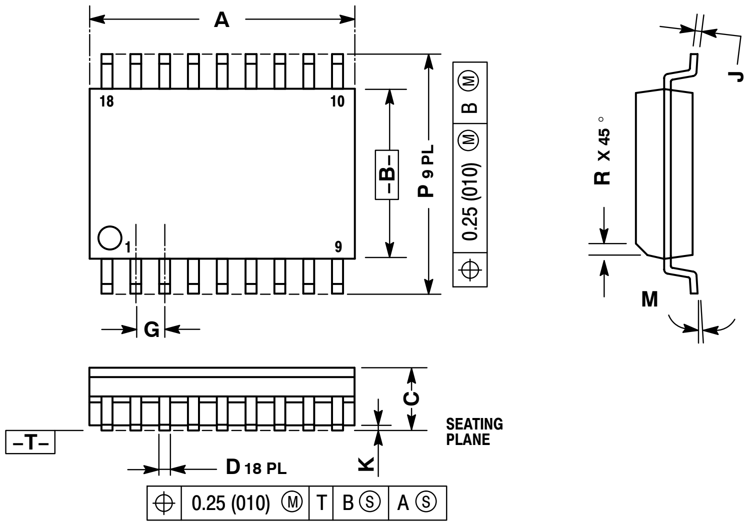
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

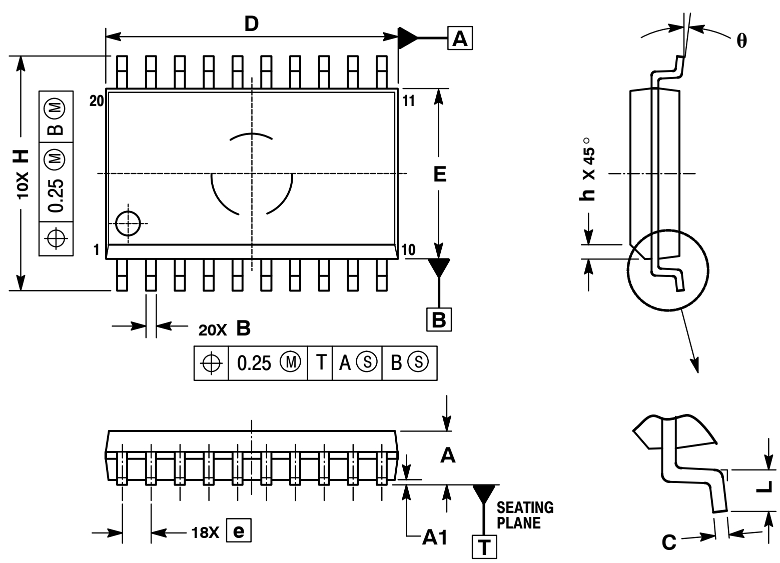
SO−18 WIDE BODY
CASE 751C−04
ISSUE F



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.40	11.70	0.449	0.460
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

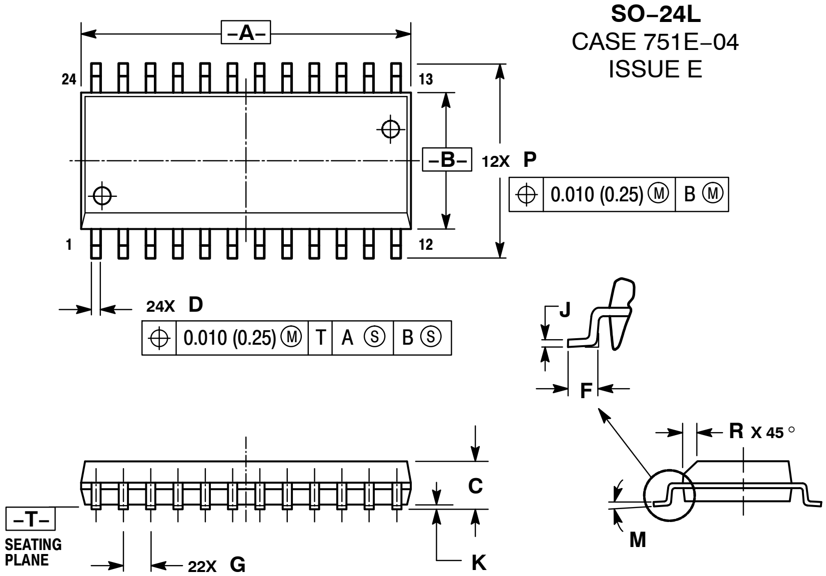
SO−20L
CASE 751D−05
ISSUE G



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

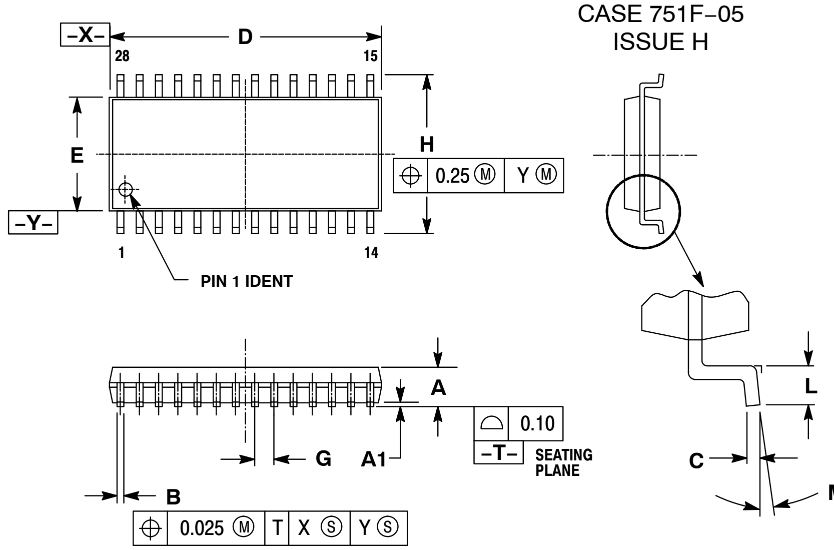
SO−24L
CASE 751E−04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

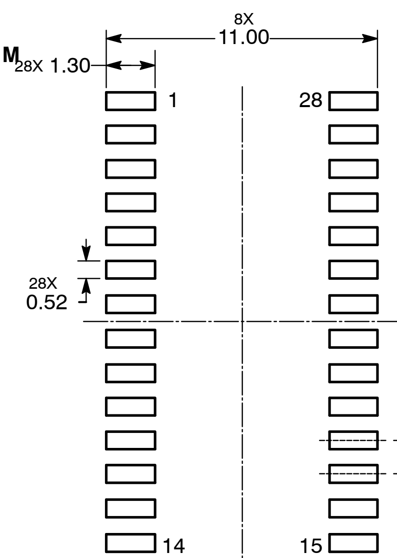
SO−28L
CASE 751F−05
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBER PR5OTRUSION SHALL NOT BE 0.13 TOTATL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

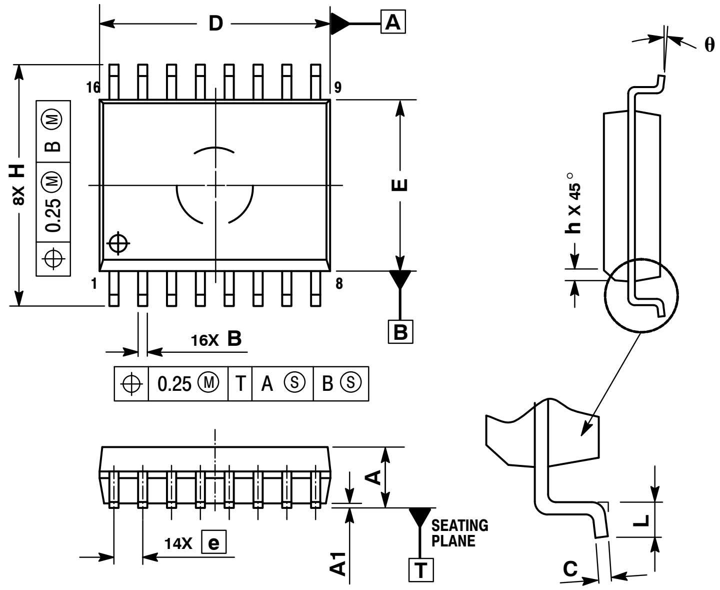
	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
G	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
M	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

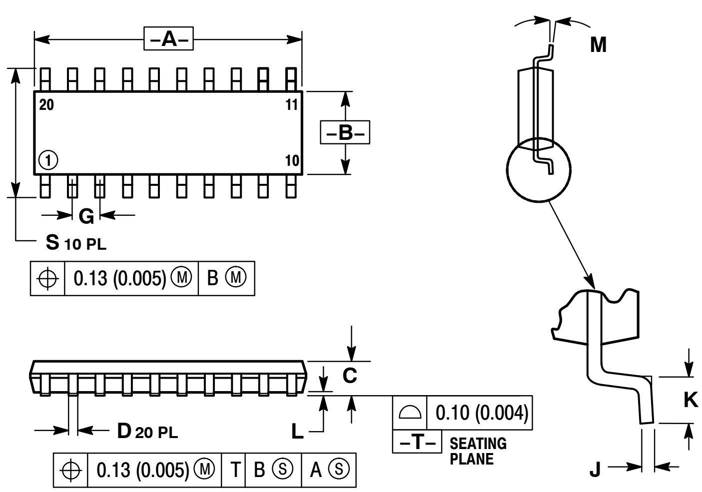
SO−16L
CASE 751G−03
ISSUE C



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

SO−20 EIAJ
CASE 751J−02
ISSUE A

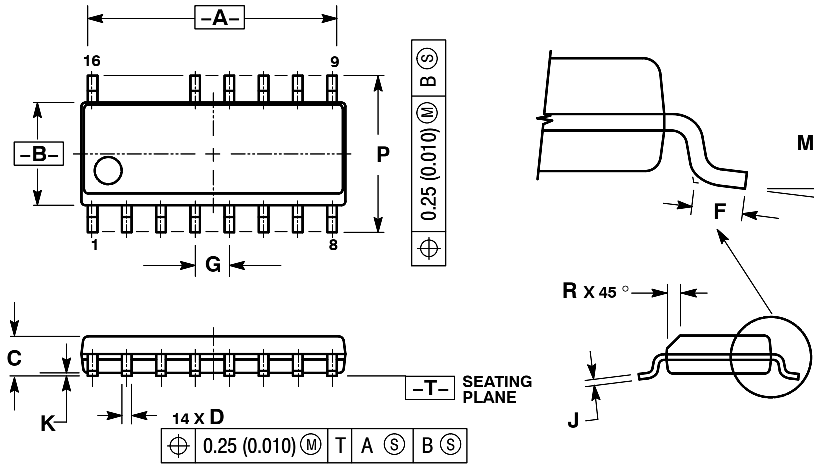


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.12 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.55	12.80	0.494	0.504
B	5.10	5.40	0.201	0.213
C	---	2.00	---	0.079
D	0.35	0.45	0.014	0.018
G	1.27 BSC		0.050 BSC	
J	0.18	0.23	0.007	0.009
K	0.55	0.85	0.022	0.033
L	0.05	0.20	0.002	0.008
M	0 °	7 °	0 °	7 °
S	7.40	8.20	0.291	0.323

SO−16 MISSING LEADS

CASE 751K−01
ISSUE O

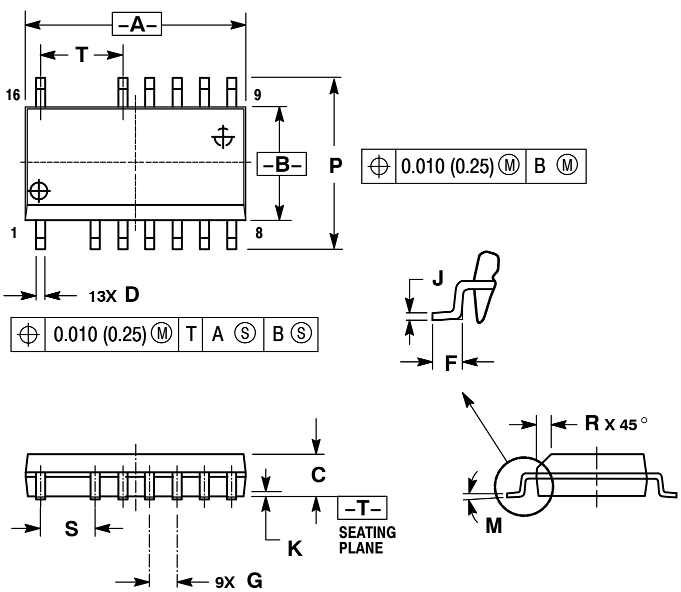


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SO−16 WIDE BODY MISSING LEADS

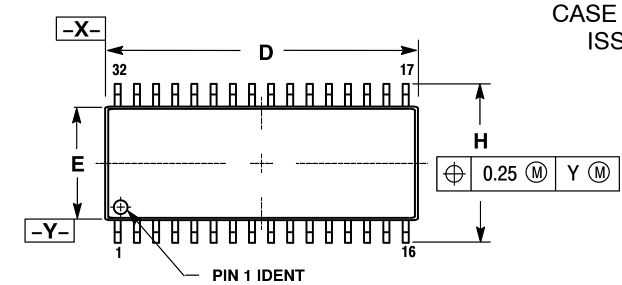
CASE 751N−01
ISSUE O

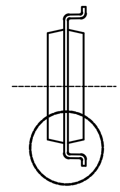


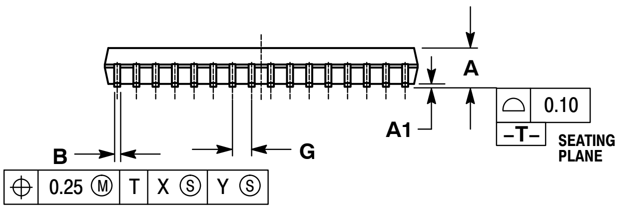
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

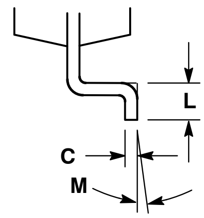
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029
S	2.54 BSC		0.100 BSC	
T	3.81 BSC		0.150 BSC	

SO−32 WIDE BODY
CASE 751P−01
ISSUE O





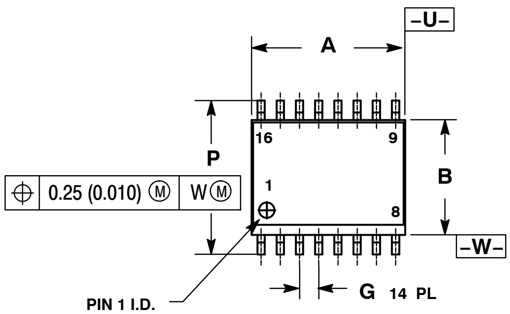




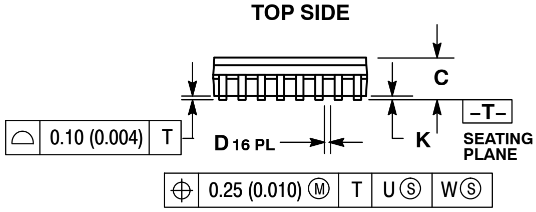
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14 .5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

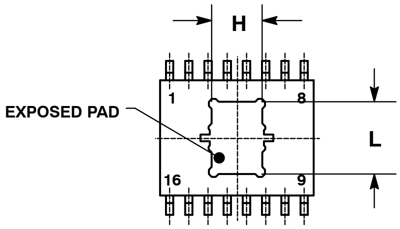
	MILLIMETERS	
DIM	MIN	MAX
A	2.29	2.54
A1	0.10	0.25
B	0.36	0.51
C	0.15	0.32
D	20.57	20.88
E	7.42	7.60
G	1.27 BSC	
H	10.29	10.64
L	0.53	1.04
M	0°	8°

SO−16 WIDE BODY, EXPOSED PAD
CASE 751R−02
ISSUE B

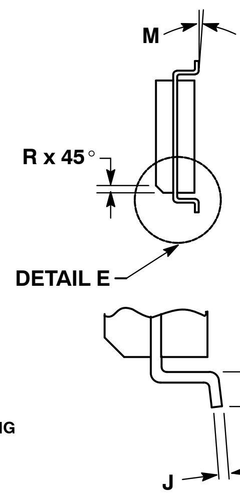


TOP SIDE





BACK SIDE

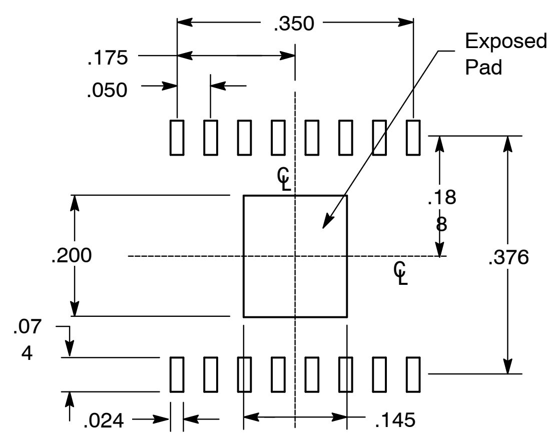


DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUTION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R−01 OBSOLETE, NEW STANDARD 751R−02.

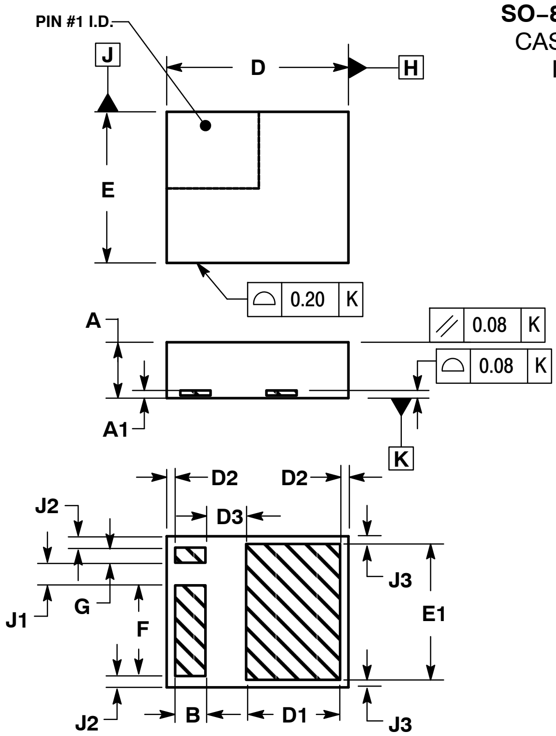
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.31	3.51	0.130	0.138
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
L	4.58	4.78	0.180	0.188
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SOLDERING FOOTPRINT



SCALE 2:1

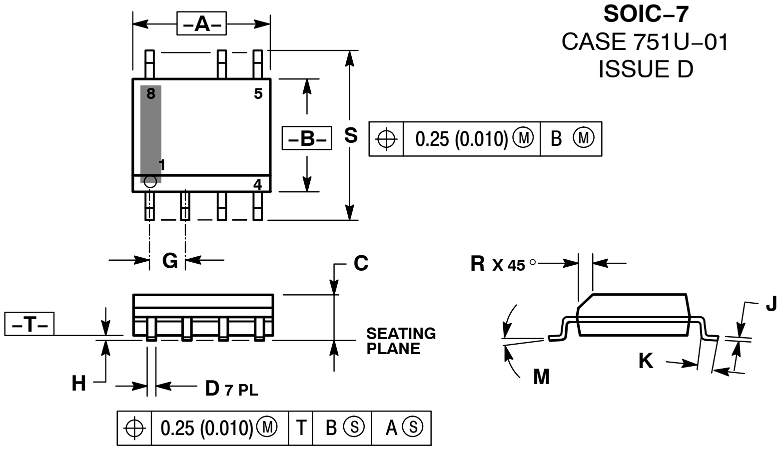
SO−8 LEADLESS
CASE 751S−02
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS	
DIM	MIN	MAX
A	1.750	1.950
A1	0.254 REF	
B	0.900	1.100
D	6.000 BSC	
D1	3.046	3.246
D2	0.154	0.354
D3	1.246	1.446
E	5.000 BSC	
E1	4.392	4.592
F	2.940	3.140
G	0.400	0.600
J1	0.680	0.880
J2	0.250	0.450
J3	0.154	0.354

SOIC−7
CASE 751U−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

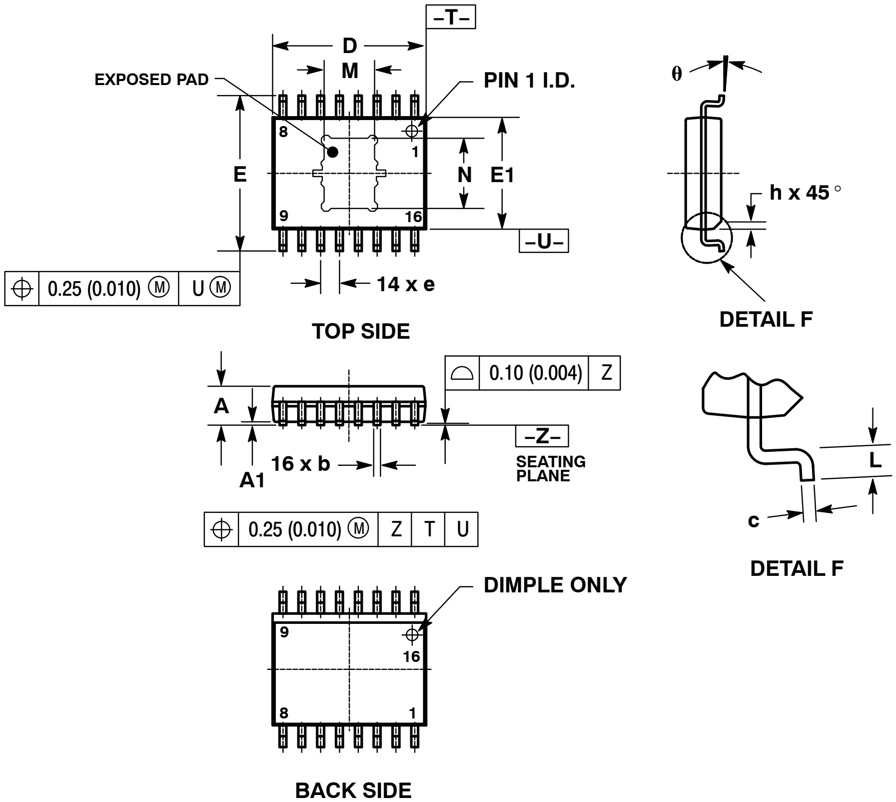
STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

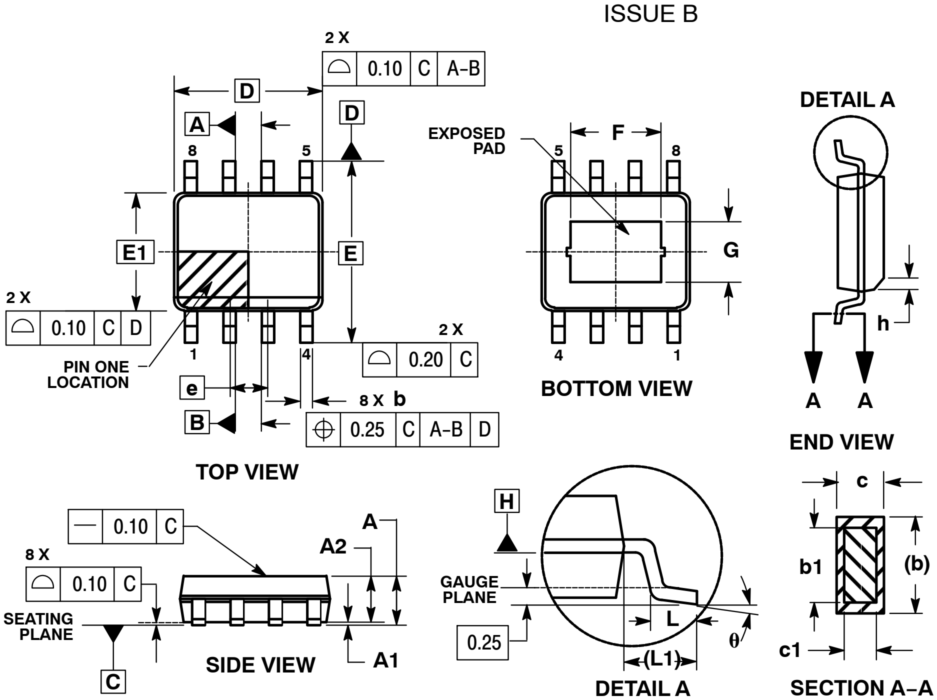
SOIC−16 WIDE BODY EXPOSED PAD
CASE 751AB−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.35	2.65	0.093	0.104
A1	0.1	0.25	0.004	0.009
D	10.15	10.45	0.400	0.411
E	10.05	10.55	0.395	0.415
E1	7.4	7.6	0.292	0.299
b	0.35	0.49	0.014	0.019
c	0.25	0.32	0.010	0.012
e	1.27 BSC		0.050 BSC	
L	0.5	0.9	0.020	0.035
h	0.25	0.75	0.010	0.029
θ	0 °	7 °	0 °	7 °
M	3.31	3.51	0.130	0.138
N	4.58	4.78	0.180	0.188

SOIC−8 EXPOSED PAD
CASE 751AC−01
ISSUE B

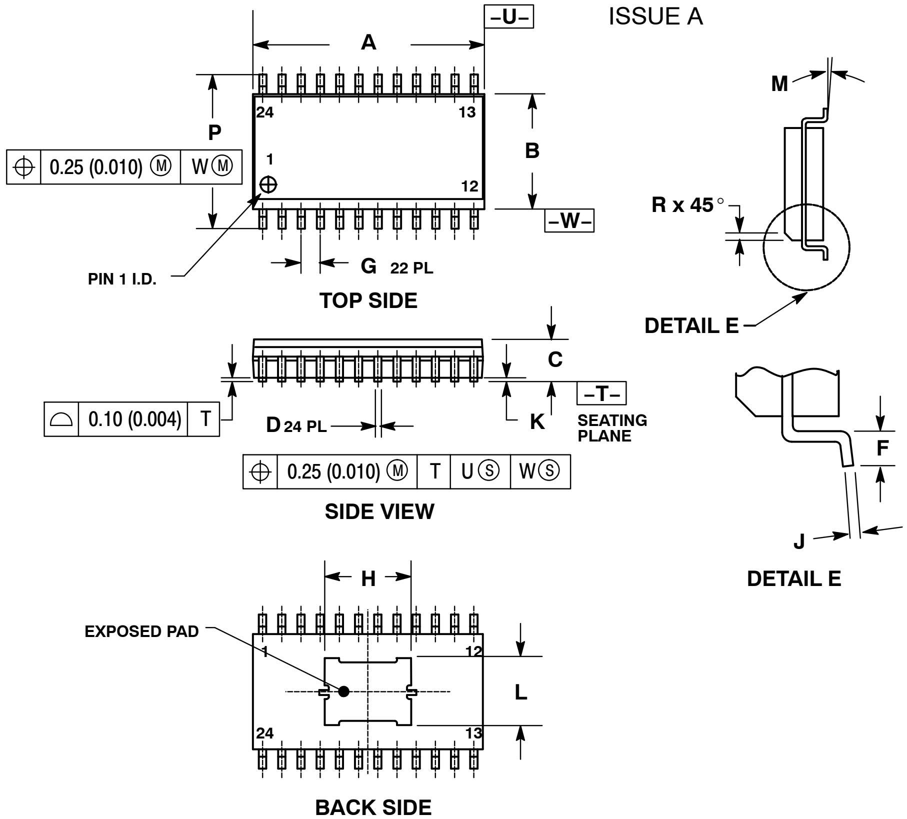


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

SOIC−24 WIDE BODY EXPOSED PAD

CASE 751AE−01
ISSUE A

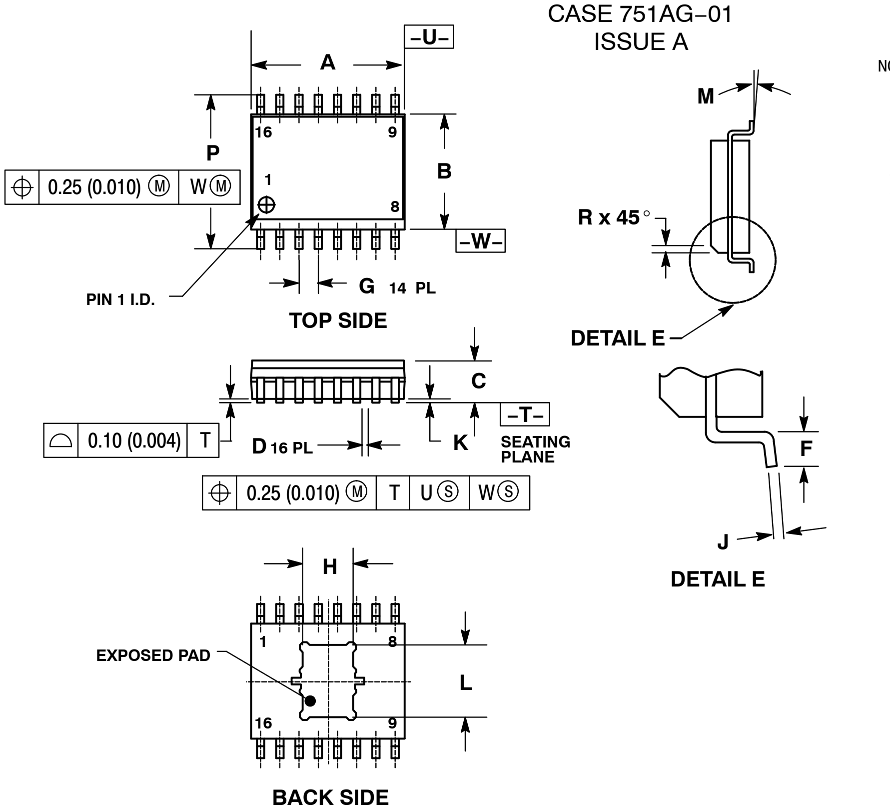


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	15.25	15.54
B	7.40	7.60
C	2.35	2.65
D	0.35	0.49
F	0.41	0.90
G	1.27 BSC	
H	5.596	5.796
J	0.25	0.32
K	0.13	0.29
L	3.767	3.969
M	0 °	8 °
P	10.05	10.55
R	0.25	0.75

SOIC−16 WIDE BODY EXPOSED PAD

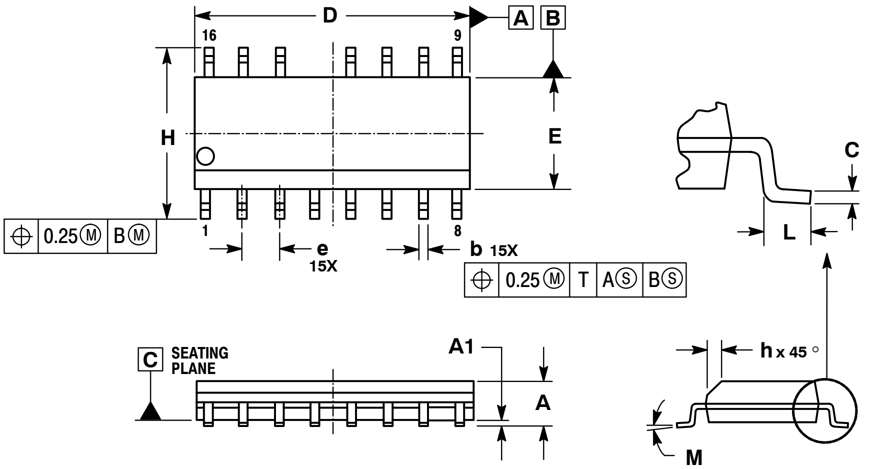
CASE 751AG−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R−01 OBSOLETE, NEW STANDARD 751R−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

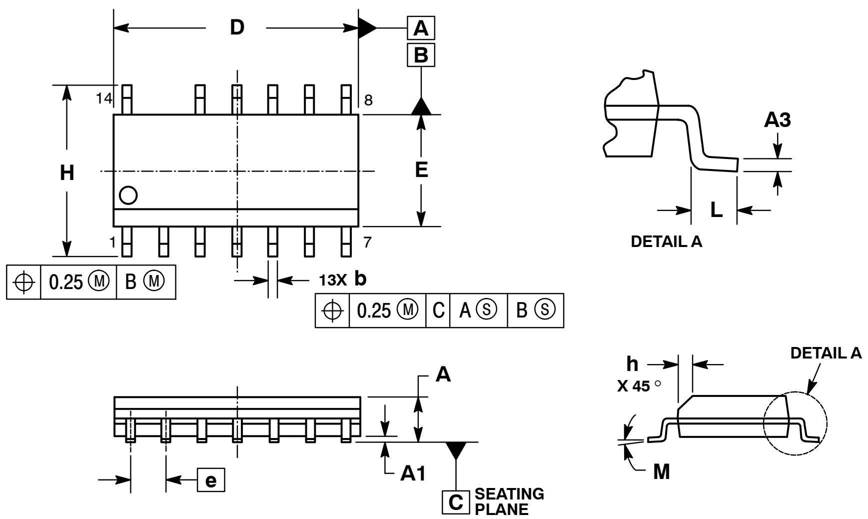
SOIC−16 NB, LESS PIN 13
CASE 751AM−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

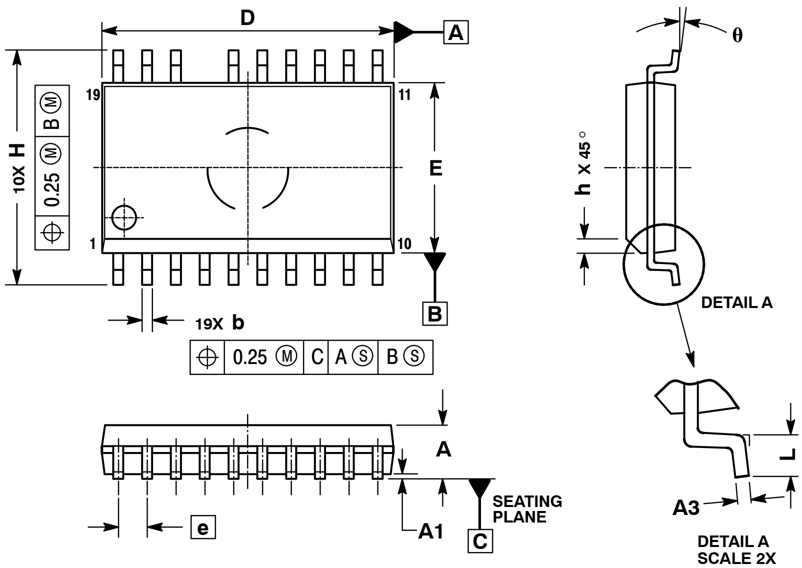
SOIC−14 NB, LESS PIN 13
CASE 751AN−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
A3	0.19	0.25
b	0.35	0.49
D	8.55	8.75
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

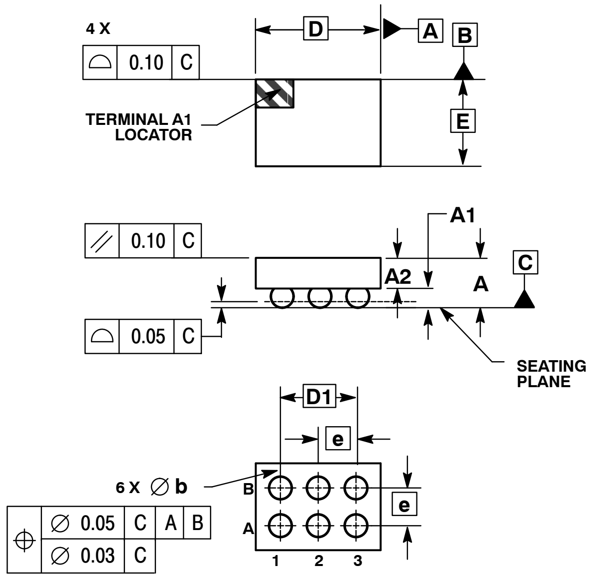
SOIC−20 WB, LESS PIN 17 (SO−19)
CASE 752AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
A3	0.23	0.32
b	0.35	0.49
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

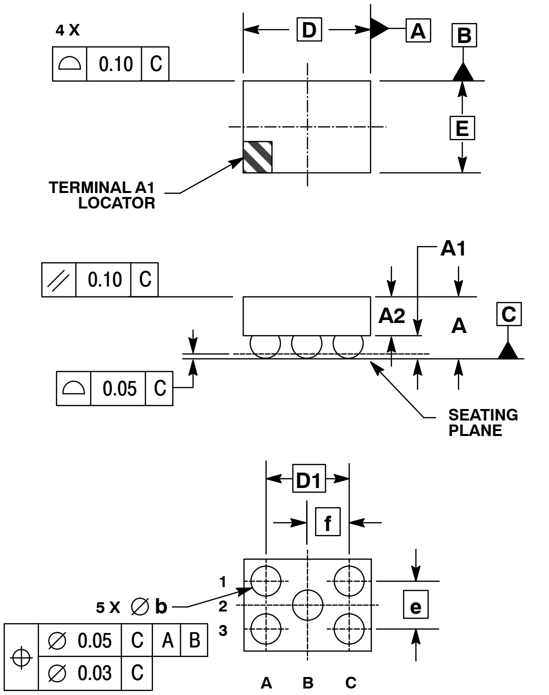
6−PIN FLIP−CHIP
CASE 766AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.660
A1	0.210	0.270
A2	0.380	0.430
D	1.650 BSC	
E	1.150 BSC	
b	0.290	0.340
e	0.500 BSC	
D1	1.000 BSC	

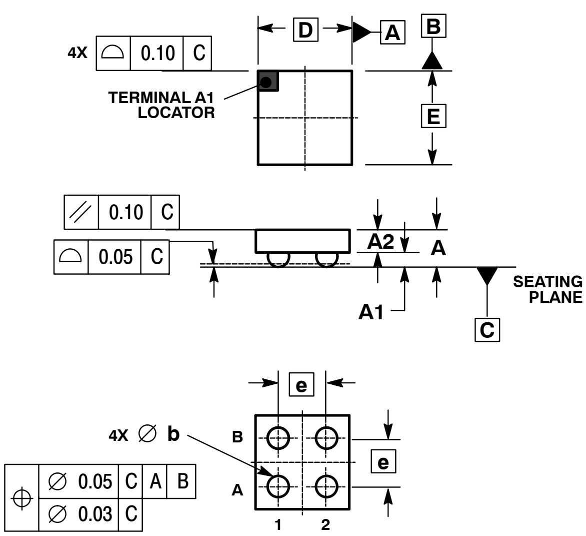
5−PIN FLIP−CHIP
CASE 766AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	---	0.680
A1	0.210	0.270
A2	0.380	0.430
D	1.330 BSC	
E	0.960 BSC	
b	0.290	0.340
e	0.500 BSC	
f	0.433 BSC	
D1	0.866 BSC	

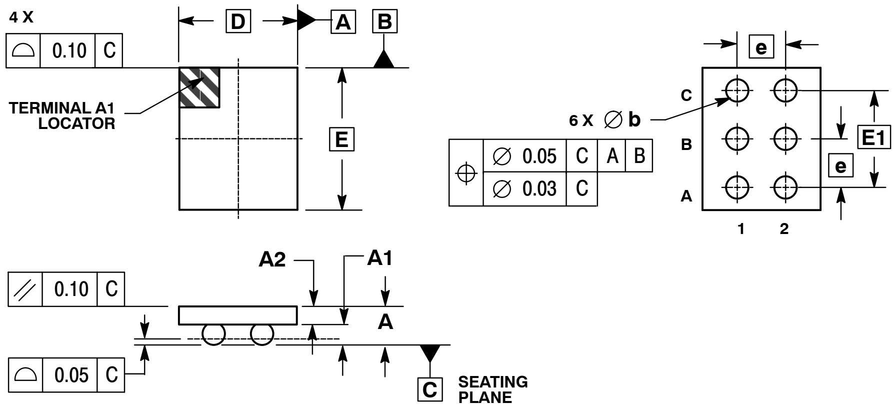
4−PIN FLIP−CHIP
CASE 766AC−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS IN COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	---	0.630
A1	0.250	0.310
A2	0.290	0.320
D	1.550 BSC	
E	1.550 BSC	
b	0.330	0.390
e	0.800 BSC	

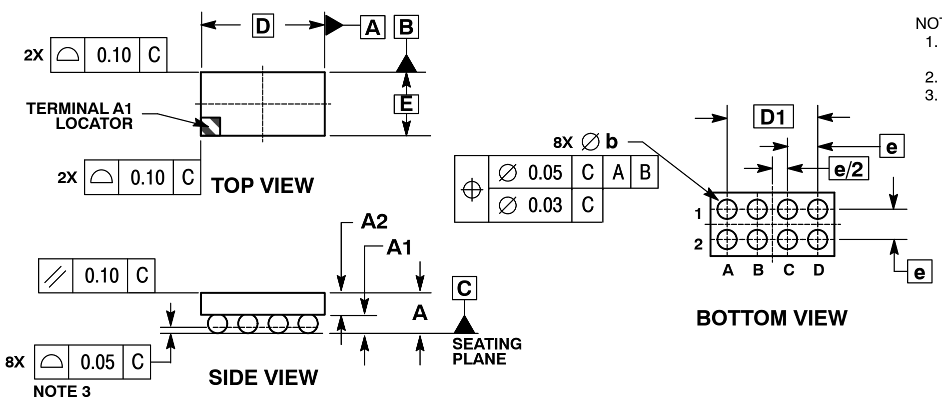
6−PIN FLIP−CHIP
CASE 766AD−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.630
A1	0.250	0.310
A2	0.290	0.320
D	1.950 BSC	
E	2.350 BSC	
E1	1.600 BSC	
b	0.330	0.390
e	0.800 BSC	

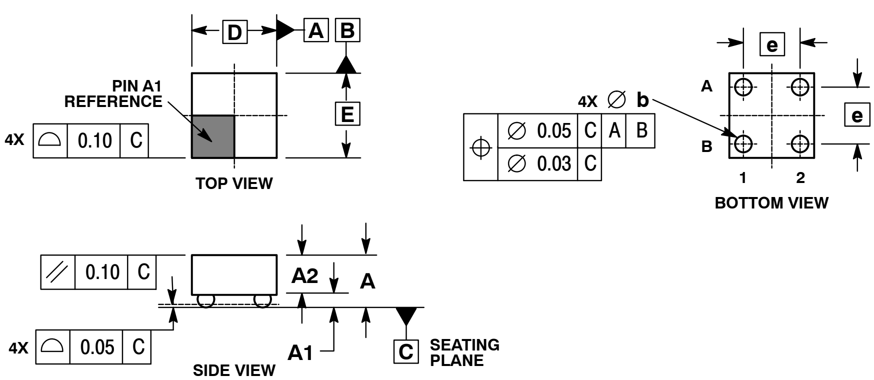
8−PIN FLIP−CHIP
CASE 766AE−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.655
A1	0.210	0.270
A2	0.335	0.385
b	0.290	0.340
D	2.050 BSC	
D1	1.500 BSC	
E	1.050 BSC	
e	0.500 BSC	

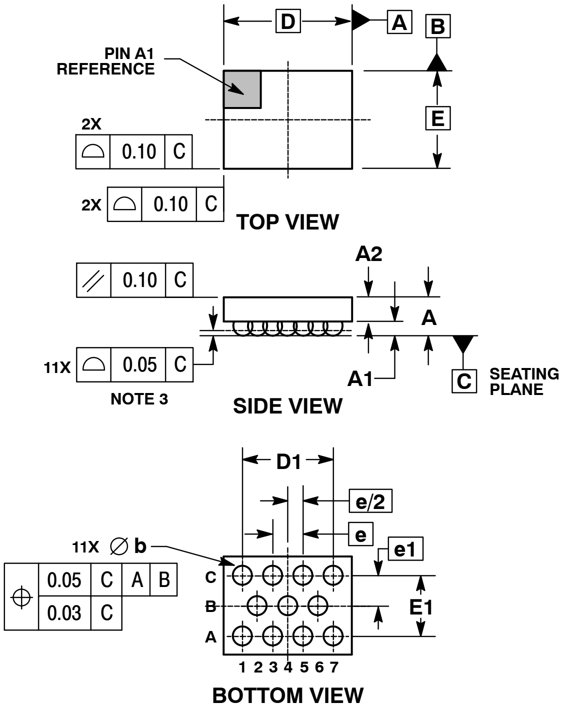
4−PIN FLIP−CHIP
CASE 766AF−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	−−−	0.692	0.742
A1	0.142	0.167	0.192
A2	0.500	0.525	0.550
b	0.190	0.220	0.224
D	1.118 BSC		
E	1.118 BSC		
e	0.750 BSC		

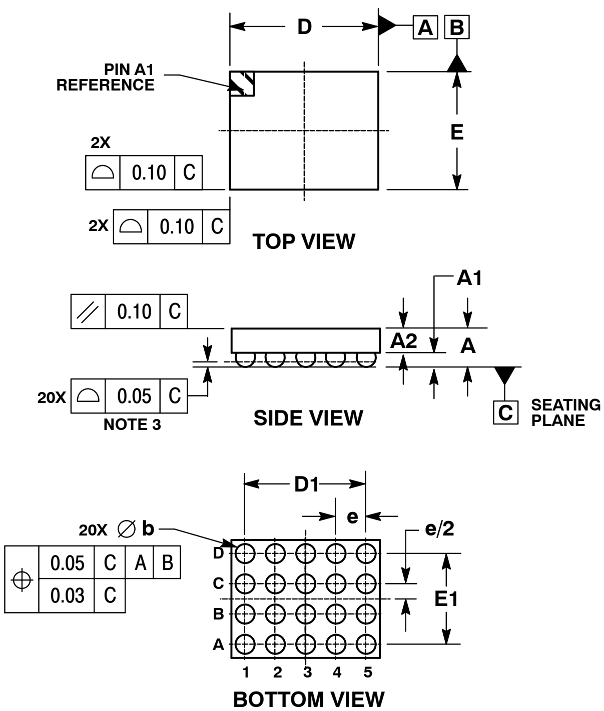
11−PIN FLIP−CHIP
CASE 766AJ−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.66
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.04 BSC	
D1	1.50 BSC	
E	1.41 BSC	
E1	0.86 BSC	
e	0.50 BSC	
e1	0.43 BSC	

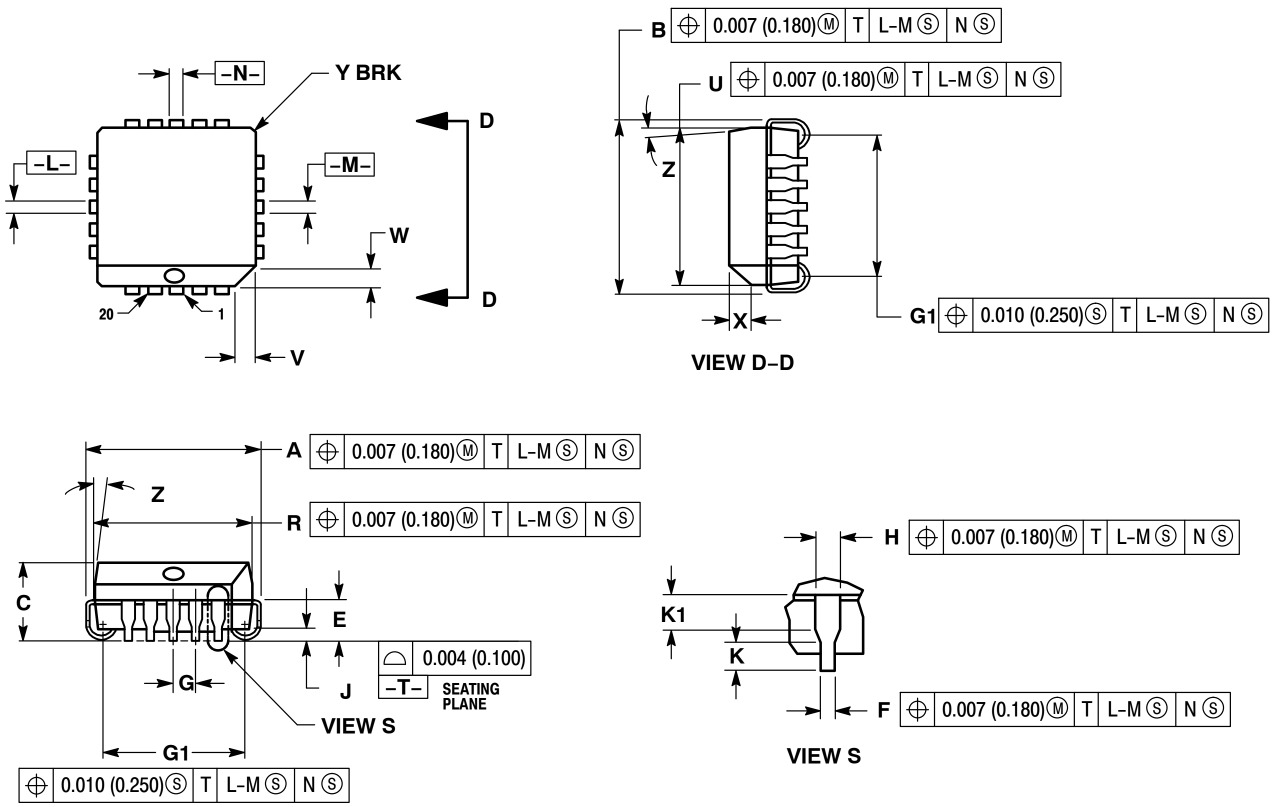
20−PIN FLIP−CHIP
CASE 766AK−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.66
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.54 BSC	
D1	2.00 BSC	
E	2.03 BSC	
E1	1.50 BSC	
e	0.50 BSC	

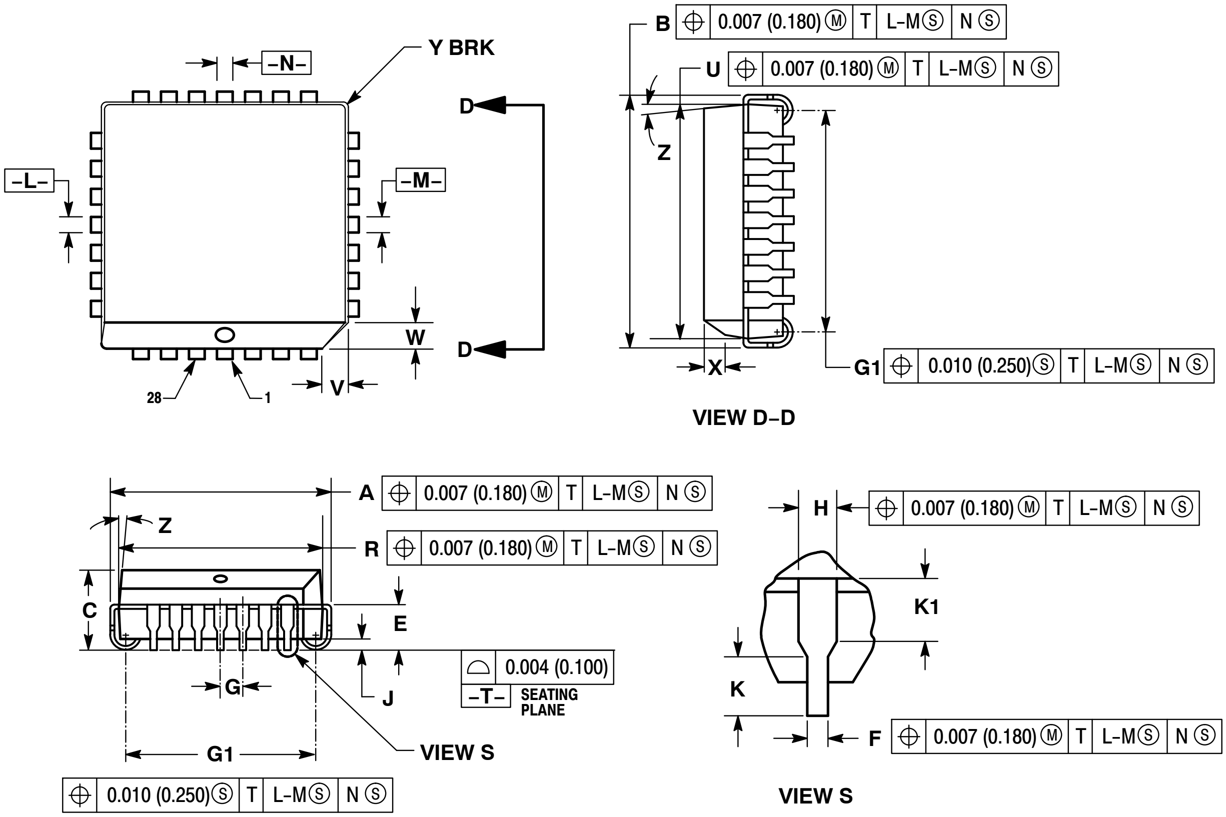
PLCC−20
CASE 775−02
ISSUE E



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

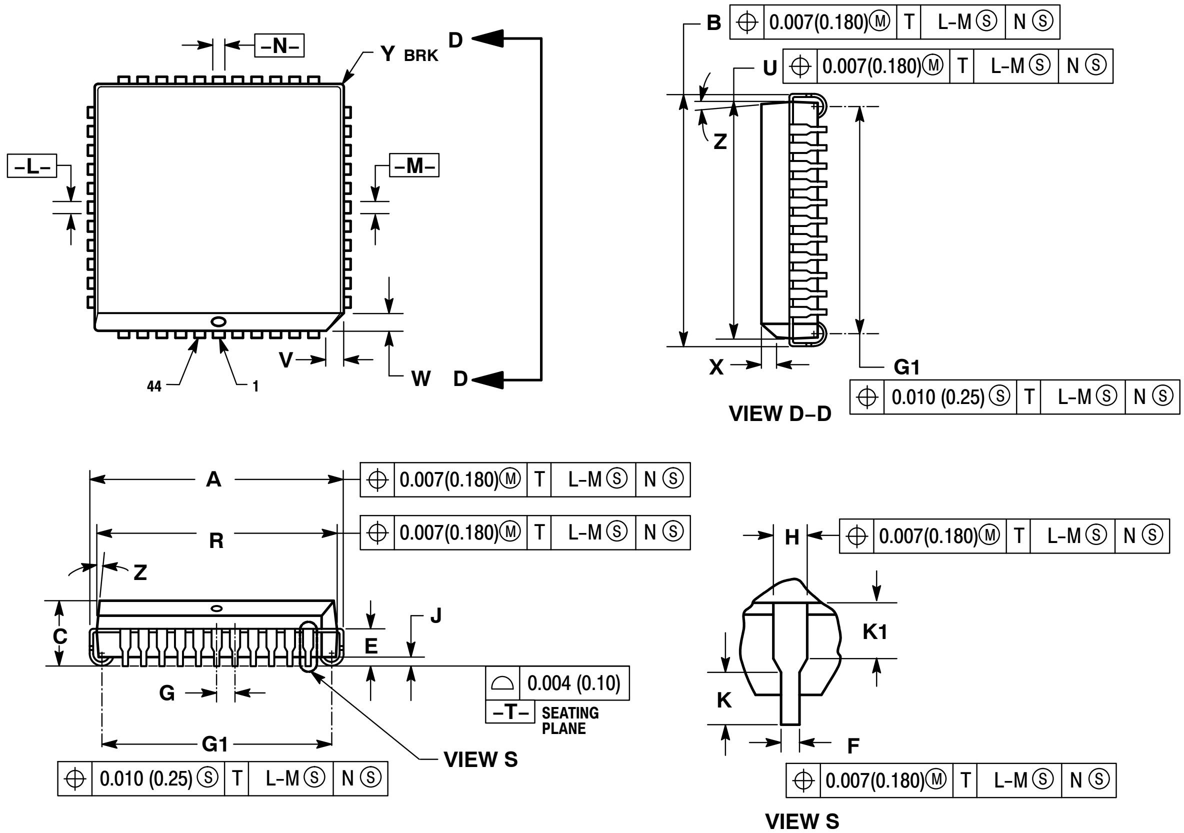
PLCC−28
CASE 776−02
ISSUE E



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

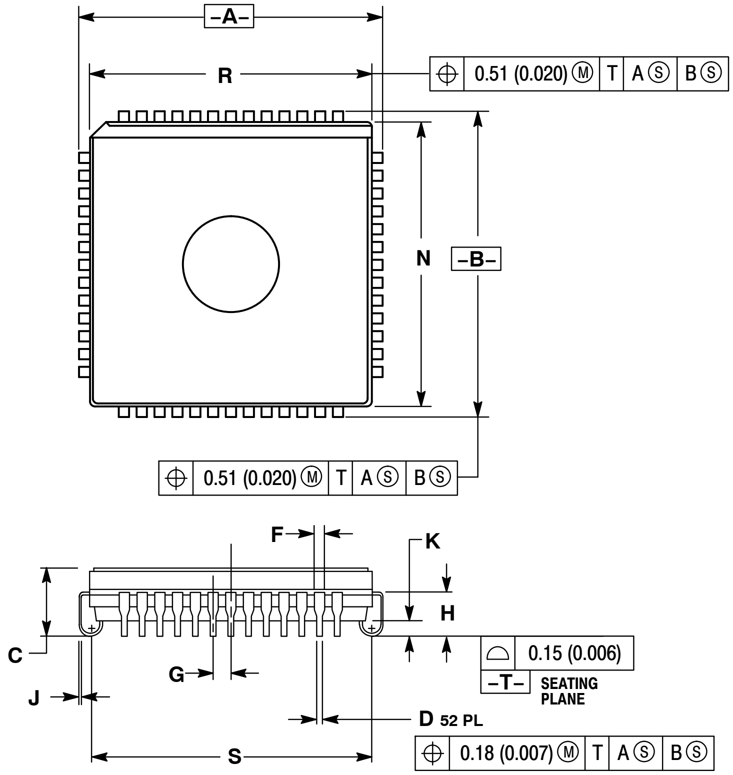
PLCC−44
CASE 777−02
ISSUE D



NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	---	1.02	---

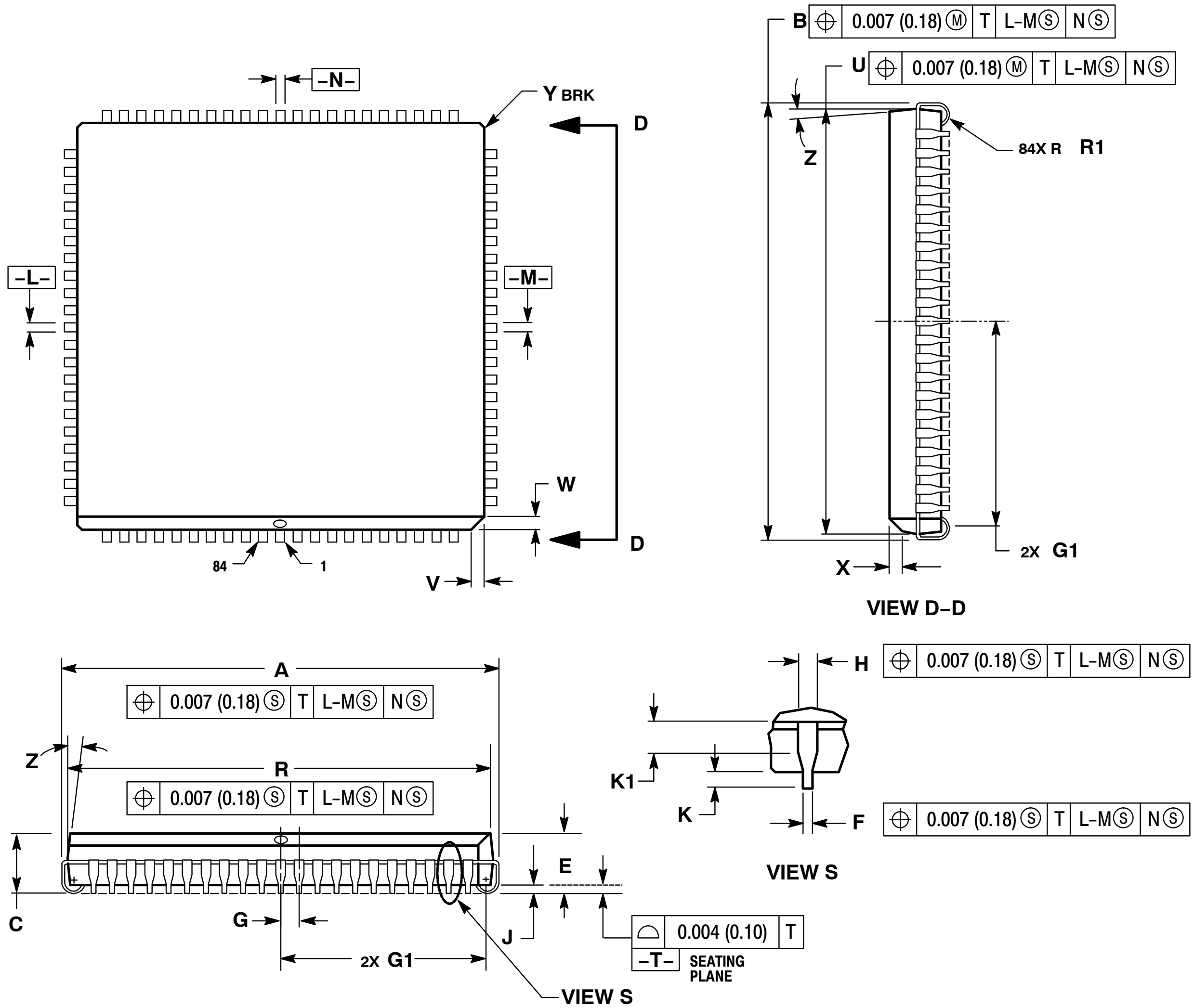
PLCC−52
CASE 778B−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R AND N DO NOT INCLUDE GLASS PROTRUSION. GLASS PROTRUSION TO BE 0.25 (0.010) MAXIMUM.
4. ALL DIMENSIONS AND TOLERANCES INCLUDE LEAD TRIM OFFSET AND LEAD FINISH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.200	4.20	5.08
D	0.017	0.021	0.44	0.53
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
H	0.090	0.130	2.29	3.30
J	0.006	0.010	0.16	0.25
K	0.035	0.045	0.89	1.14
N	0.735	0.756	18.67	19.20
R	0.735	0.756	18.67	19.20
S	0.690	0.730	17.53	18.54

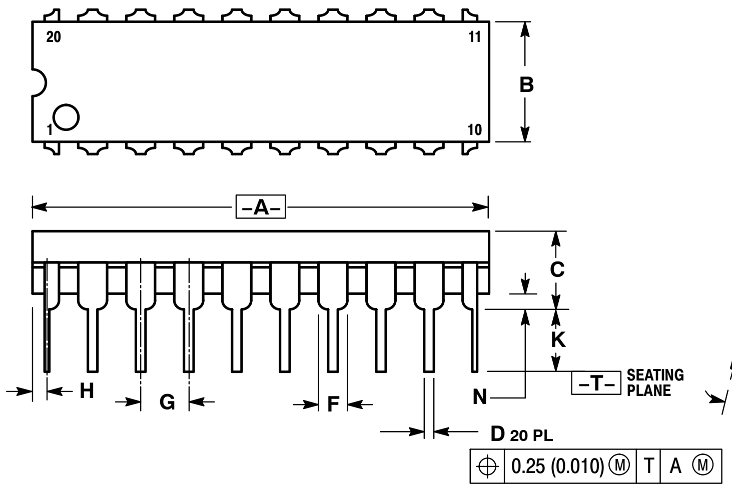
PLCC−84
CASE 780−01
ISSUE B

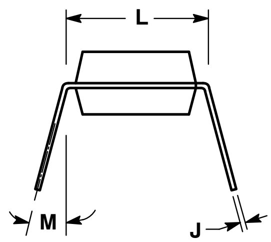


NOTES:
1. DATUMS L, M, AND N DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PACKAGE BODY AT MOLD PARTING LINE.
2. DIMENSION G1 TO BE MEASURED AT CLOSEST APPROACH OF LEAD TO DATUM T, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.94). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.185	1.195	30.10	30.35
B	1.185	1.195	30.10	30.35
C	0.165	0.180	4.20	4.57
E	0.090	0.120	2.29	3.05
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	1.150	1.156	29.21	29.36
U	1.150	1.156	29.21	29.36
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.545	0.565	13.84	14.35
K1	0.060	---	1.52	---
R1	0.025	0.045	0.64	1.14

PDIP−20
CASE 804−01
ISSUE A

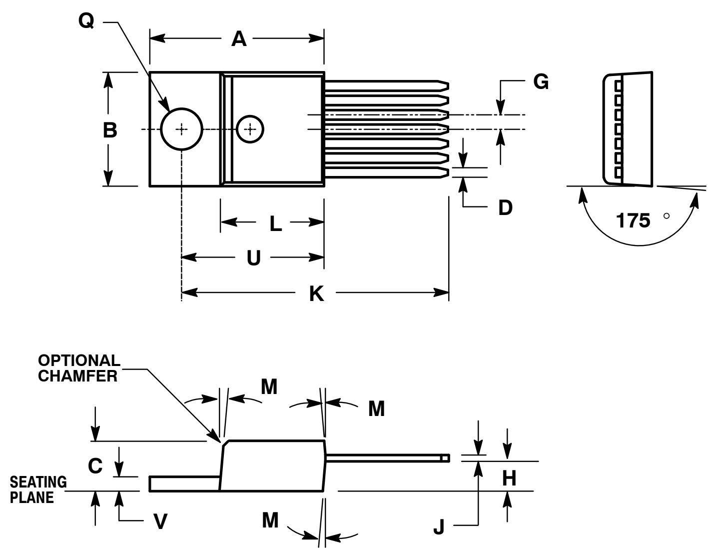




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.930	0.970	23.63	24.63
B	0.240	0.260	6.10	6.60
C	0.150	0.170	3.81	4.31
D	0.015	0.022	0.38	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.030 NOM		0.76 NOM	
J	0.009	0.013	0.23	0.33
K	0.115	0.140	2.93	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

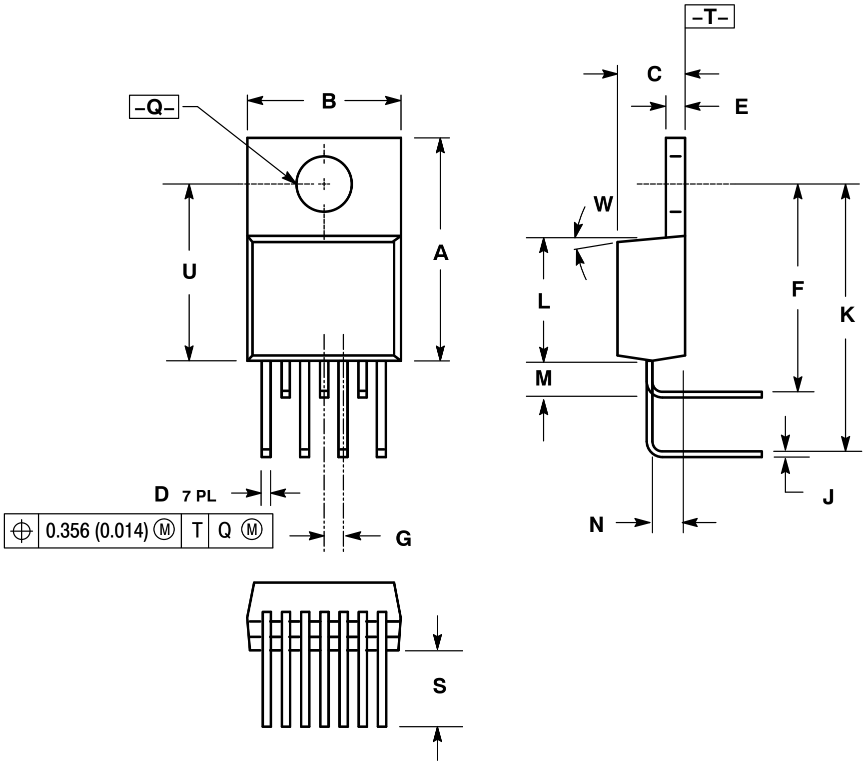
TO−220 7−LEAD
CASE 821E−04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. 821E−01 THRU 821−03 OBSOLETE, NEW STANDARD 821E−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.600	0.610	15.24	15.49
B	0.386	0.403	9.80	10.23
C	0.170	0.180	4.32	4.56
D	0.028	0.037	0.71	0.94
G	0.045	0.055	1.15	1.39
H	0.088	0.102	2.24	2.59
J	0.018	0.026	0.46	0.66
K	1.028	1.042	26.11	26.47
L	0.355	0.365	9.02	9.27
M	5° NOM		5° NOM	
Q	0.142	0.148	3.61	3.75
U	0.490	0.501	12.45	12.72
V	0.045	0.055	1.15	1.39

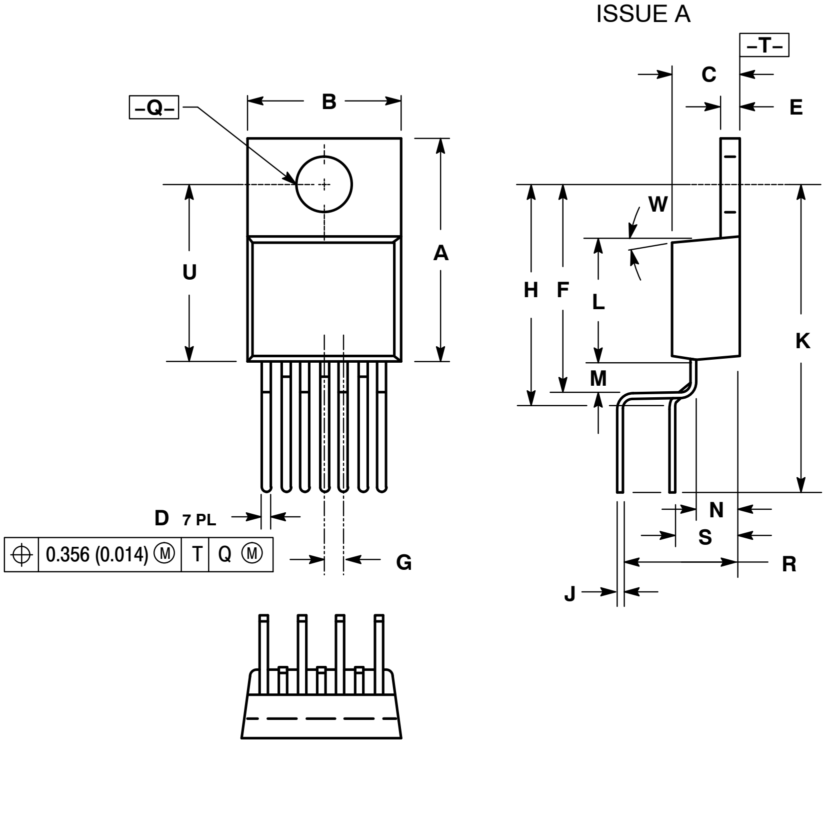
TO−220 7−LEAD (THA7)
CASE 821H−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.
5. LEADS MAINTAIN A RIGHT ANGLE WITH RESPECT TO THE PACKAGE BODY TO WITH ± 0.020”.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.568	0.583	14.43	14.81
G	0.050 BSC		1.27 BSC	
J	0.015	0.022	0.38	0.56
K	0.728	0.743	18.49	18.87
L	0.322	0.337	8.18	8.56
M	0.101	0.116	2.57	2.95
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
S	0.150	0.200	3.81	5.08
U	0.460	0.475	11.68	12.07
W	3°		3°	

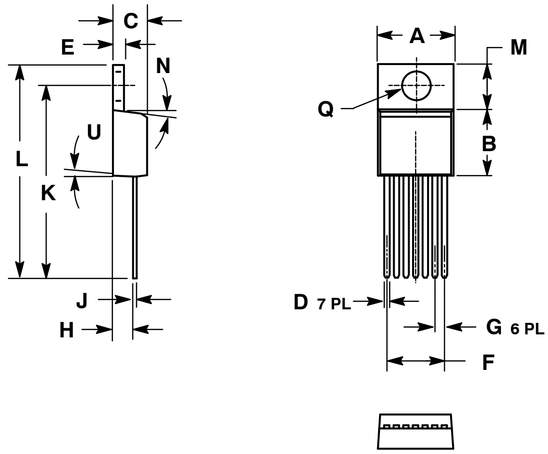
TO−220 7−LEAD (TVA7)
CASE 821J−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.77	10.54
C	0.160	0.190	4.06	4.82
D	0.023	0.037	0.58	0.94
E	0.045	0.055	1.14	1.40
F	0.540	0.555	13.72	14.10
G	0.050 BSC		1.27 BSC	
H	0.570	0.595	14.48	15.11
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.322	0.337	8.18	8.56
M	0.073	0.088	1.85	2.24
N	0.090	0.115	2.28	2.91
Q	0.146	0.156	3.70	3.95
R	0.289	0.304	7.34	7.72
S	0.164	0.179	4.17	4.55
U	0.460	0.475	11.68	12.07
W	3°		3°	

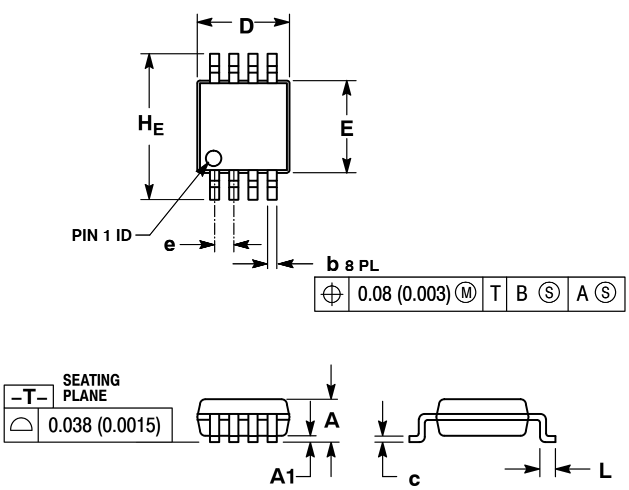
TO−220 7−LEAD
CASE 821P−03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. 821P−01 AND −02 OBSOLETE. NEW STANDARD IS 821P−03.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.54	0.390	0.415
B	8.23	9.40	0.324	0.370
C	4.19	4.83	0.165	0.190
D	0.66	0.81	0.026	0.032
E	0.89	1.40	0.035	0.055
F	7.62 TYP		0.3 TYP	
G	1.22	1.32	0.048	0.052
H	2.16	2.92	0.085	0.115
J	0.30	0.64	0.012	0.025
K	24.00	26.54	0.945	1.045
L	26.67	29.03	1.050	1.143
M	6.10	6.48	0.240	0.255
N	7°	---	7°	---
Q	3.53	3.96	0.139	0.156
U	4°	6°	4°	6°

Micro8™
MSOP−8
CASE 846A−02
ISSUE H



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

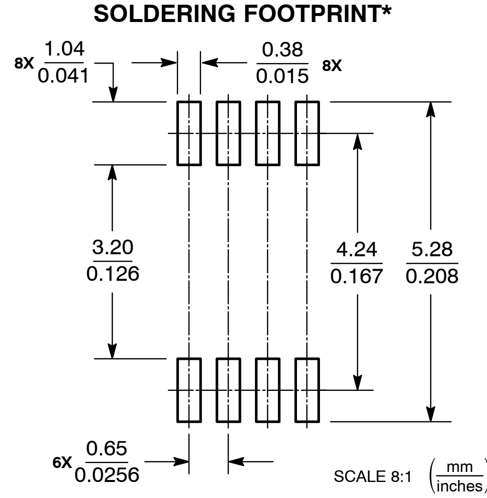
DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX	INCHES MIN	INCHES NOM	INCHES MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

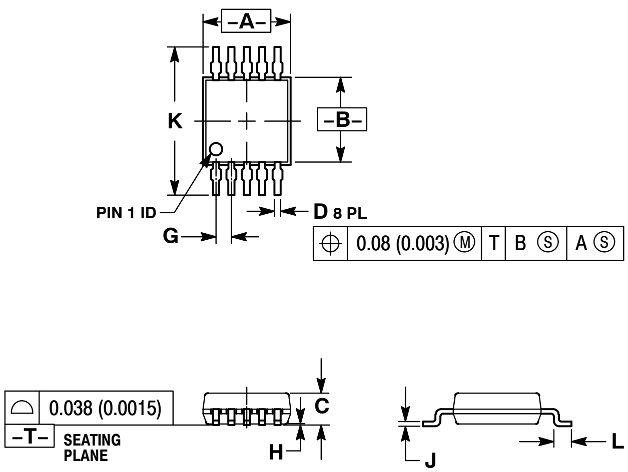
STYLE 3:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

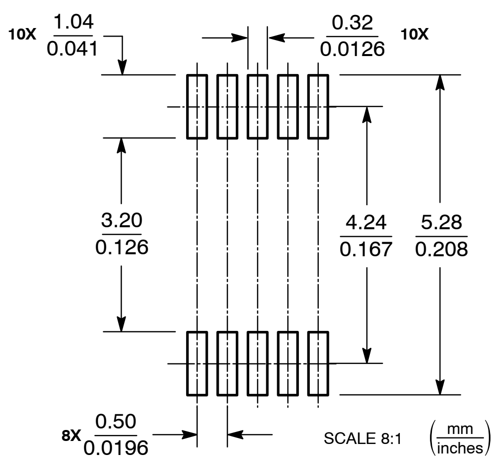
Micro10
CASE 846B−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

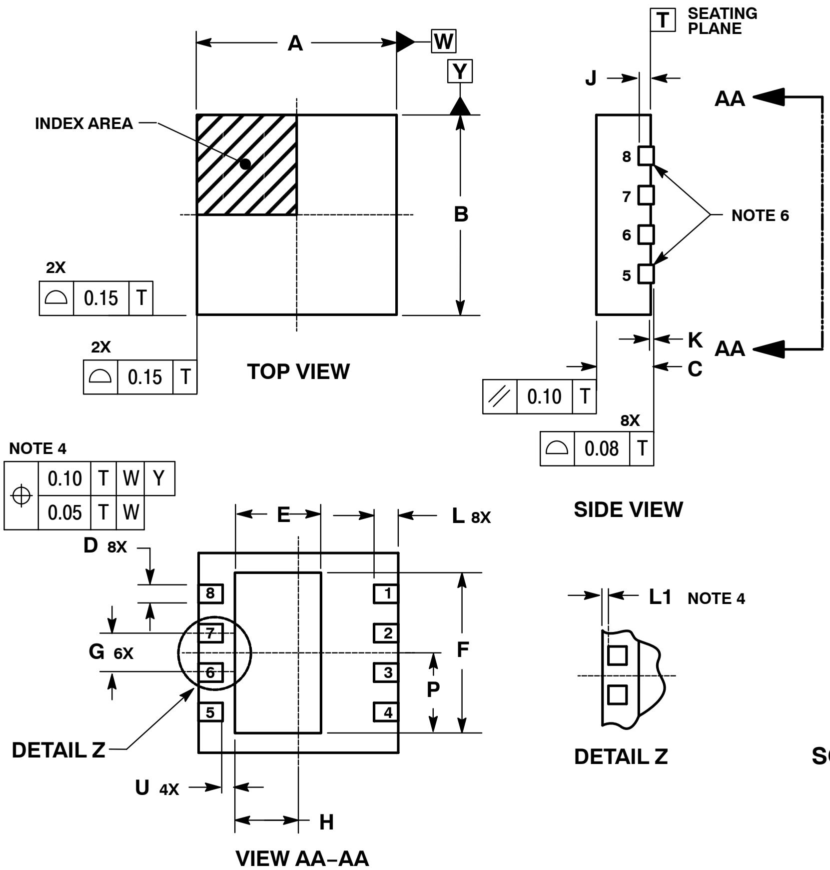
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT



Micro10

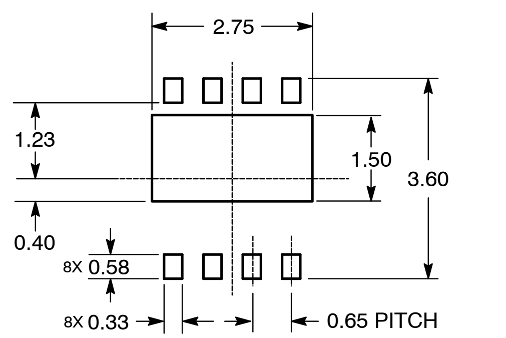
Micro8 LEADLESS
CASE 846C−01
ISSUE C



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95−1 SPP−012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
4. DIMENSION D APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 0.30 MM FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1 MM IS ACCEPTABLE. L1 IS OPTIONAL.
5. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
6. OPTIONAL SIDE VIEW CAN SHOW LEADS 5 AND 8 REMOVED.

	MILLIMETERS	
DIM	MIN	MAX
A	3.30 BSC	
B	3.30 BSC	
C	0.85	0.95
D	0.25	0.35
E	1.30	1.50
F	2.55	2.75
G	0.65 BSC	
H	0.95	1.15
J	0.25 BSC	
K	0.00	0.05
L	0.35	0.45
L1	0.00	0.10
P	1.28	1.38
U	0.17 TYP	

SOLDERING FOOTPRINT*

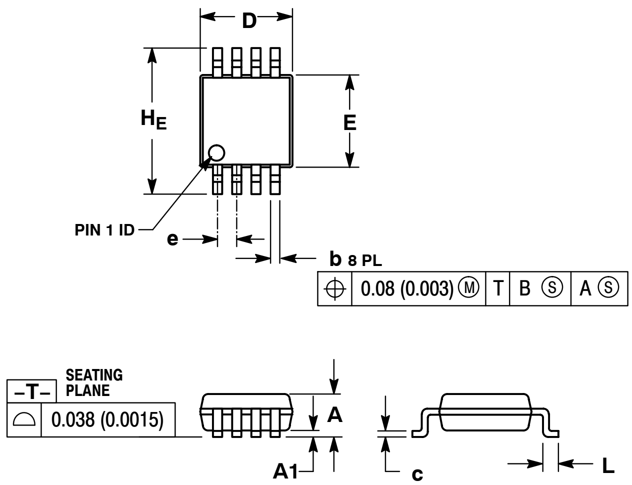


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Micro8 /TSSOP8, 3x3

CASE 846AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

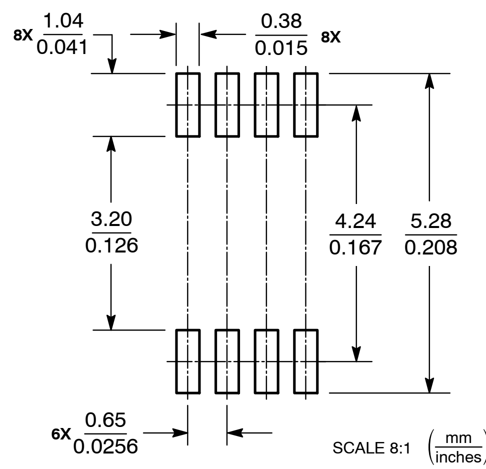
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

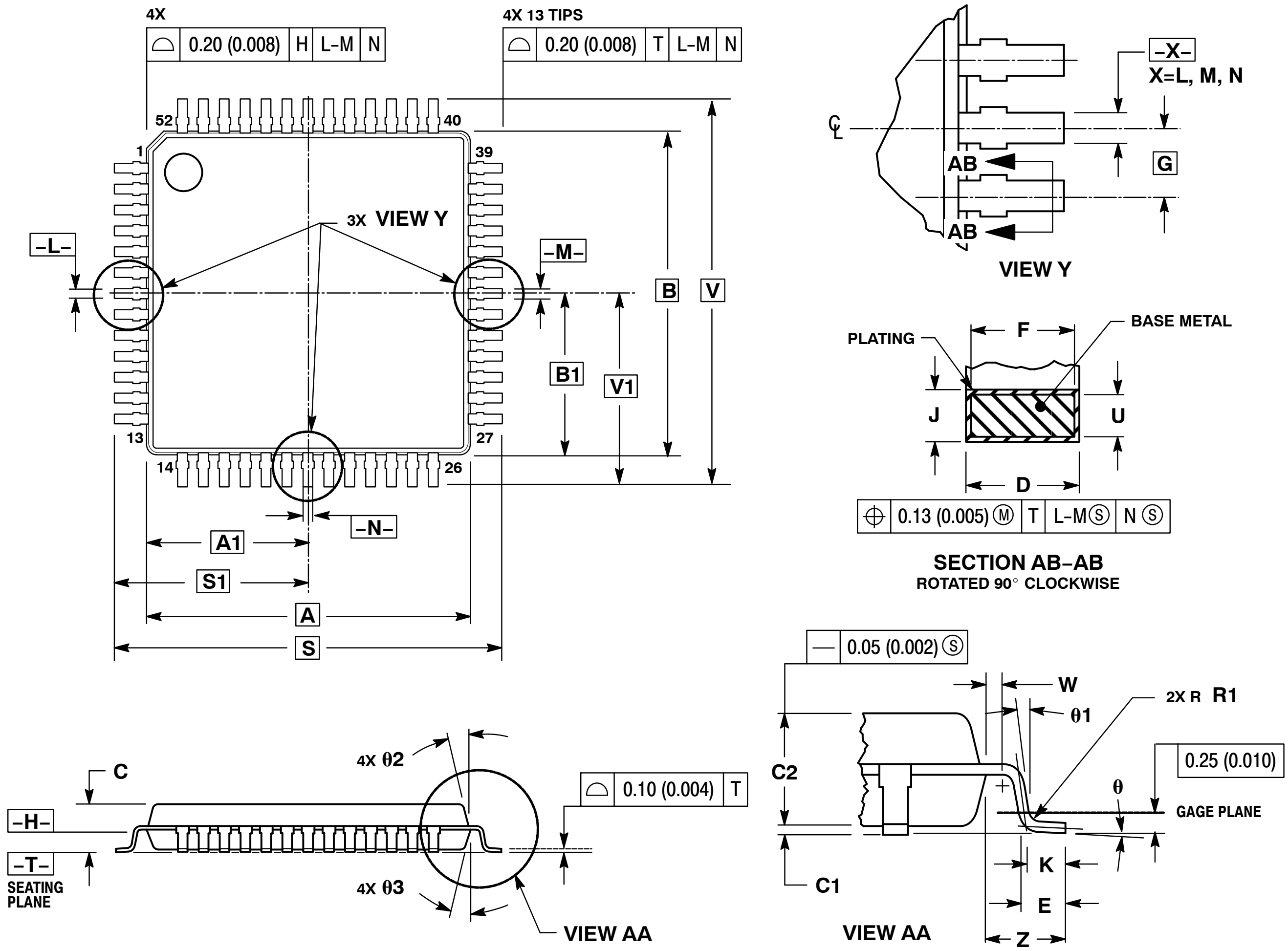
STYLE 3:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

LQFP−52
CASE 848D−02
ISSUE D



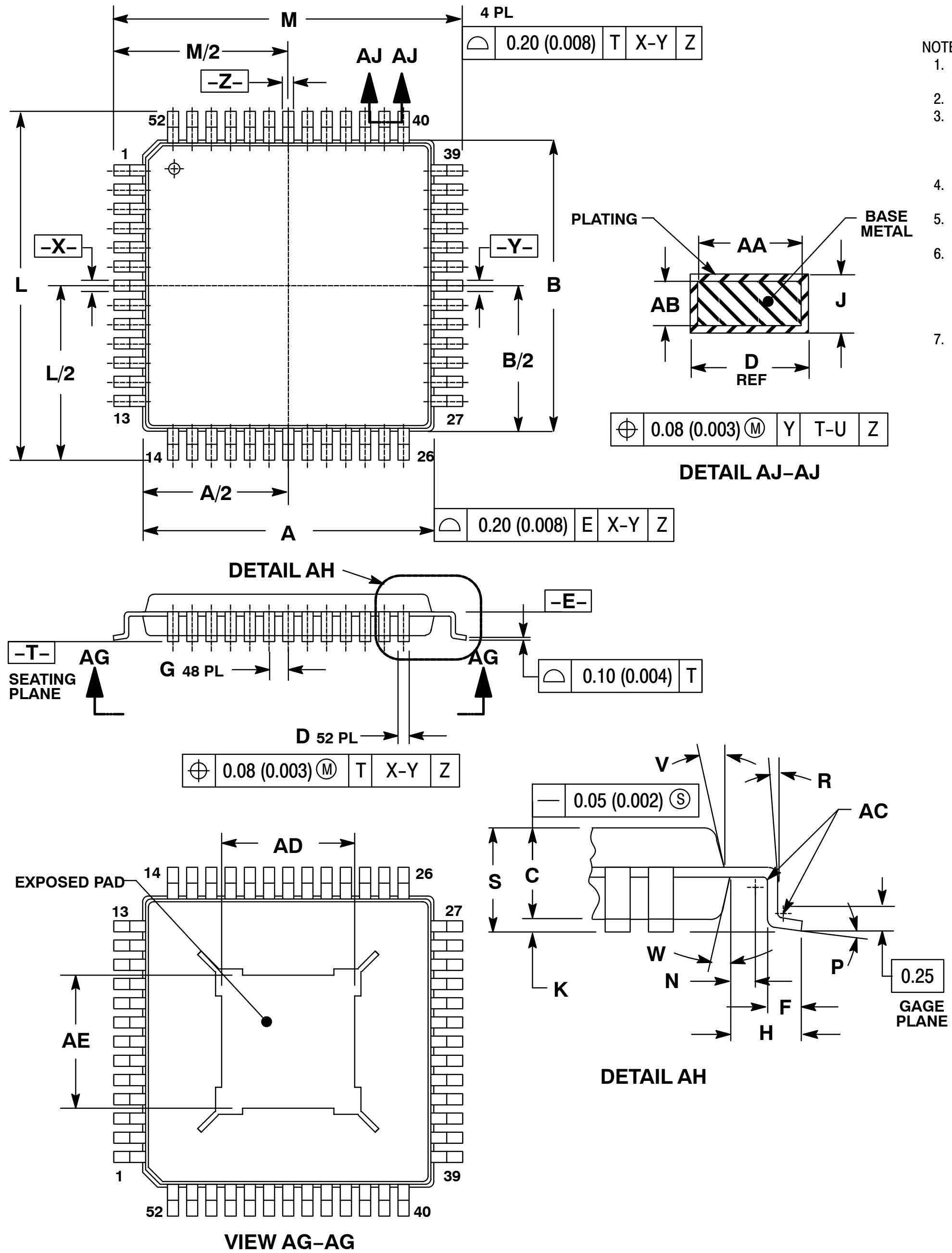
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	---	0°	---
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

LQFP−52 EXPOSED PAD

CASE 848H−01

ISSUE A



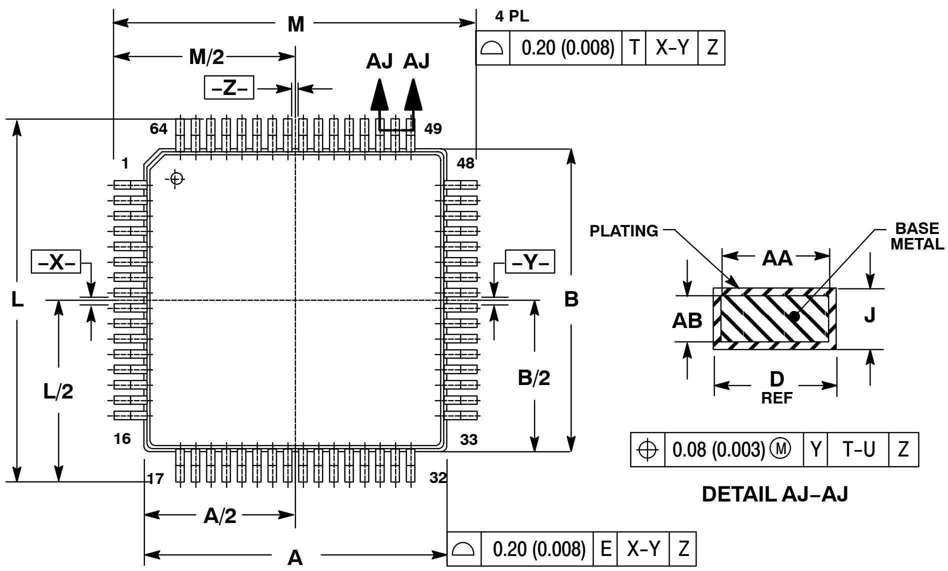
NOTES:

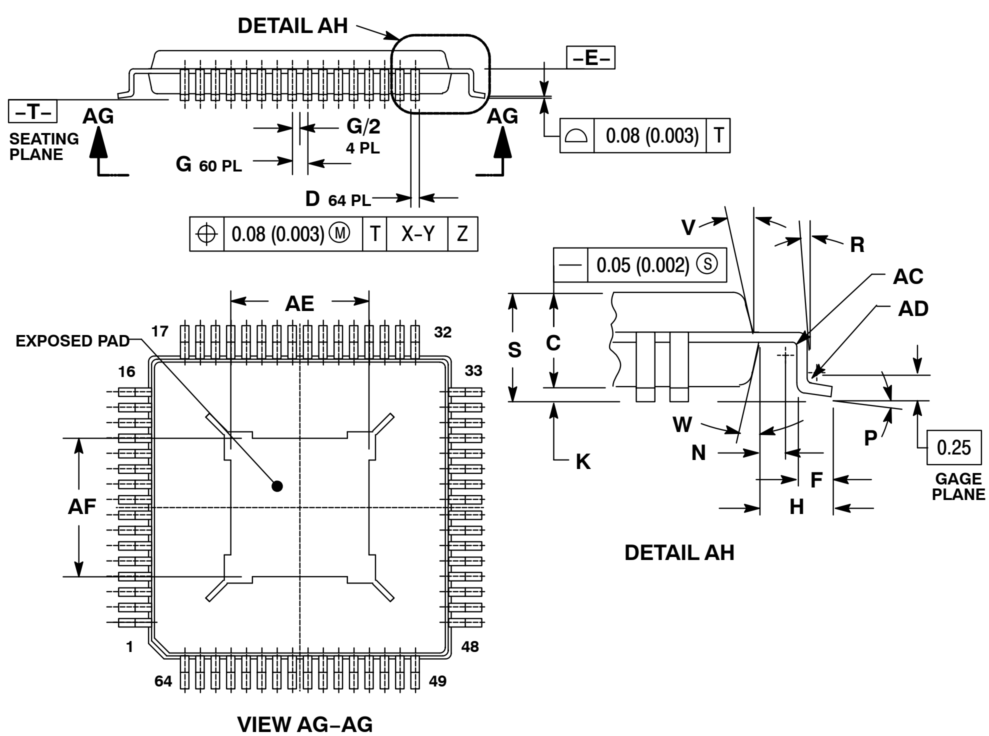
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM PLANE “E” IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
4. DATUM “X”, “Y” AND “Z” TO BE DETERMINED AT DATUM PLANE DATUM “E”.
5. DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM “T”.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLAND “E”.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
B	10.00 BSC		0.394 BSC	
C	1.30	1.50	0.051	0.059
D	0.22	0.40	0.009	0.016
F	0.45	0.75	0.018	0.030
G	0.65 BSC		0.026 BSC	
H	1.00 REF		0.039 BSC	
J	0.09	0.20	0.004	0.008
K	0.05	0.20	0.002	0.008
L	12.00 BSC		0.472 BSC	
M	12.00 BSC		0.472 BSC	
N	0.20 REF		0.008 REF	
P	0 °	7 °	0 °	7 °
R	0 °	---	0 °	---
S	---	1.70	---	0.067
V	12 ° REF		12 ° REF	
W	12 ° REF		12 ° REF	
AA	0.20	0.35	0.008	0.014
AB	0.07	0.16	0.003	0.006
AC	0.08	0.20	0.003	0.008
AD	4.58	4.78	0.180	0.188
AE	4.58	4.78	0.180	0.188

LQFP−64 EXPOSED PAD

CASE 848G−02
ISSUE A

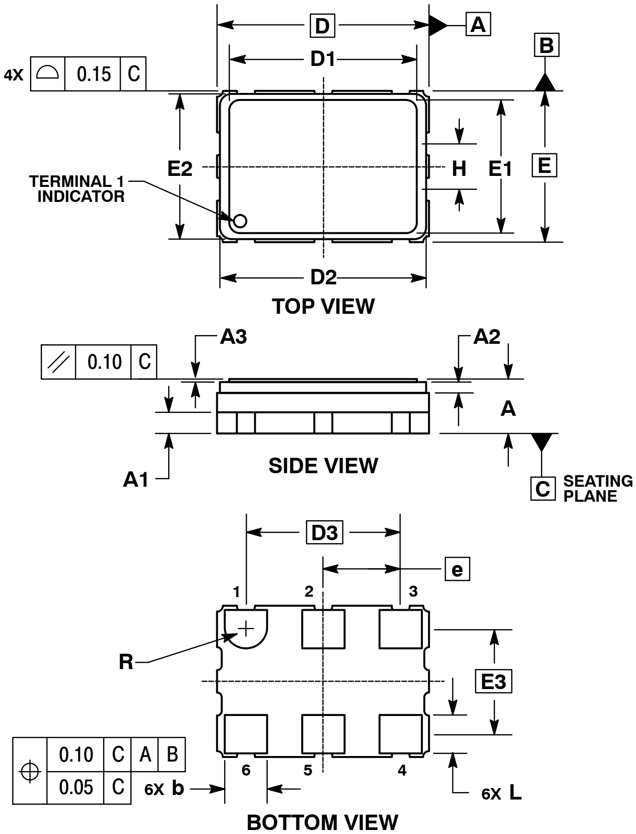




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM PLANE “E” IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING PLANE.
4. DATUM “X”, “Y” AND “Z” TO BE DETERMINED AT DATUM PLANE DATUM “E”.
5. DIMENSIONS M AND L TO BE DETERMINED AT SEATING PLANE DATUM “T”.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLAND “E”.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
B	10.00 BSC		0.394 BSC	
C	1.35	1.45	0.053	0.057
D	0.17	0.27	0.007	0.011
F	0.45	0.75	0.018	0.030
G	0.50 BSC		0.020 BSC	
H	1.00 REF		0.039 BSC	
J	0.09	0.20	0.004	0.008
K	0.05	0.15	0.002	0.006
L	12.00 BSC		0.472 BSC	
M	12.00 BSC		0.472 BSC	
N	0.20	---	0.008	---
P	0 °	7 °	0 °	7 °
R	0 °	---	0 °	---
S	---	1.60	---	0.063
V	11 °	13 °	11 °	13 °
W	11 °	13 °	11 °	13 °
AA	0.17	0.23	0.007	0.009
AB	0.09	0.16	0.004	0.006
AC	0.08	---	0.003	---
AD	0.08	---	0.003	---
AE	4.50	4.78	0.180	0.188
AF	4.50	4.78	0.180	0.188

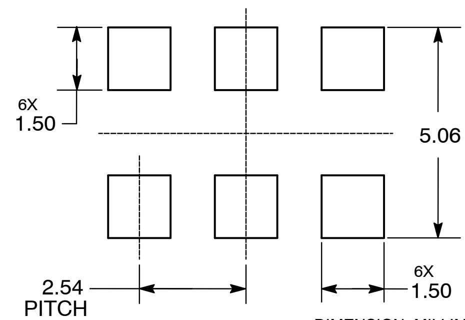
6 PIN CLCC, 7x5, 2.54P
CASE 848AB−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

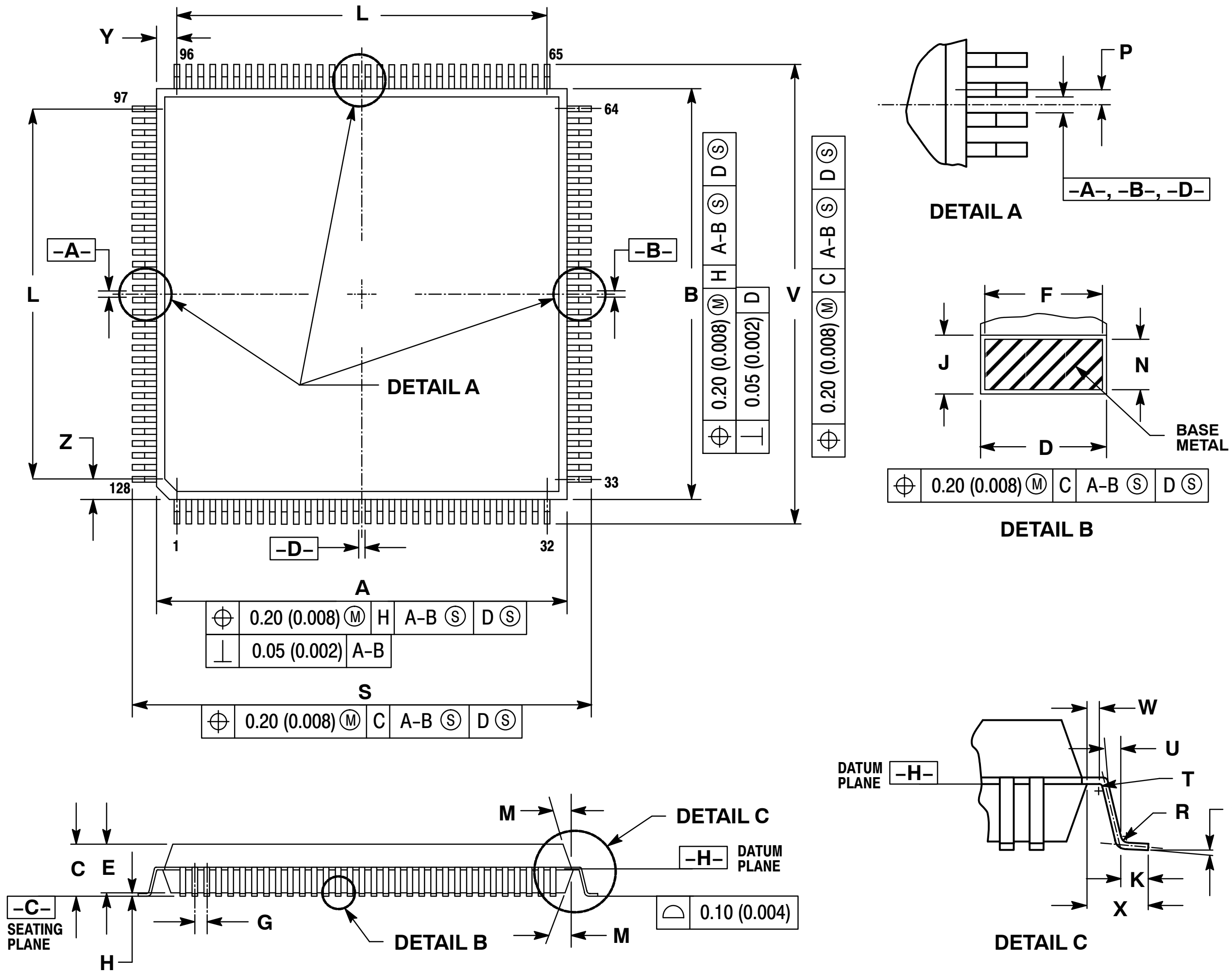
DIM	MILLIMETERS MIN	NOM	MAX
A	1.70	1.80	1.90
A1		0.70 REF	
A2		0.36 REF	
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D		7.00 BSC	
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3		5.08 BSC	
E		5.00 BSC	
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3		3.49 BSC	
e		2.54 BSC	
H		1.80 REF	
L	1.17	1.27	1.37
R		0.70 REF	

SOLDERING FOOTPRINT



DIMENSION: MILLIMETERS

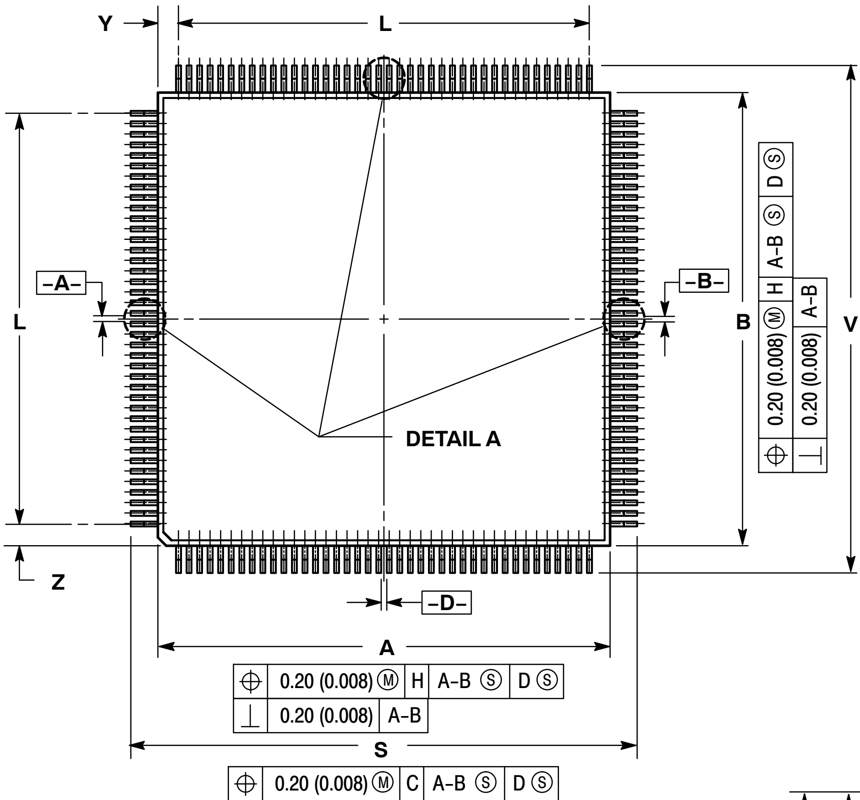
QFP−128
CASE 862A−02
ISSUE B

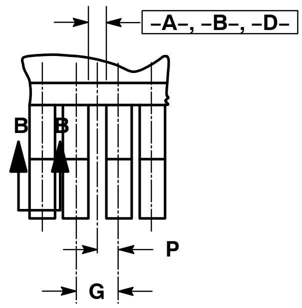


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D-TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

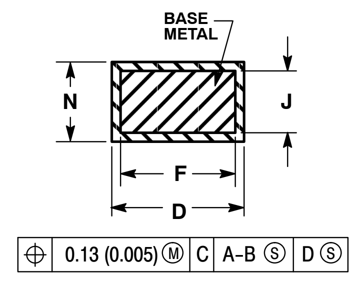
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	---	4.07	---	0.160
D	0.30	0.45	0.012	0.018
E	3.17	3.67	0.125	0.144
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.032 BSC	
H	0.25	0.35	0.010	0.014
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	24.80 REF		0.976 REF	
M	5 °	16 °	5 °	16 °
N	0.13	0.17	0.005	0.007
P	0.40 BSC		0.016 BSC	
Q	0 °	7 °	0 °	7 °
R	0.13	0.30	0.005	0.012
S	30.95	31.45	1.219	1.238
T	0.13	---	0.005	---
U	0 °	---	0 °	---
V	30.95	31.45	1.219	1.238
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.60 REF		0.063 REF	
Z	1.60 REF		0.063 REF	

QFP−160
CASE 864A−03
ISSUE C

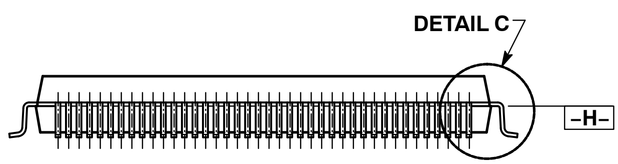


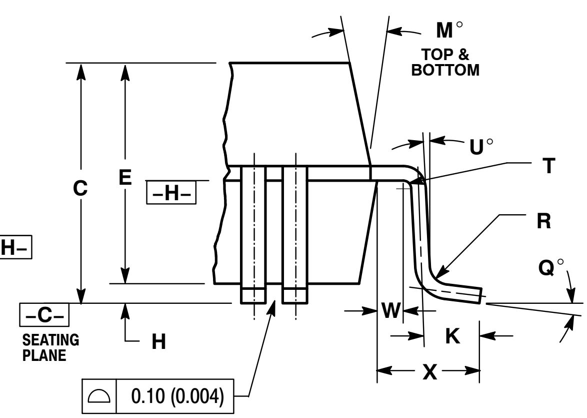


DETAIL A



SECTION B−B



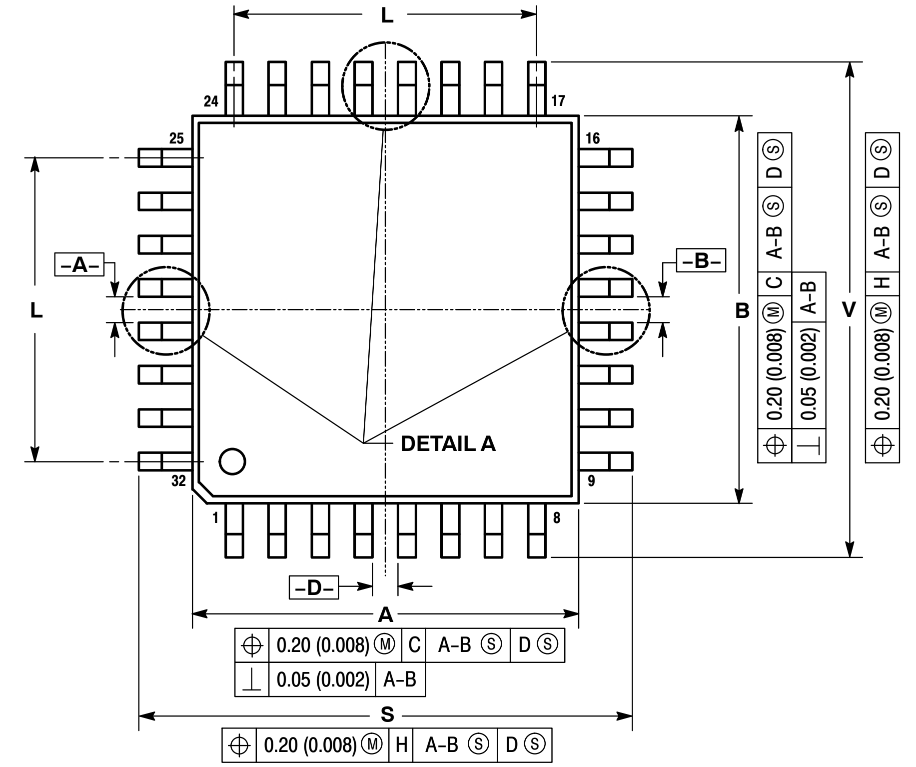


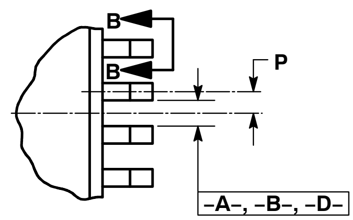
DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

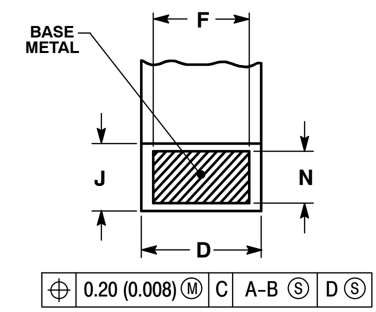
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.00	31.40	1.220	1.236
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

TQFP−32
CASE 873−01
ISSUE A

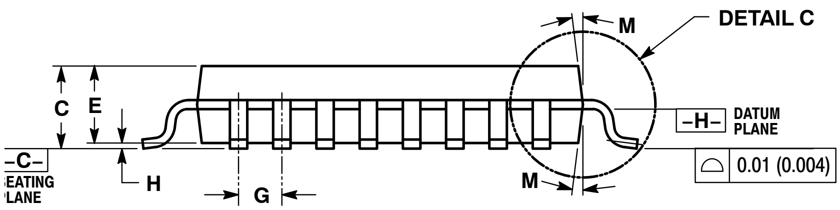


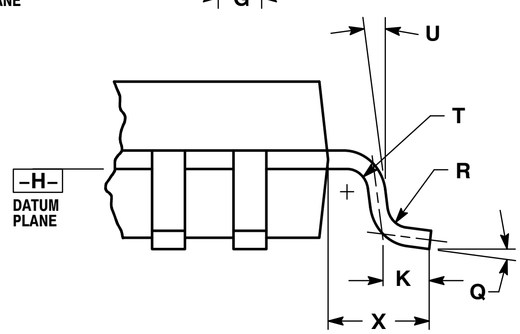


DETAIL A



SECTION B−B
VIEW ROTATED 90° CLOCKWISE



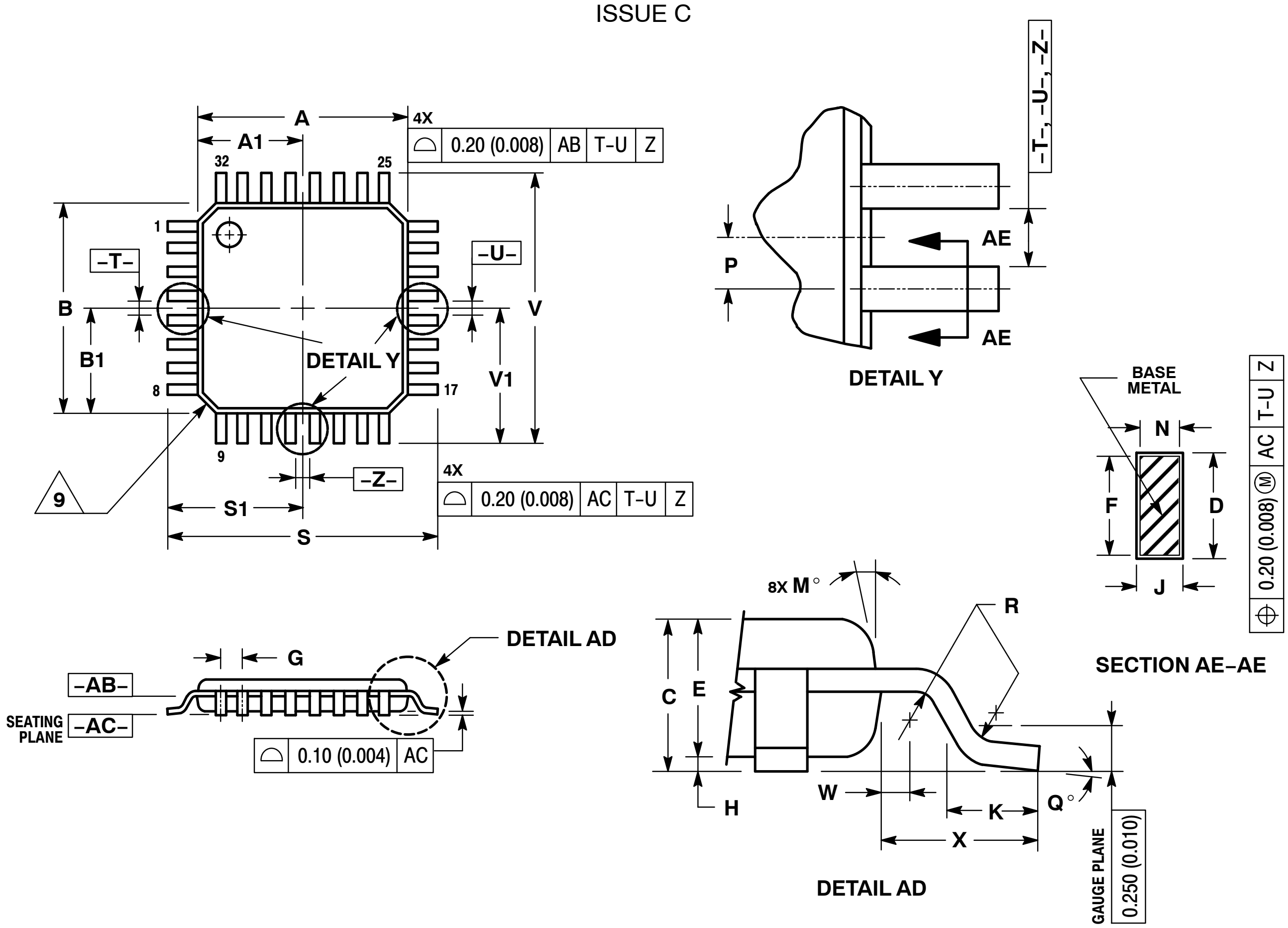


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS −A−, −B− AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	---	0.010	---
G	0.80 BSC		0.031 BSC	
H	---	0.20	---	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

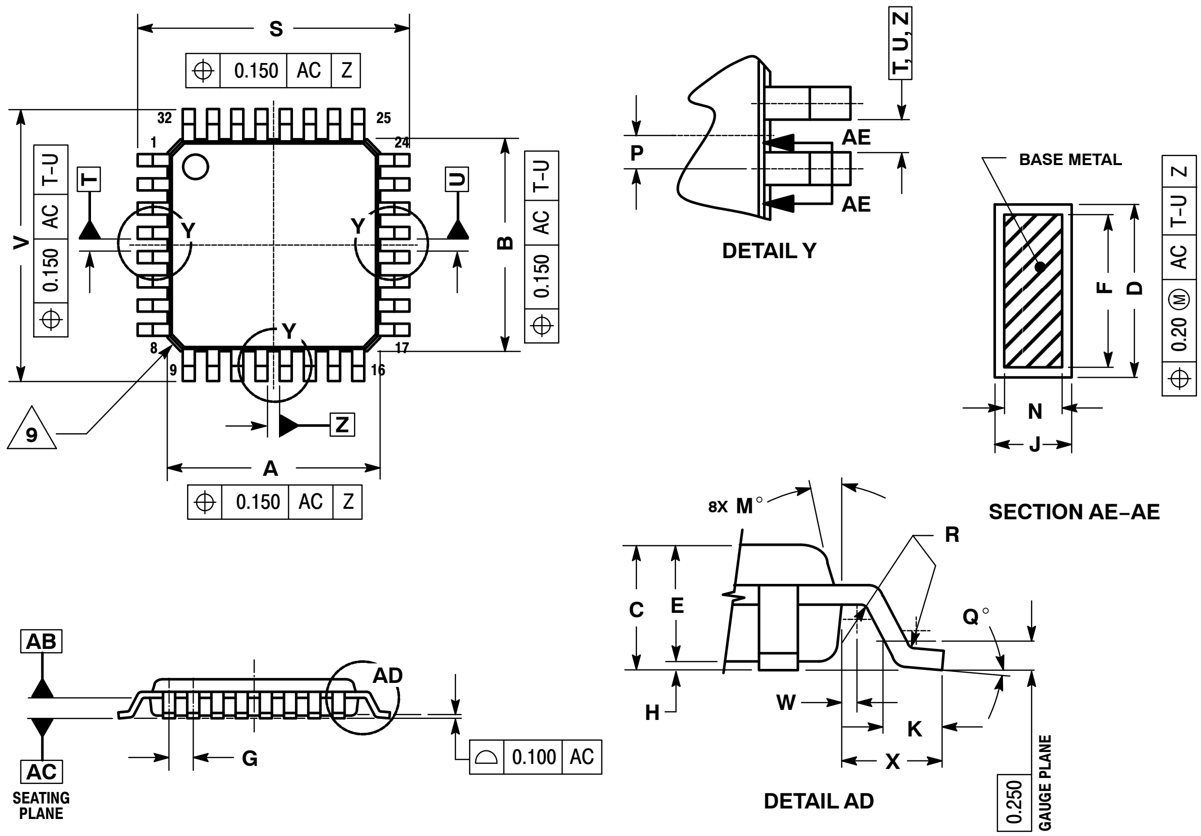
LQFP−32
CASE 873A−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

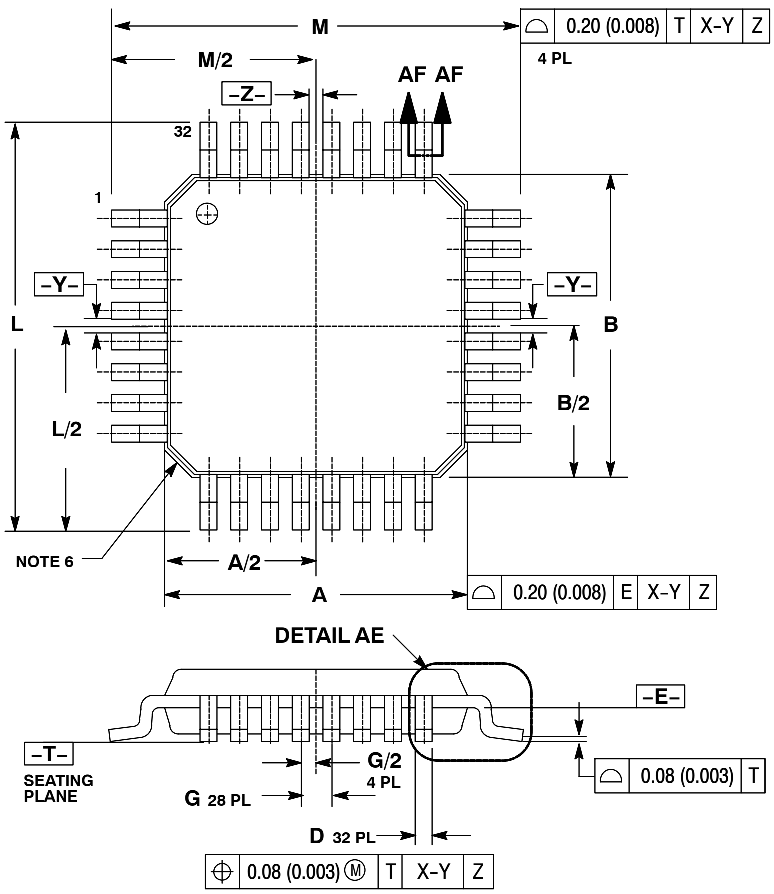
TQFP−32
CASE 873B−02
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U AND Z TO BE DETERMINED AT DATUM PLANE AB .
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.533.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

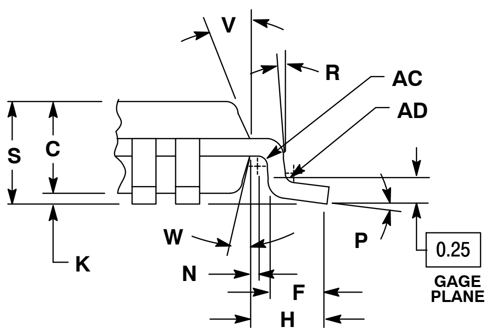
	MILLIMETERS	
DIM	MIN	MAX
A	6.950	7.050
B	6.950	7.050
C	1.000	1.200
D	0.300	0.450
E	0.950	1.050
F	0.300	0.400
G	0.800 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
M	12° REF	
N	0.090	0.178
P	0.400 BSC	
Q	0°	7°
R	0.150	0.250
S	8.950	9.050
V	8.950	9.050
W	0.200 REF	
X	1.000 REF	

TQFP−32
CASE 873F−01
ISSUE O

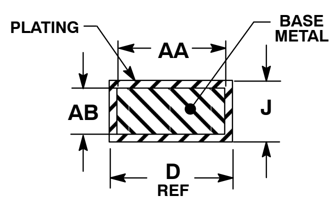


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MM.
3. DATUM “X”, “Y” AND “Z” TO BE DETERMINED AT DATUM PLANE DATUM “E”.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLAND “E”.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM D DIMENSION BY MORE THAN 0.08 (0.003). DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).
6. EXACT SHAPE CORNERS MAY VARY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.00 BSC		0.197 BSC	
B	5.00 BSC		0.197 BSC	
C	0.95	1.05	0.037	0.041
D	0.17	0.27	0.007	0.011
F	0.45	0.75	0.018	0.030
G	0.50 BSC		0.020 BSC	
H	1.00 REF		0.039 BSC	
J	0.09	0.20	0.004	0.008
K	0.05	0.15	0.002	0.006
L	7.00 BSC		0.276 BSC	
M	7.00 BSC		0.276 BSC	
N	0.20	---	0.008	---
P	0 °	7 °	0 °	7 °
R	0 °	---	0 °	---
S	---	1.20	---	0.047
V	11 °	13 °	11 °	13 °
W	11 °	13 °	11 °	13 °
AA	0.17	0.23	0.007	0.009
AB	0.09	0.16	0.004	0.006
AC	0.08	---	0.003	---
AD	0.08	0.20	0.003	0.008

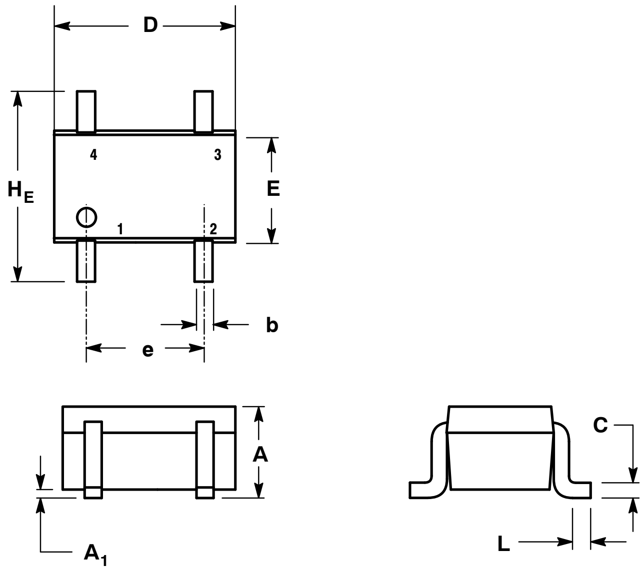


DETAIL AH



SECTION AF−AF

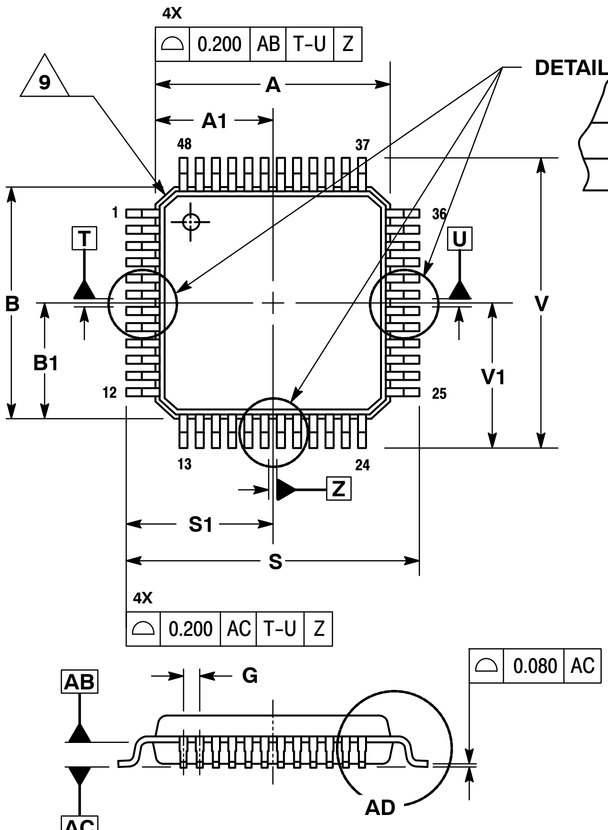
SC−82, 4 LEAD, GULL WING
CASE 900AA−01
ISSUE O

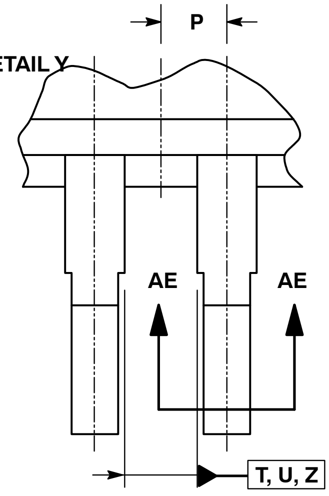


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUMTHICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

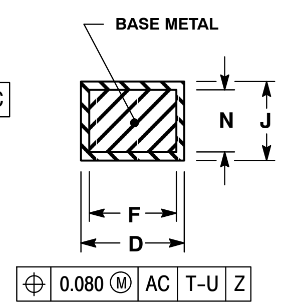
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.04
A_1	0	−−−	0.10	0	−−−	0.004
b	0.10	0.20	0.30	0.004	0.008	0.012
C	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.15	1.25	1.35	0.045	0.049	0.053
e	1.30 BSC			0.051 BSC		
H_E	2.00	2.10	2.20	0.079	0.083	0.087
L	0.10	0.20	0.30	0.004	0.008	0.012

TQFP−48
CASE 932−02
ISSUE E

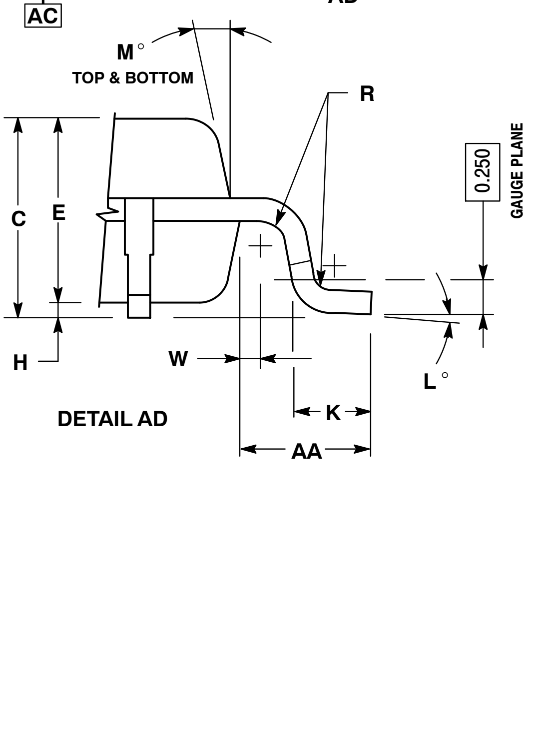




DETAIL Y



SECTION AE−AE



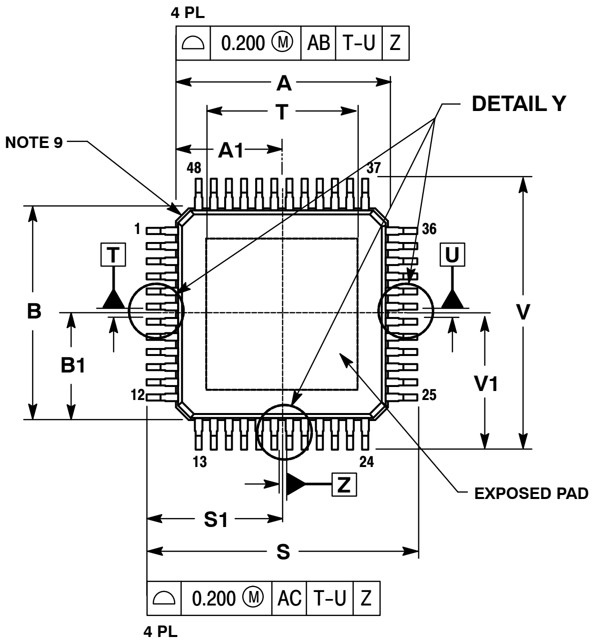
DETAIL AD

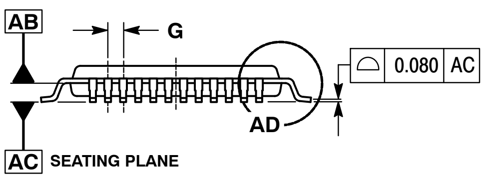
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

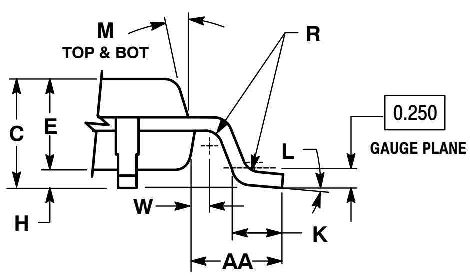
	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	1°	5°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

TQFP−48

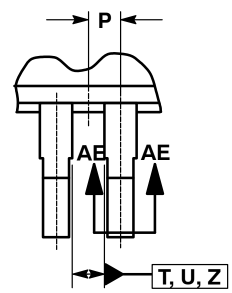
CASE 932F−01
ISSUE A



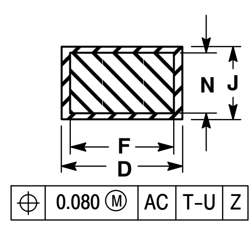




DETAIL AD



DETAIL Y

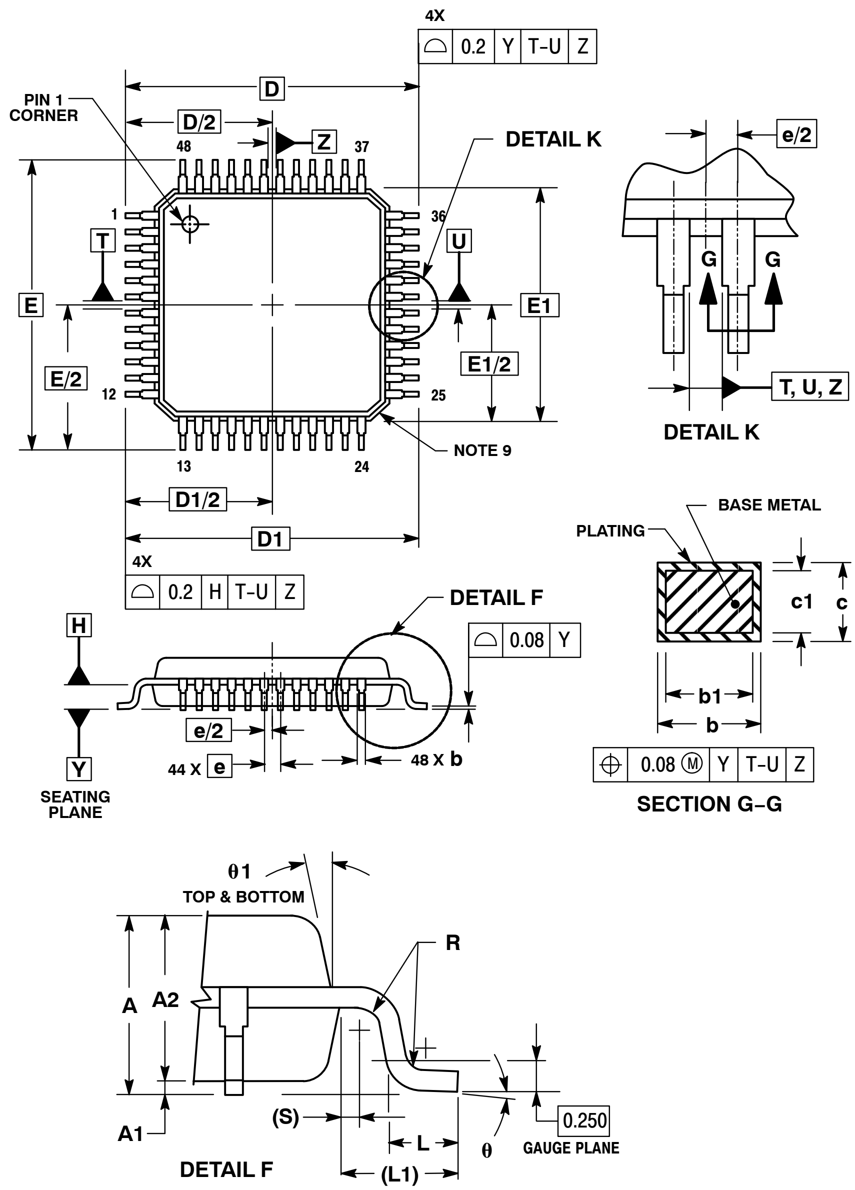


SECTION AE−AE

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND AB TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	0.900	1.100
D	0.170	0.270
E	0.950	1.250
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
T	5.000 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

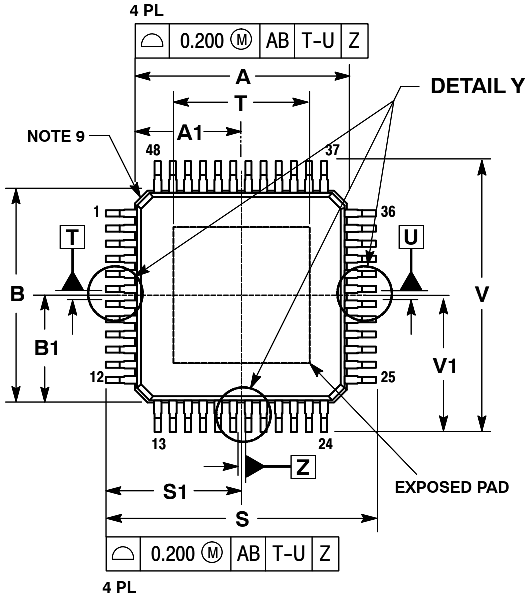
LQFP−48
CASE 932AA−01
ISSUE O

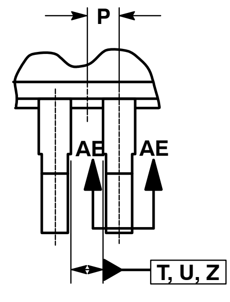


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE Y.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

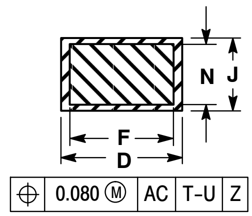
	MILLIMETERS	
DIM	MIN	MAX
A	1.4	1.6
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	9.0 BSC	
D1	7.0 BSC	
e	0.5 BSC	
E	9.0 BSC	
E1	7.0 BSC	
L	0.5	0.7
L1	1.0 REF	
R	0.15	0.25
S	0.2 REF	
θ	1°	5°
θ1	12 REF	

TQFP−48 EP 7x7, 0.5P
CASE 932AB−01
ISSUE O

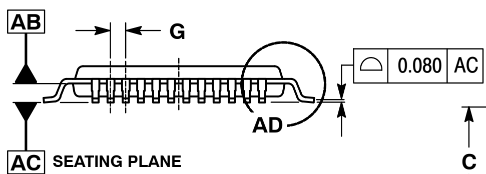


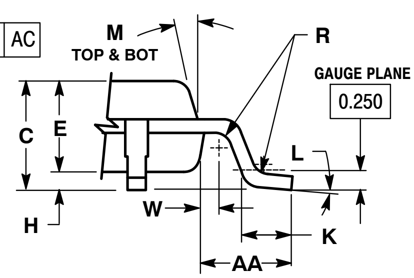


DETAIL Y



SECTION AE−AE



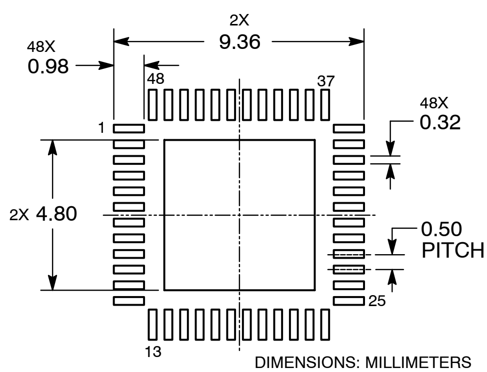


DETAIL AD

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S, S1, V, V1 AND AA TO BE DETERMINED AT DATUM PLANE AC.
6. DIMENSIONS A, A1, B, AND B1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A, A1, B, AND B1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

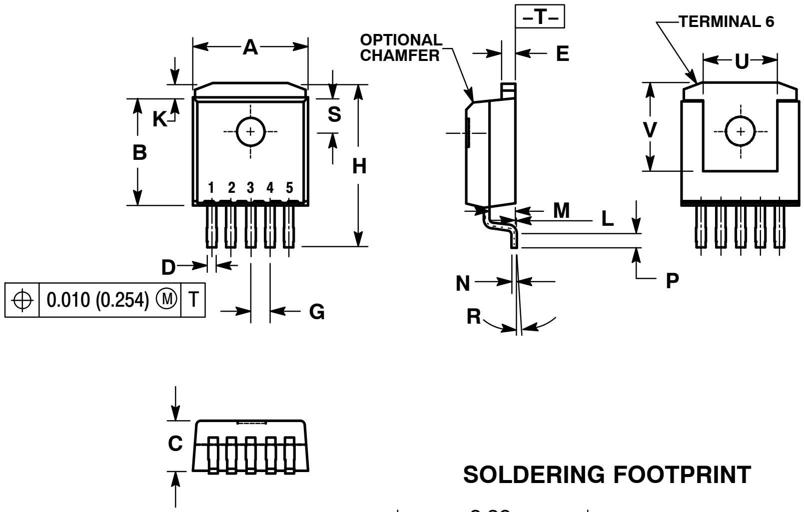
	MILLIMETERS	
DIM	MIN	MAX
A	7.00 BSC	
A1	3.50 BSC	
B	7.00 BSC	
B1	3.50 BSC	
C	----	1.20
D	0.17	0.27
E	0.95	1.05
F	0.17	0.23
G	0.50 BSC	
H	0.05	0.15
J	0.09	0.20
K	0.50	0.70
L	0°	7°
M	12° REF	
N	0.09	0.16
P	0.25 BSC	
R	0.15	0.25
S	9.00 BSC	
S1	4.50 BSC	
T	4.50 BSC	
V	9.00 BSC	
V1	4.50 BSC	
W	0.20 REF	
AA	1.00 REF	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

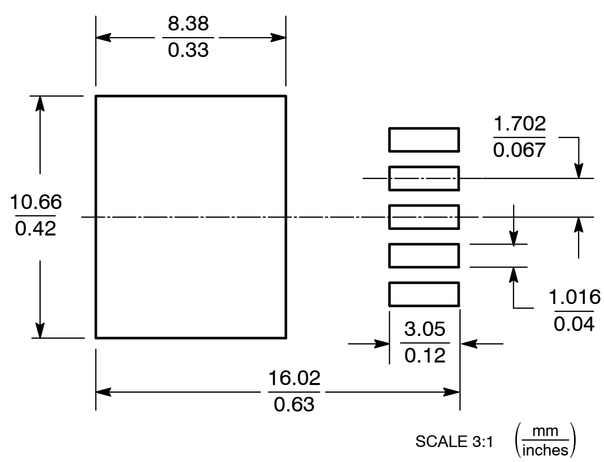
D²PAK 5−PIN
CASE 936A−02
ISSUE C



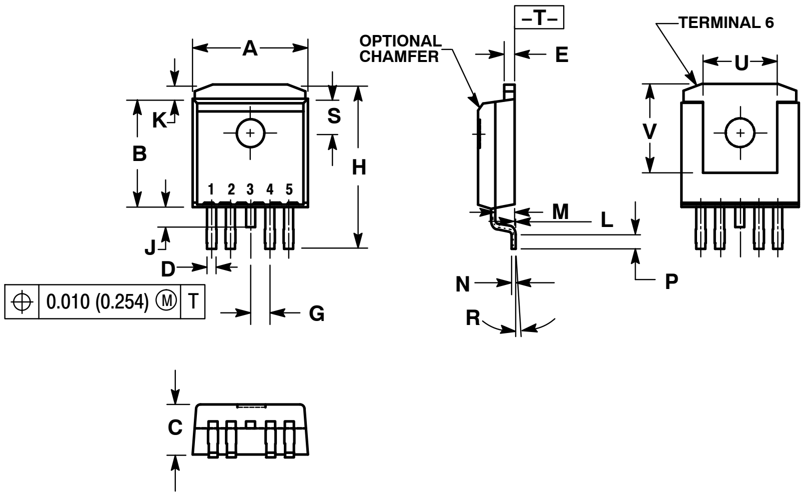
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT



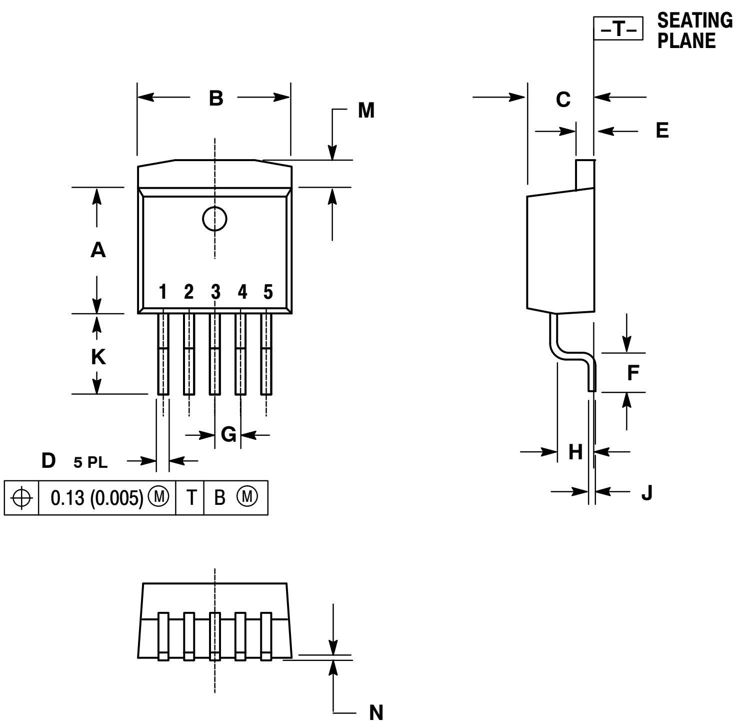
D2PAK 5−LEAD, CENTER CROPPED
CASE 936D−03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

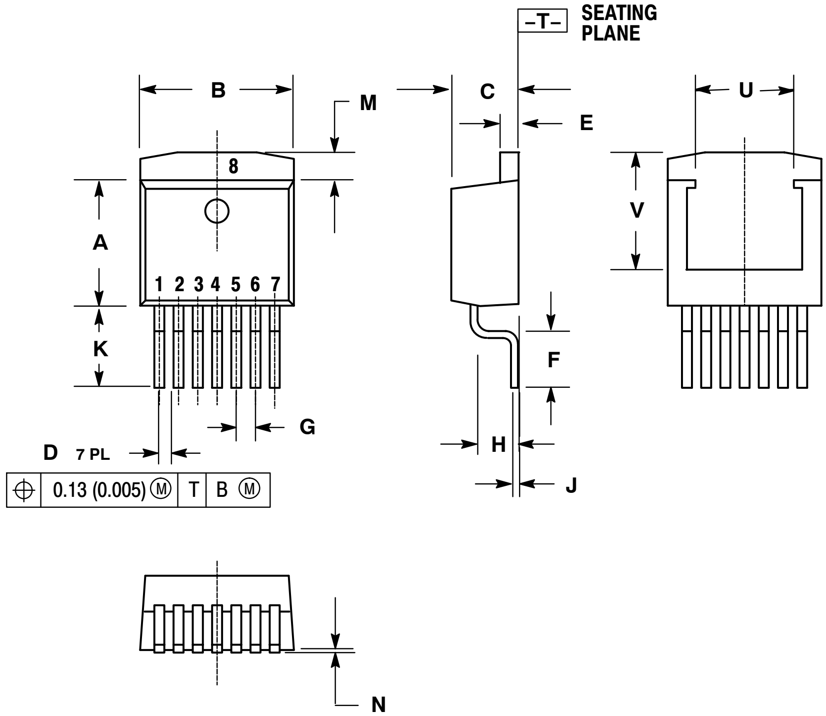
D2PAK 5−LEAD LONG LEAD
CASE 936F−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.035	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.067 BSC		1.70 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

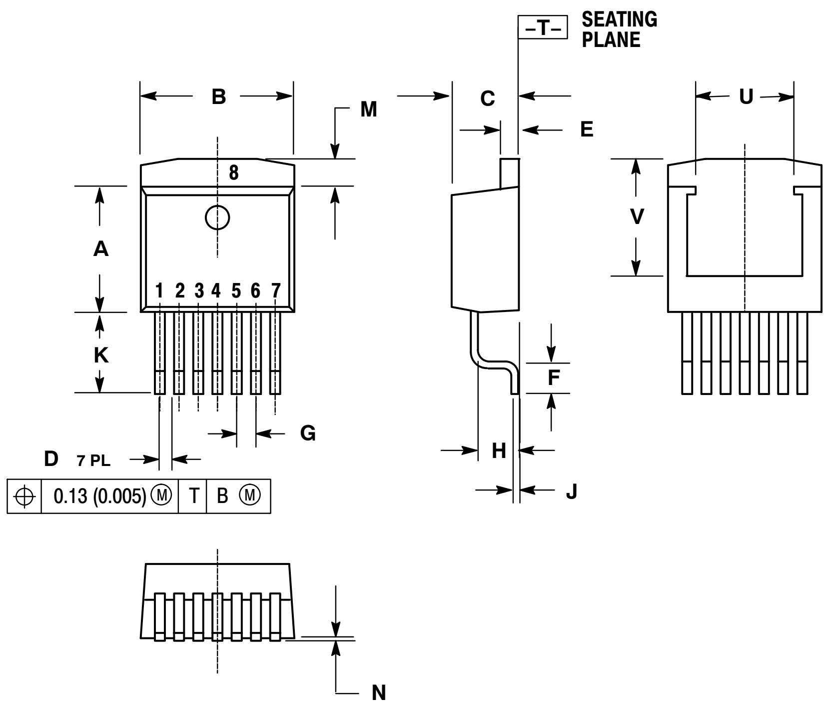
D2PAK 7−LEAD
CASE 936G−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.050 BSC		1.27 BSC	
H	0.100	0.110	2.54	2.79
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

D2PAK SHORT 7−LEAD
CASE 936H−01
ISSUE O

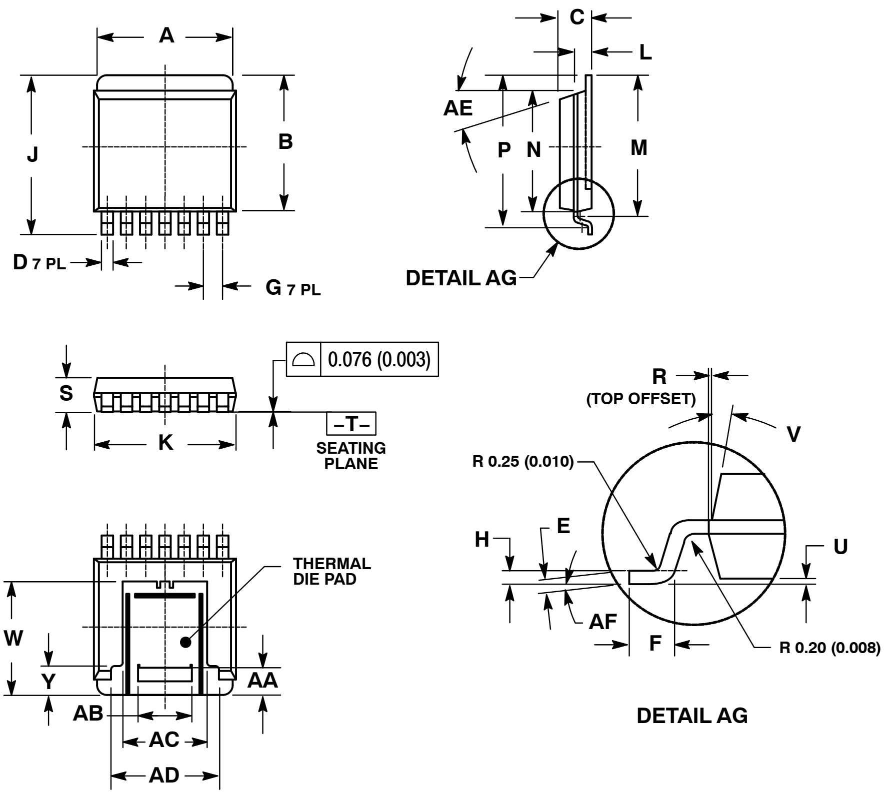


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.058	0.078	1.41	1.98
G	0.050 BSC		1.27 BSC	
H	0.100	0.110	2.54	2.79
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

POWERFLEX, 7−LEAD

CASE 936J−01
ISSUE O

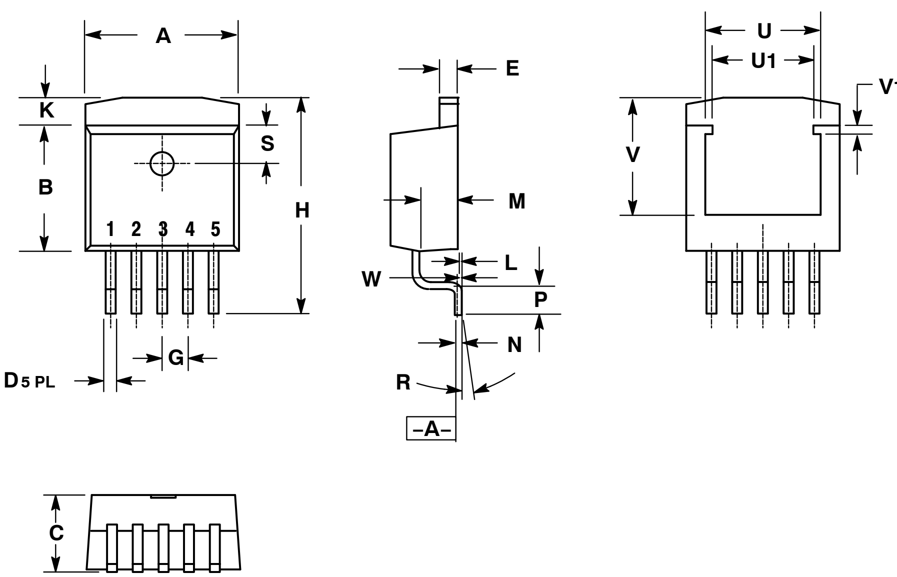


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.350	0.360	8.89	9.14
B	0.350	0.360	8.89	9.14
C	0.070	0.080	1.78	2.03
D	0.026	0.030	0.66	0.76
E	0.005	0.015	0.13	0.38
F	0.031	0.041	0.79	1.04
G	0.050 BSC		1.270 BSC	
H	0.008	0.012	0.199	0.301
J	0.410	0.420	10.41	10.67
K	0.365	00.375	9.27	9.53
L	0.040 REF		1.02 REF	
M	0.361	0.367	9.16	9.31
N	0.310	0.320	7.87	8.13
P	0.394	0.400	10.00	10.16
R	0.002	---	0.05	---
S	0.070	0.080	1.78	2.03
U	0.001	0.005	0.03	0.13
V	12 °		12 °	
W	0.296 REF		7.52 REF	
Y	0.075 REF		1.91 REF	
AA	0.071 REF		1.81 REF	
AB	0.140 REF		3.56 REF	
AC	0.220 REF		5.58 REF	
AD	0.281 REF		7.14 REF	
AE	12 °		12 °	
AF	3 °	6 °	3 °	6 °

D²PAK 5−LEAD

CASE 936AA−01
ISSUE B

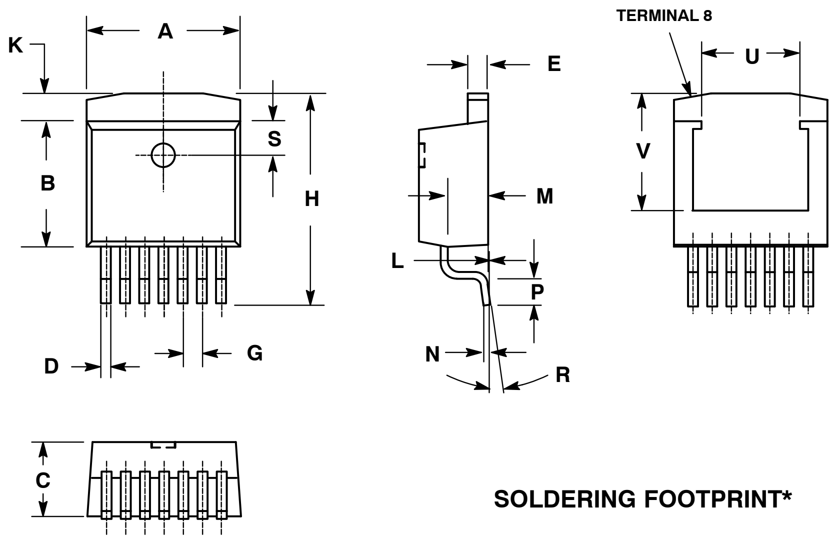


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
4. PACKAGE OUTLINE EXCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.396	0.406	10.05	10.31
B	0.330	0.340	8.38	8.64
C	0.170	0.180	4.31	4.57
D	0.026	0.035	0.66	0.91
E	0.045	0.055	1.14	1.40
G	0.067 BSC		1.70 BSC	
H	0.539	0.579	13.69	14.71
K	0.055	0.066	1.40	1.68
L	0.000	0.010	0.00	0.25
M	0.098	0.108	2.49	2.74
N	0.017	0.023	0.43	0.58
P	0.058	0.078	1.47	1.98
R	0 °	8 °	0 °	8 °
S	0.095	0.105	2.41	2.67
U	0.296	0.304	7.52	7.72
U1	0.265	0.272	6.72	6.92
V	0.296	0.300	7.53	7.63
V1	0.040	0.044	1.01	1.11
W	0.010		0.25	

D^2PAK 7−LEAD (SHORT LEAD)

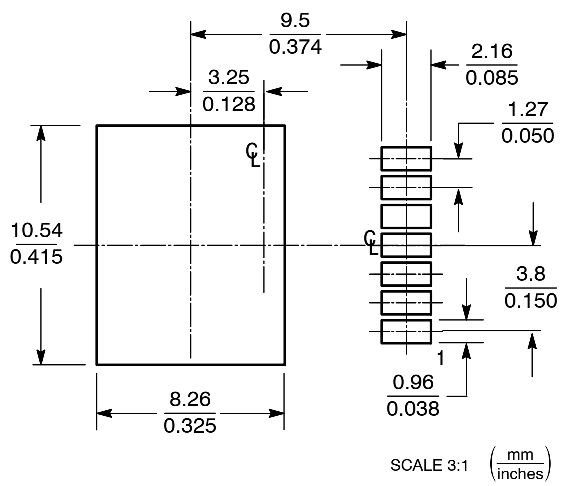
CASE 936AB−01
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

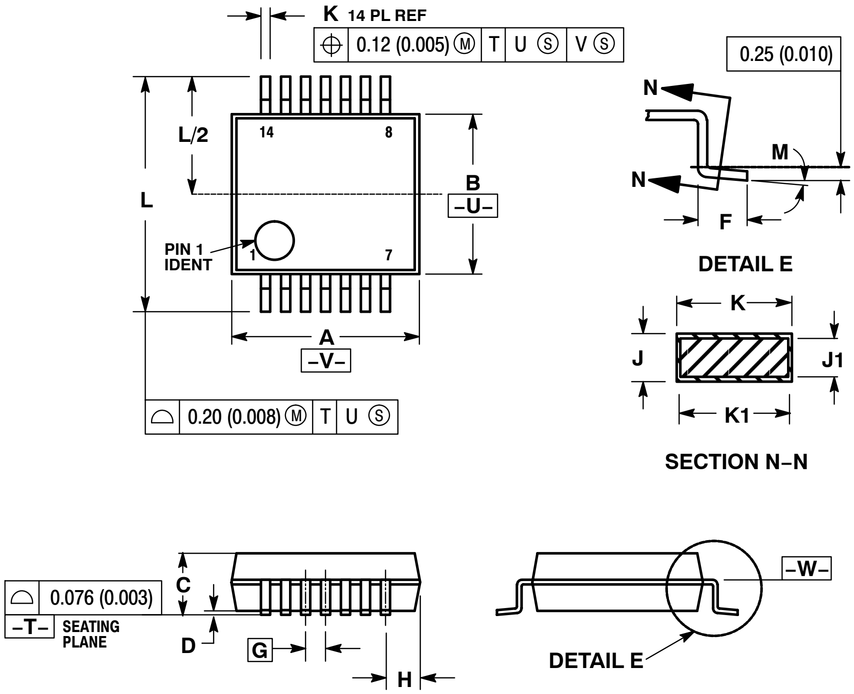
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.396	0.406	10.05	10.31
B	0.326	0.336	8.28	8.53
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
G	0.050 REF		1.27 REF	
H	0.539	0.579	13.69	14.71
K	0.055	0.066	1.40	1.68
L	0.000	0.010	0.00	0.25
M	0.100	0.110	2.54	2.79
N	0.017	0.023	0.43	0.58
P	0.058	0.078	1.47	1.98
R	0 °	8 °	0 °	8 °
S	0.095	0.105	2.41	2.67
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

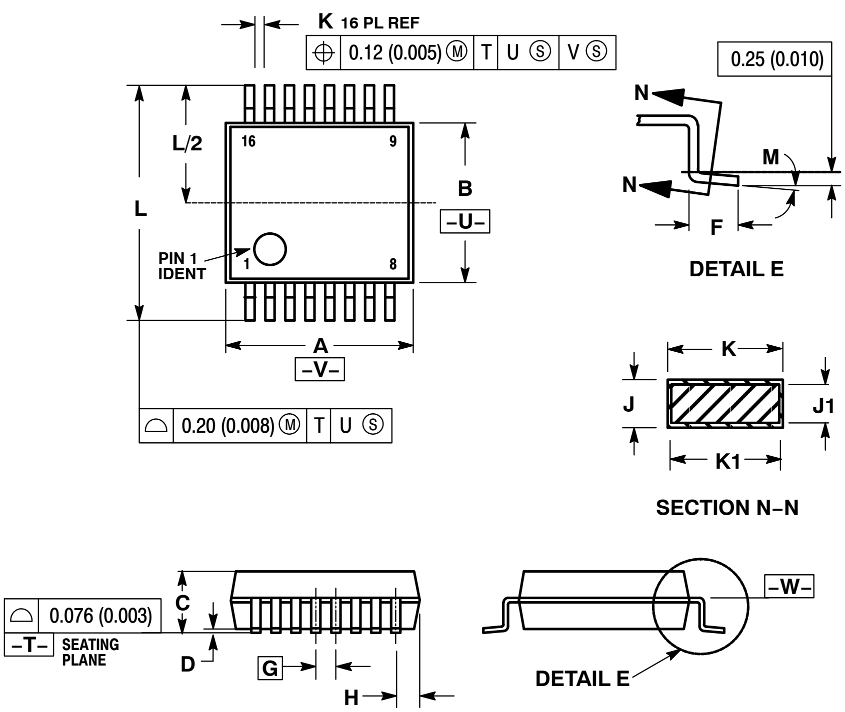
14−LEAD SSOP
CASE 940A−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	1.08	1.22	0.042	0.048
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.38	0.010	0.015
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

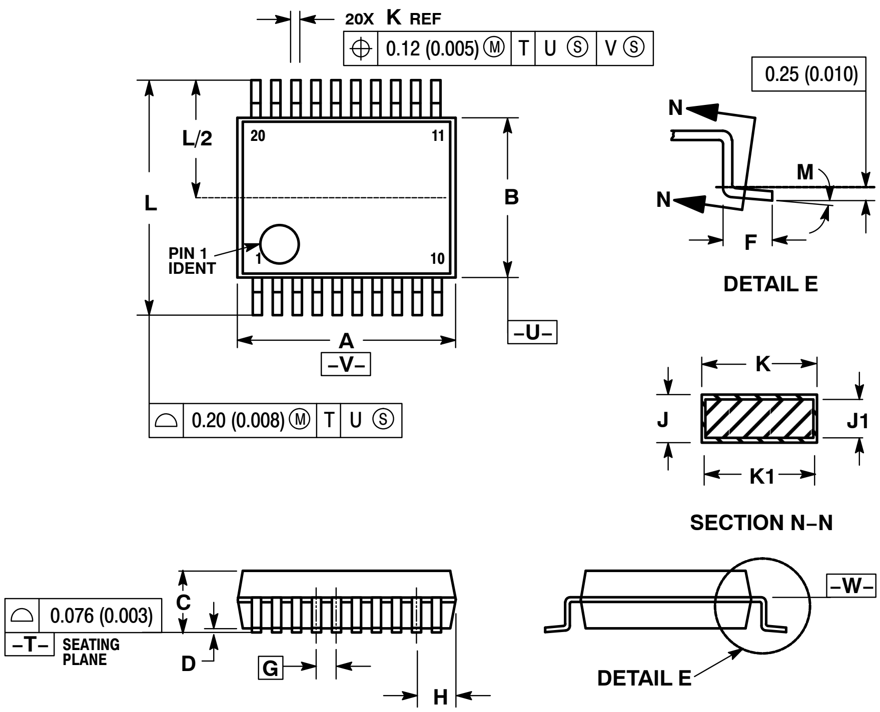
16−LEAD SSOP
CASE 940B−03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

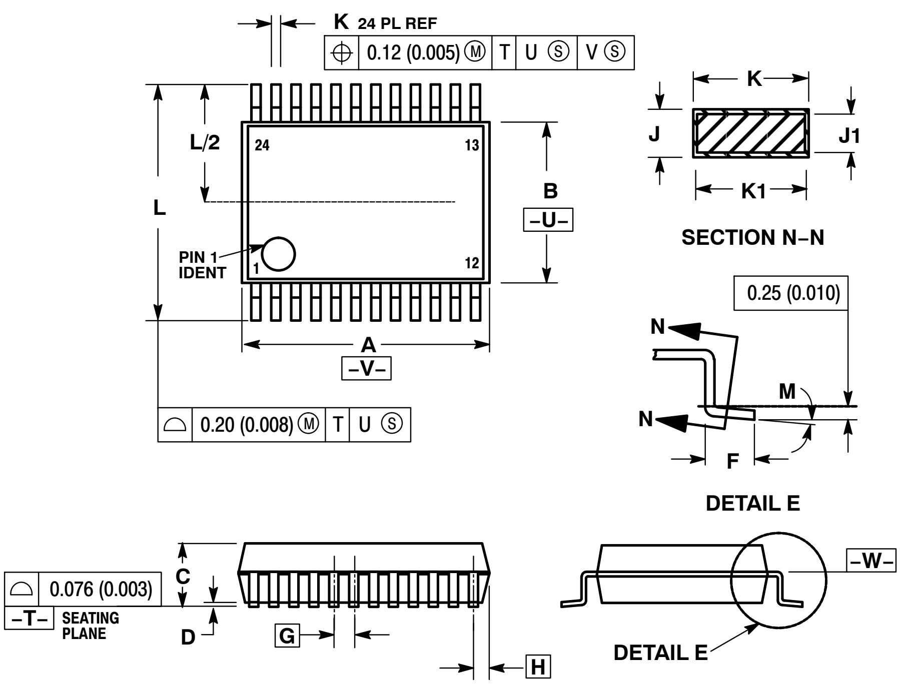
20–LEAD SSOP
CASE 940C–03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

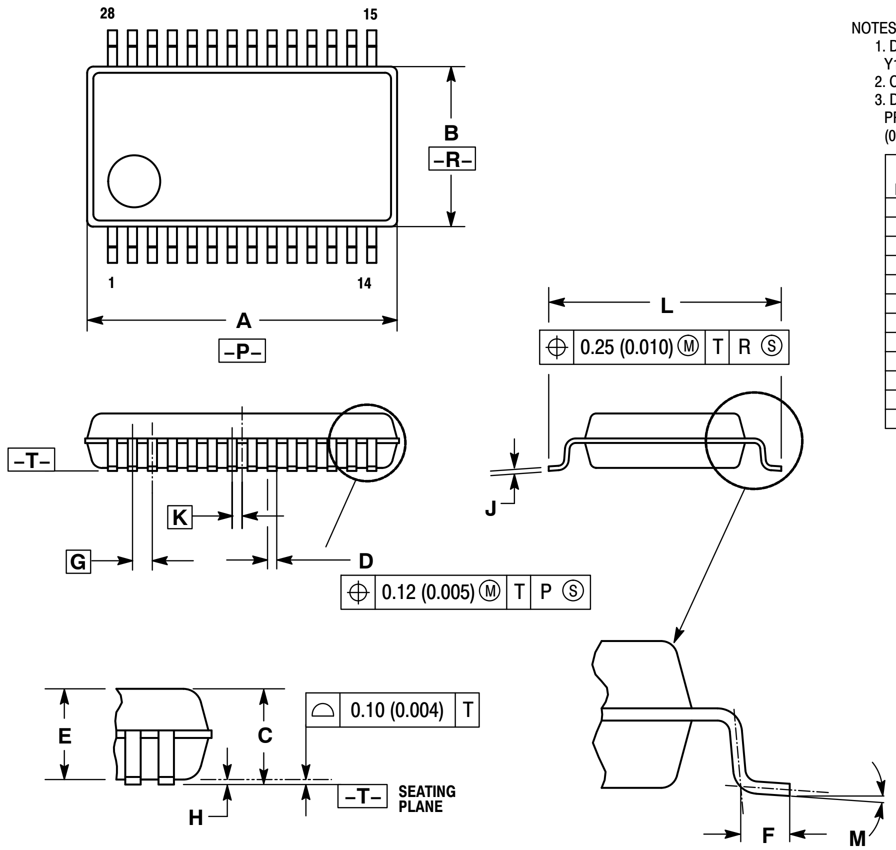
24–LEAD SSOP
CASE 940D–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0 °	8 °	0 °	8 °

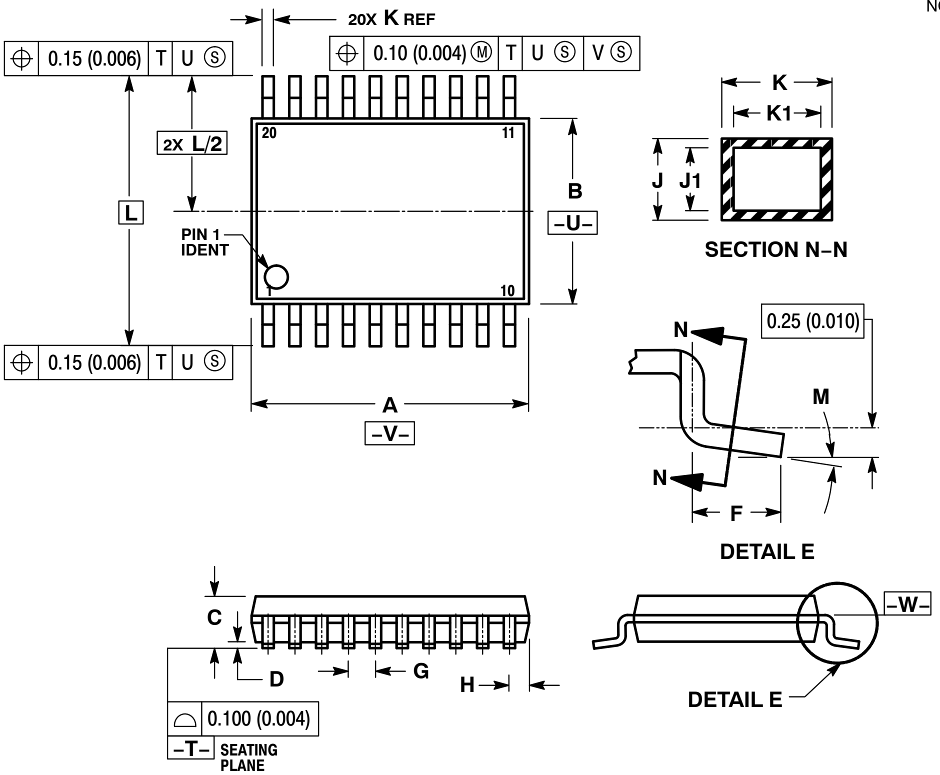
28−LEAD SSOP
CASE 940J−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION IS 0.15 (0.006) MAX PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.10	10.20	0.398	0.402
B	5.20	5.30	0.205	0.209
C	---	2.00	---	0.079
D	0.20	0.40	0.008	0.016
E	1.75	1.85	0.069	0.073
F	0.45	0.75	0.018	0.030
G	0.65 BSC		0.0256 BSC	
H	0.00	0.15	0.000	0.006
J	0.10	0.20	0.004	0.008
K	0.325 BSC		0.0128 BSC	
L	7.50	7.90	0.295	0.311
M	1°	7°	1°	7°

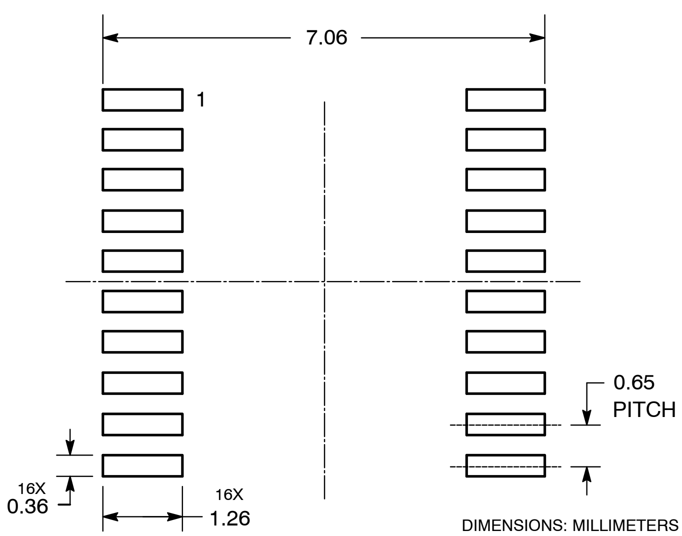
TSSOP−20
CASE 948E−02
ISSUE C



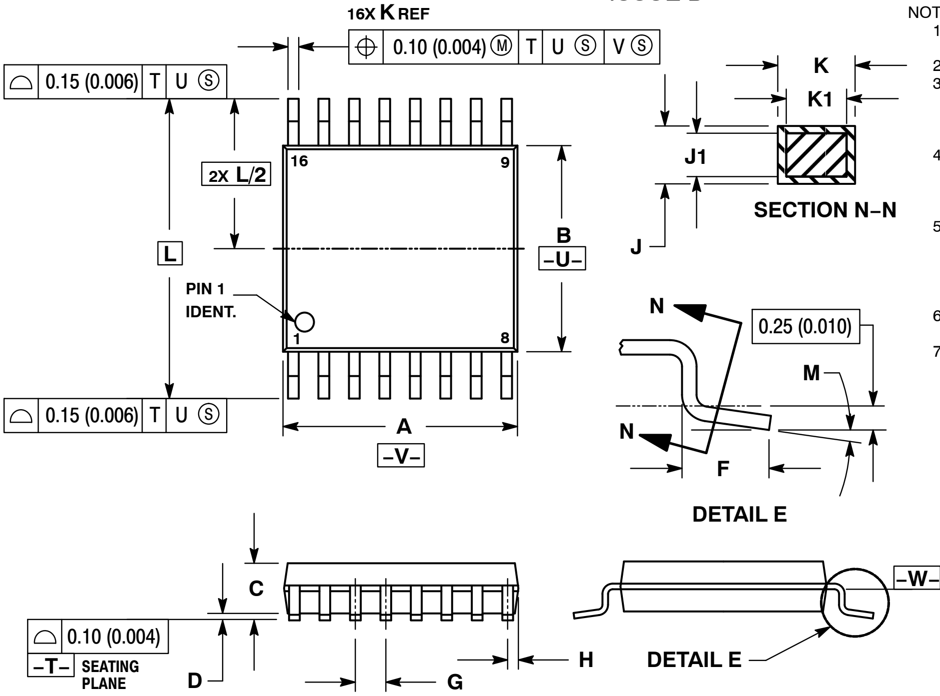
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



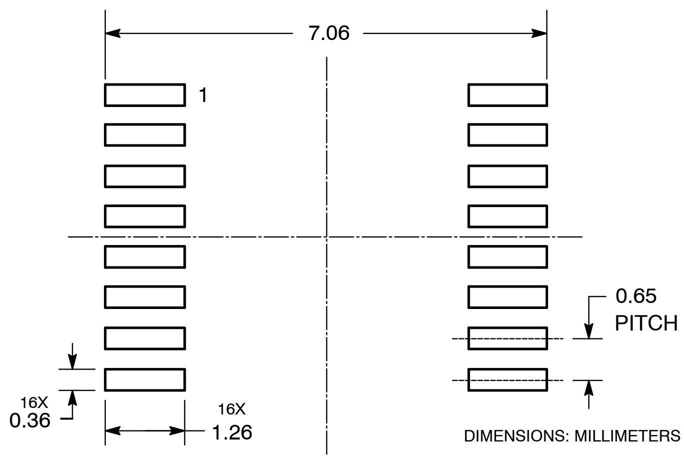
TSSOP−16
CASE 948F−01
ISSUE B



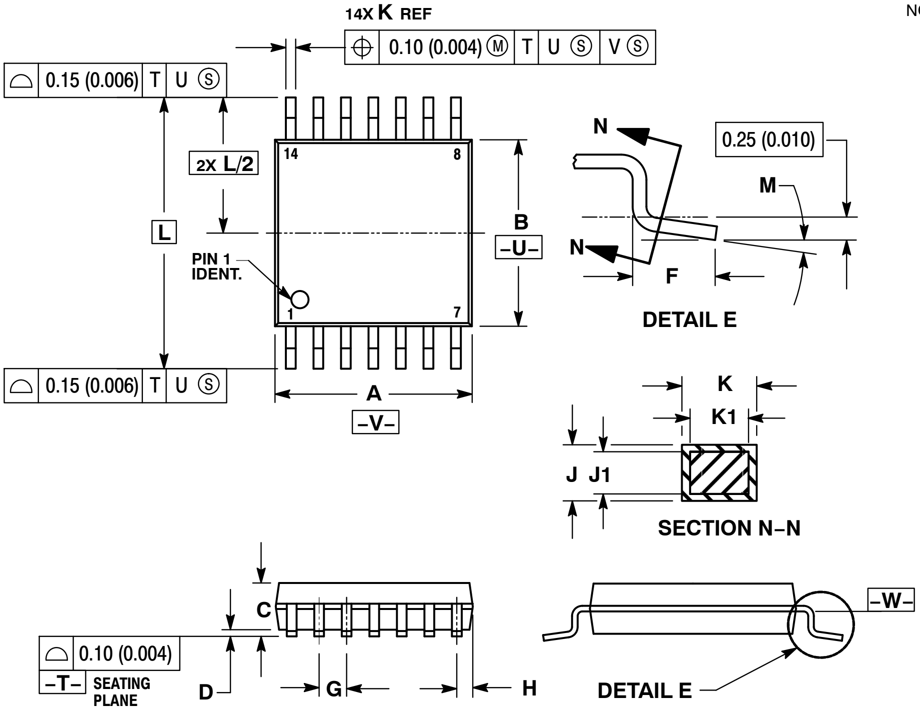
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



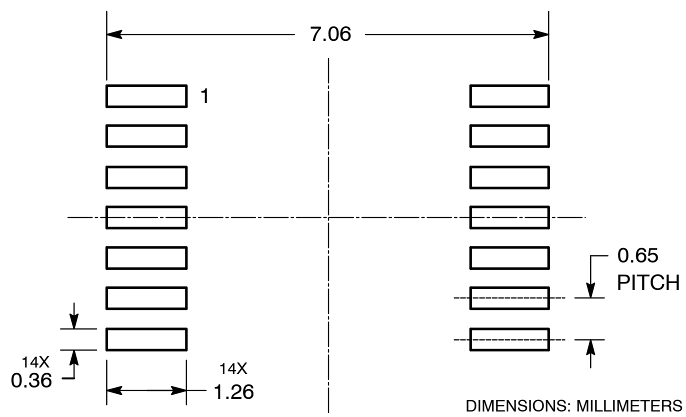
TSSOP−14
CASE 948G−01
ISSUE B



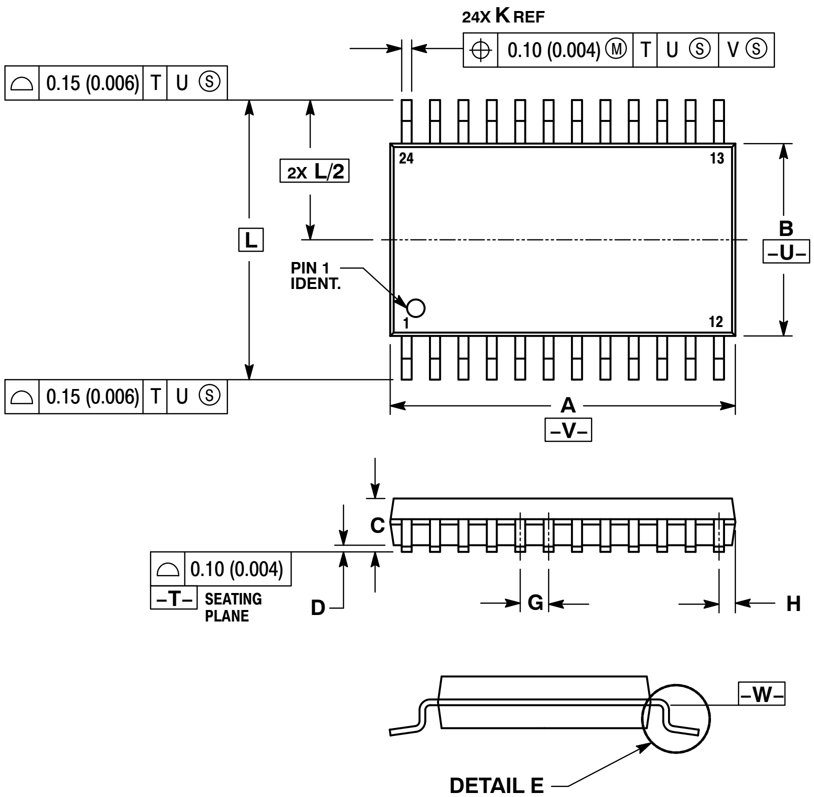
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

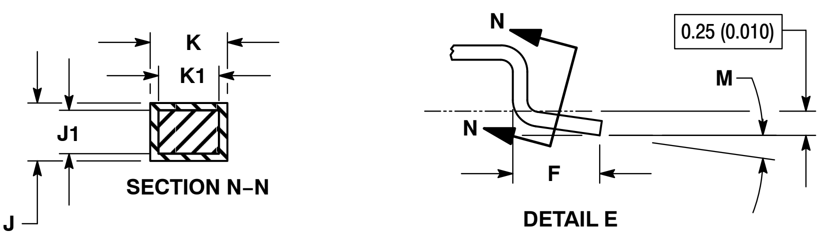
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



TSSOP−24
CASE 948H−01
ISSUE A

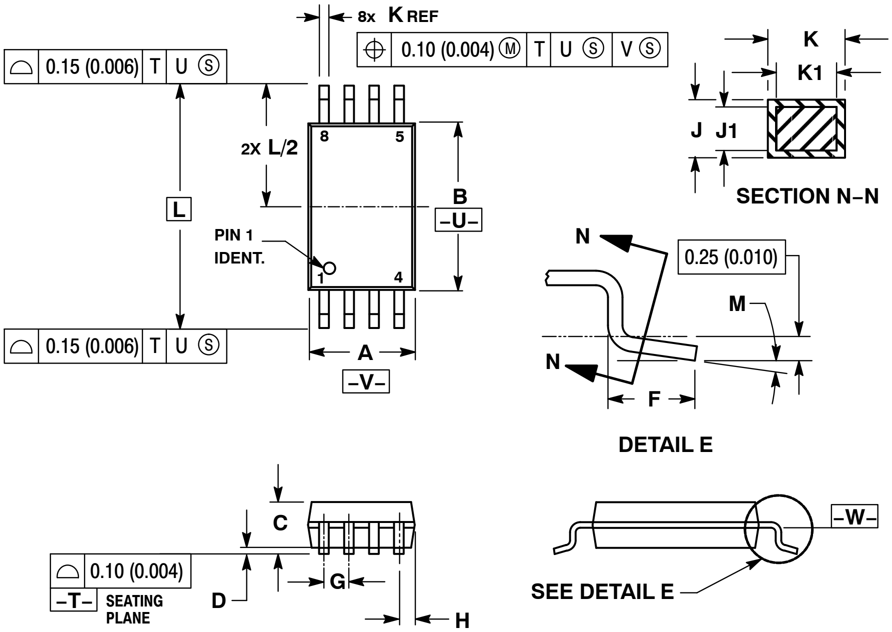




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

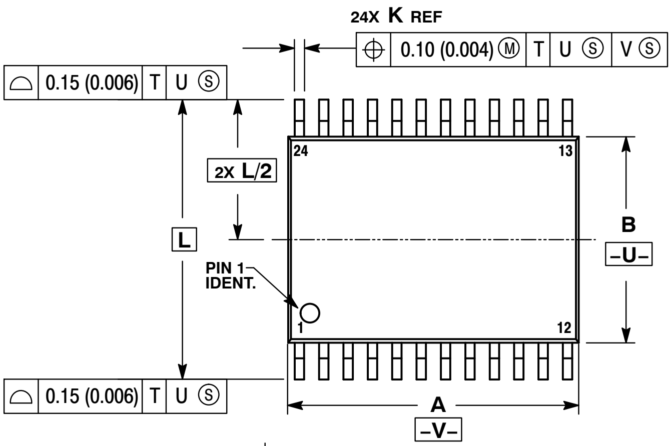
TSSOP−8
CASE 948J−01
ISSUE A

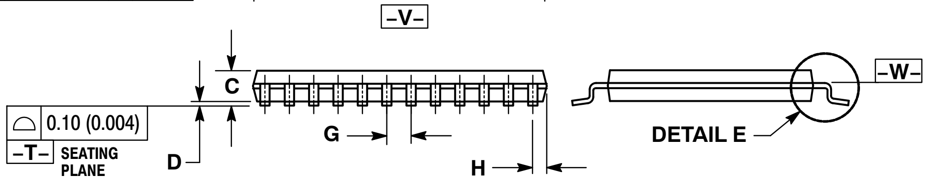


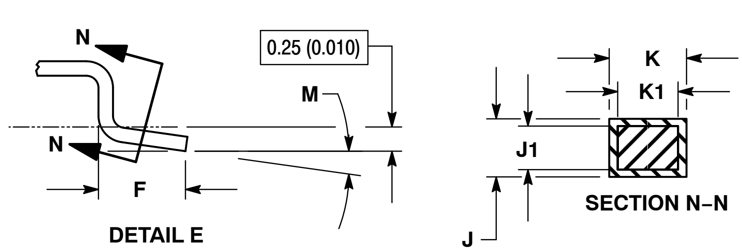
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

TSSOP−24 WIDE BODY
CASE 948K−01
ISSUE O



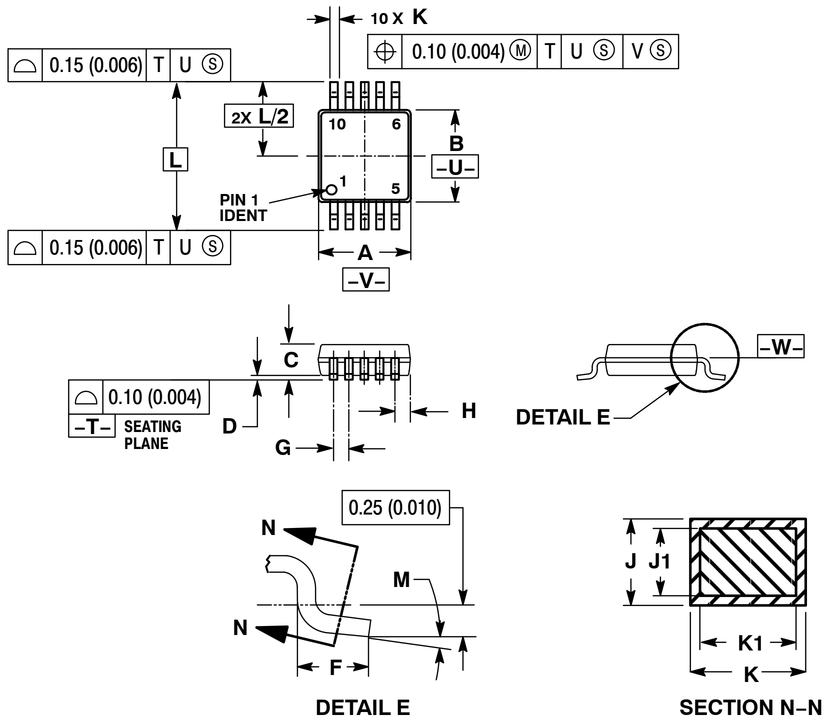




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14 .5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	5.50	5.70	0.216	0.224
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	7.60 BSC		0.299 BSC	
M	0°	8°	0°	8°

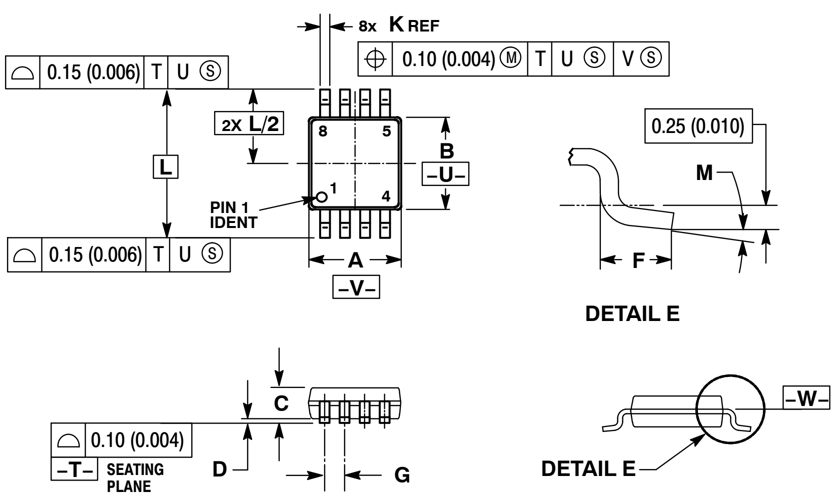
TSSOP−10
CASE 948P−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.50 BSC		0.020 BSC	
H	0.45	0.55	0.018	0.022
J	0.13	0.23	0.005	0.009
J1	0.13	0.18	0.005	0.007
K	0.15	0.30	0.006	0.012
K1	0.15	0.25	0.006	0.010
L	4.90 BSC		0.193 BSC	
M	0°	5°	0°	5°

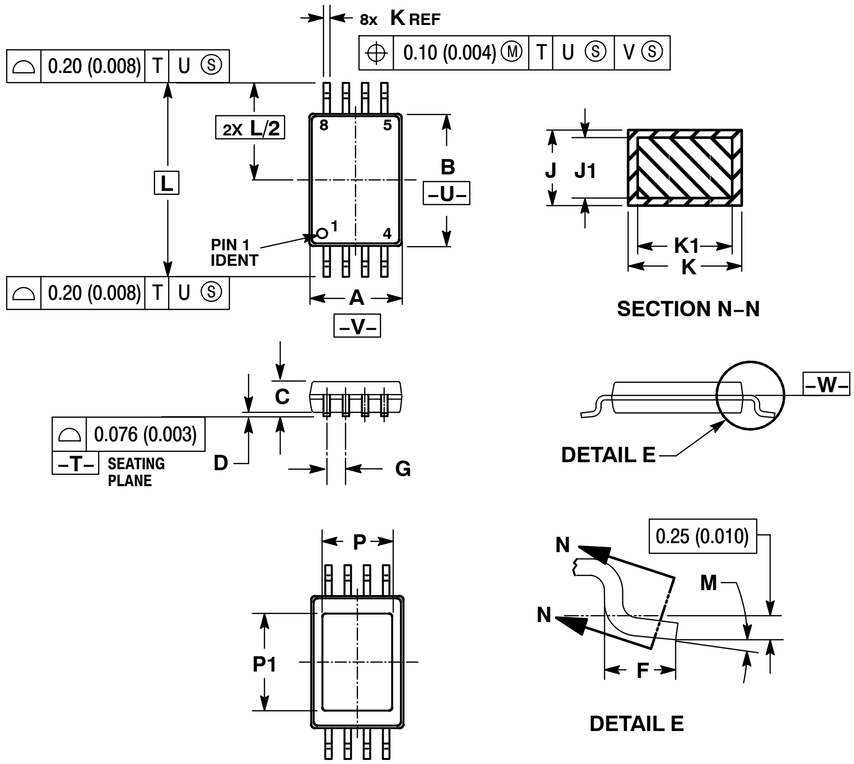
TSSOP−8
Micro8
CASE 948R−02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

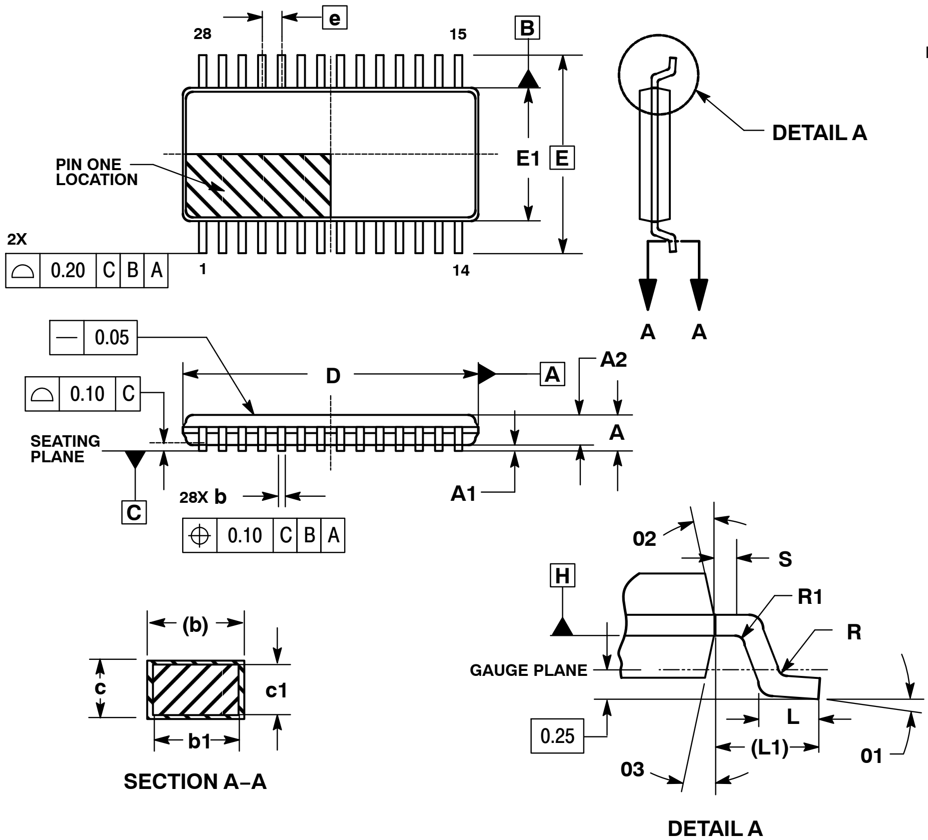
TSSOP−8
CASE 948S−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°
P	---	2.20	---	0.087
P1	---	3.20	---	0.126

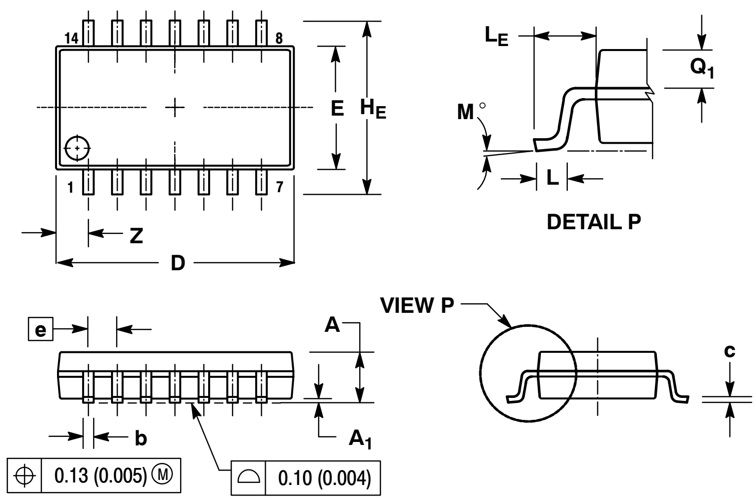
TSSOP−24
CASE 948AA−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	9.60	9.80
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.45	0.75
L1	1.00 REF	
R	0.09	−−−
R1	0.09	−−−
S	0.20	−−−
01	0 °	8 °
02	12 ° REF	
03	12 ° REF	

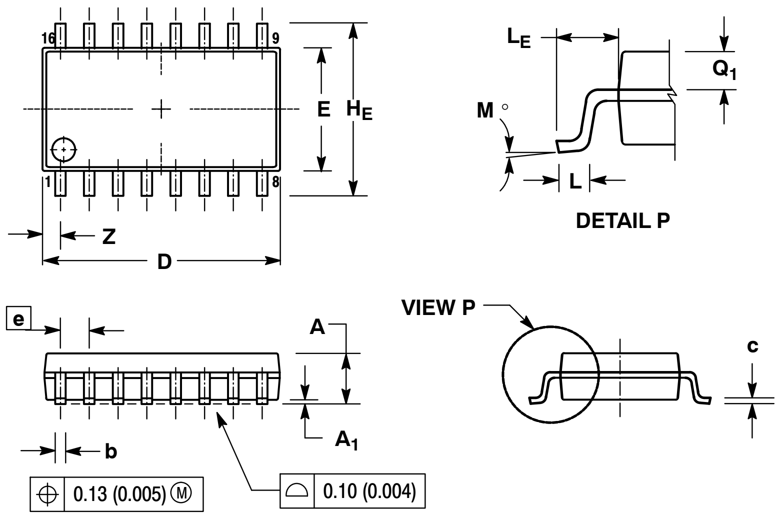
EIAJ−14
CASE 965−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

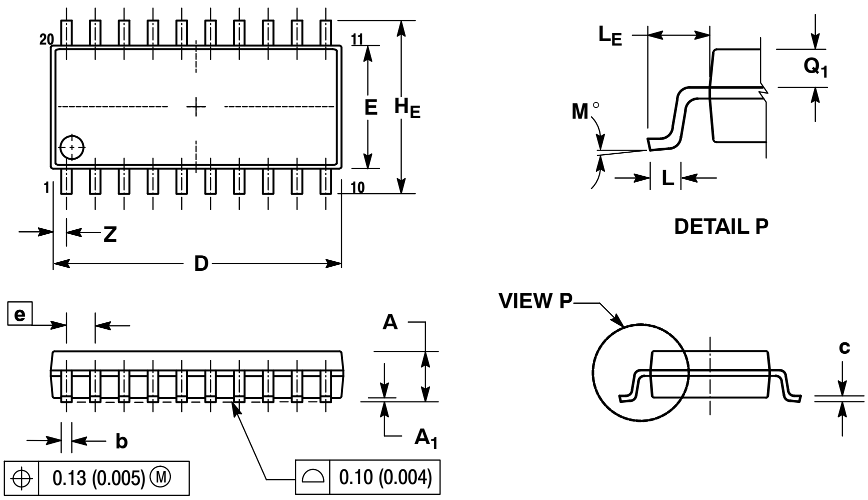
EIAJ−16
CASE 966−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

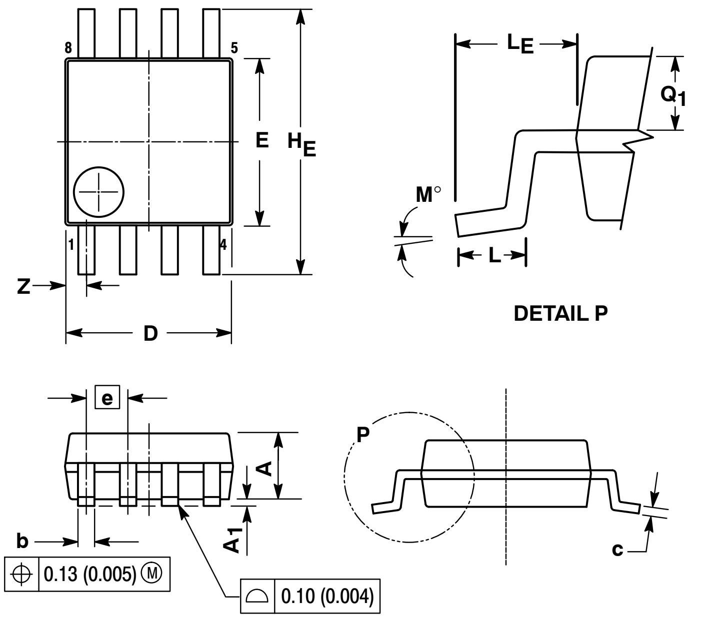
EIAJ−20
CASE 967−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

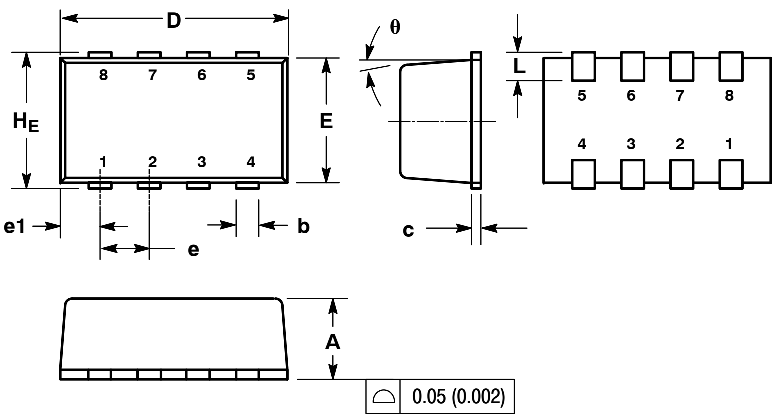
SOEIAJ−8
CASE 968−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSION D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	5.10	5.50	0.201	0.217
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	---	0.94	---	0.037

ChipFET LEADLESS
CASE 1206A−03
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e		0.65 BSC			0.025 BSC	
e1		0.55 BSC			0.022 BSC	
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ		5° NOM			5° NOM	

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

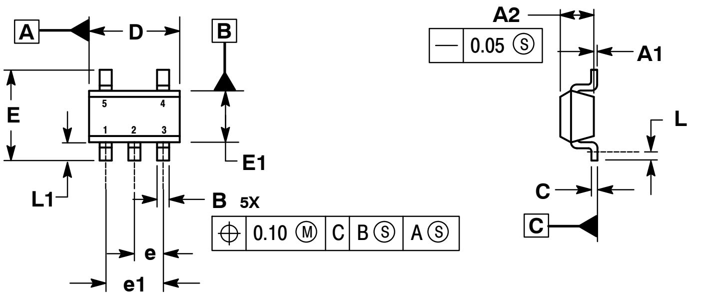
STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINTS*

(Please see official case outline for soldering footprint options)

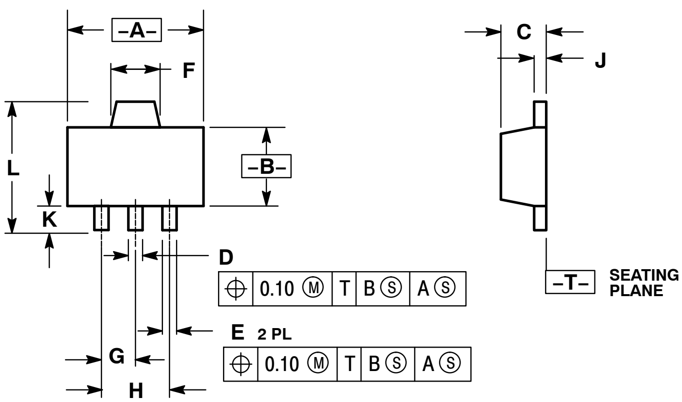
SOT23−5
CASE 1212−01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	---
L1	0.45	0.75

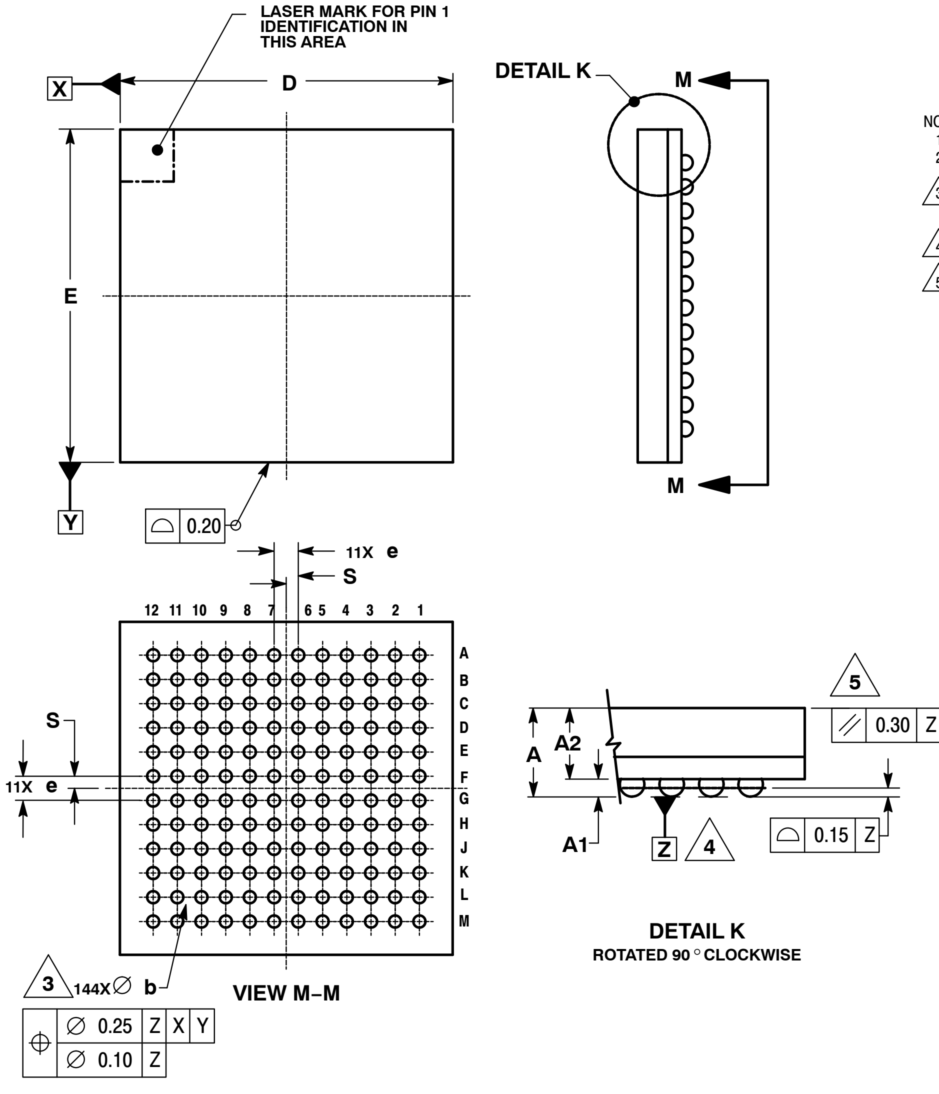
SOT−89
CASE 1213−02
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 1213−01 OBSOLETE, NEW STANDARD 1213−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.40	4.60	0.173	0.181
B	2.40	2.60	0.094	0.102
C	1.40	1.60	0.055	0.063
D	0.37	0.57	0.015	0.022
E	0.32	0.52	0.013	0.020
F	1.50	1.83	0.059	0.072
G	1.50 BSC		0.059 BSC	
H	3.00 BSC		0.118 BSC	
J	0.30	0.50	0.012	0.020
K	0.80	---	0.031	---
L	---	4.25	---	0.167

144−BGA
CASE 1242−01
ISSUE O



VIEW M−M

DETAIL K
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.60
A1	0.20	0.34
A2	1.16 REF	
b	0.30	0.50
D	11.00 BSC	
E	11.00 BSC	
e	0.80 BSC	
S	0.40 BSC	

Section 3

Thermal Considerations

Basic Semiconductor Thermal Measurement

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INTRODUCTION

This paper will provide the reader with a basic understanding of power semiconductor thermal parameters, how they are measured, and how they are used. With this knowledge, the reader will be able to better describe power semiconductors and answer many common questions relating to their power handling capability.

This paper will cover the following key topics.

- Understanding basic semiconductor thermal parameters
- Semiconductor thermal test equipment
- Thermal parameter test procedures
- Using thermal parameters to solve often asked thermal questions

Understanding Basic Semiconductor Thermal Parameters

Heat flows from a higher to a lower temperature region. The quantity that resists or impedes this flow of heat energy is called thermal resistance or thermal impedance.

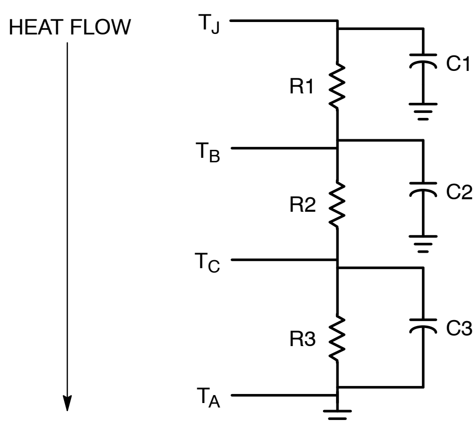
When the quantity of heat being generated by a device is equal to the quantity of heat being removed from it, a steady state condition is achieved.

To describe the thermal capability of a device, several key parameters and terms are used. They describe the steady state thermal capability of a power semiconductor device.

Key Parameters, Terms, and Definitions

T_J = *junction* temperature
T_C = *case* temperature
T_A = *ambient* temperature
TSP = **T**emperature **S**ensitive **P**arameter
T_R = *reference* temperature (i.e., *case* or *ambient*)
R_{thjr} = junction−to−*reference* thermal resistance
R_{thjc} = junction−to−*case* thermal resistance
R_{thja} = junction−to−*ambient* thermal resistance
$R_{thjr(t)}$ = junction−to−*reference* transient thermal resistance
P_D = power dissipation

The thermal behavior of a device can be described, for practical purposes, by an electrical equivalent circuit. This circuit consists of a resistor−capacitor network as shown.



Heat generated in a device's junction flows from a higher temperature region through each resistor−capacitor pair to a lower temperature region.

Figure 1. Thermal Electrical Equivalent Circuit

Resistors R1, R2, and R3 are all analogous to individual thermal resistance, or quantities that impede heat flow. Resistor R1 is the thermal resistance from the device's junction to its die−bond. Resistor R2 is the thermal resistance from the die−bond to the device's case. Resistor R3 is the thermal resistance from the device's case to ambient. The thermal resistance from the junction to some reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance R_{thjc} from junction−to−case is equal to the sum of resistors R1 and R2. The thermal resistance R_{thja} from junction−to−ambient, therefore, is equal to the sum of resistors R1, R2 and R3.

The capacitors shown help model the transient thermal response of the circuit. When heat is instantaneously applied and or generated, there is a charging effect that takes place. This response follows an RC time constant determined by the resistor−capacitor thermal network. Thermal resistance, at a given time, is called transient thermal resistance, $R_{thjr(t)}$.

To further understand transient thermal response, refer to ON Semiconductor Application Note AN569, "Transient Thermal Resistance − General Data And Its Use." [4] A detailed discussion of this will not be included here.

Using the key parameters and terms shown earlier, only a few equations are necessary to solve often asked thermal questions.

$$R_{thjr} = (T_J - T_R) / \text{power} \quad (1)$$

$$P_D = (\text{max. device temp.} - T_R) / R_{thjr} \quad (2)$$

$$T_J = P_D * R_{thjr} + T_R \quad (3)$$

Semiconductor Thermal Test Equipment

The procedure used determines the test equipment needed for measurement. Below you will find the equipment used for both a manual and an automated approach to thermal measurement.

Manual Technique:

Power supply	*(supplies power to the device under test)*
Thermocouple	*(measures T_R)*
Multimeter	*(measures current and voltage)*
Heat exchanger	*(needed to mount device to and remove heat)*
Chiller	*(needed to remove heat from device)*
Test fixture	*(provides power and sampling pulse train)*

Automated Systems Available:

Analysis Tech	*(Phase 6, 7, 8, and 9)*
Sage	*(Star 150)*
TESEC	*(DV240)*

The automated systems shown above each provide different levels of automation. Analysis Tech has the most complete automation and TESEC the least. One nice feature of the Analysis Tech system is that it will output the 3 resistor−capacitor values for the electrical equivalent circuit.

These values are very useful for modeling the thermal effects in computer simulation software such as SPICE. The level of automation you need depends both on your thermal measurement goals and available budget.

The main advantages of an automated approach are;

- Ease of use
- Less operator dependence on measurement
- Consistency
- Accuracy
- System network capability for data transfer

Thermal Parameter Test Procedure

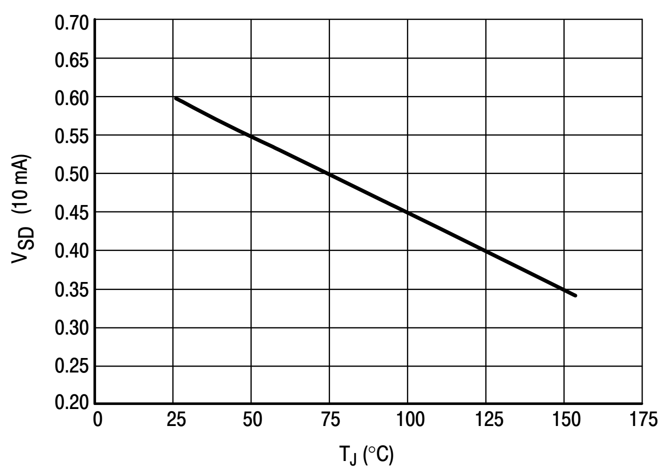
The basic procedure for measuring thermal parameters is as follows.

1. Calibrate the TSP (Temperature Sensitive Parameter).
2. Apply continuous power and TSP sampling pulses.
3. Measure T_J, T_R, and applied test power.
4. Calculate thermal resistance, $R_{thj(r)}$, and Maximum Power, P_D.

1. Calibrating the TSP, Temperature Sensitive Parameter

Since it is basically impossible to put a physical thermometer onto a device's junction to measure its temperature while under power, we must find another approach. Fortunately, we can use the device's forward junction voltage to tell us its temperature. The forward voltage drop of a diode's pn junction has a very linear relationship with temperature. We can use this relationship to tell us what the junction temperature is under any power condition.

To determine the actual voltage temperature relationship of a TSP for a given device, simply calibrate the TSP at a constant sense current over temperature as shown in Figure 2. The TSP sense current used should be small so as to not cause additional heating during calibration.



The forward voltage drop of a MOSFET body diode decreases linearly over temperature at rate of about 2 millivolts per degree Celsius when measured at a sense current of 10ma.

Figure 2. Typical Temperature Calibration Curve for a TMOS™ body diode.

Other device electrical parameters have similar linear relationships to temperature as well. The following are several other temperature sensitive parameters used in the industry to determine a device's junction temperature.

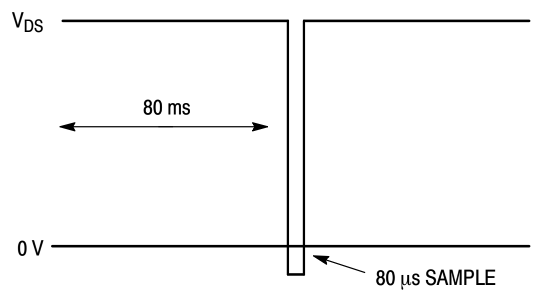
Common TSP:	Device Type:
V_{TH}, $V_{DS(on)}$, $R_{DS(on)}$	MOSFET
V_{TH}, $V_{CE(s)}$	IGBT
V_{BE}, $V_{CE(s)}$	Bipolar
V_F	Diode

Make sure to develop the actual electrical to thermal correlation of the TSP and check it for linearity prior to its use. The linearity of this parameter is critical for accurate thermal measurement.

2. Applying Continuous Power and TSP Sampling Pulses

With a properly chosen and calibrated TSP, we can now provide test signals to the device and make thermal measurements.

We begin by applying a continuous power of known current and voltage to the device. A continuous train of sampling pulses monitors the TSP, and thus the junction temperature. The TSP sampling pulse must provide a sense current equal to that used during calibration. While monitoring the TSP, adjust the applied power so as to insure a sufficient rise in T_J. Adjusting the applied power to achieve a T_J rise of about 100° above the reference temperature will generate enough temperature delta to insure good measurement resolution.



A continuous pulse train consisting of an 80 ms power pulse followed by an 80 μs diode sample is used to apply both power to the device as well as a sample pulse for TSP measurement.

Figure 3. Example of a power and sample pulse train during R_{thjc} measurement of a TMOS device.

The TSP sample time must be very short so as to not allow for any appreciable cooling of the junction prior to re−applying power. The power and sample pulse train shown in Figure 3 has a duty cycle of 99.9% which for all practical purposes is considered continuous power.

Obviously, with this much power being applied to the device under test, the device's case will get very hot. To keep the device cool while under test, we need to mount it to a heat sink of some sort. A heat exchanger with chilled water flowing through it provides a good heat sink. In this way, we can keep the device's case temperature down (i.e., near 25°C) and maintain good measurement resolution (i.e., large temperature delta between the junction and reference location).

3. Measuring T_J, T_R, and Applied Power

After T_J has stabilized, we must record its value along with the reference temperature, T_R, and applied power. To calculate the devices maximum power rating, P_D, and thermal resistance, R_{thjr}, we need to have these measurements.

The devices junction temperature, T_J, is taken from the TSP electrical measurement. With the correlation between the TSP electrical measurement and temperature already established, determining T_J is pretty much straight forward.

A thermocouple placed at the reference location measures the reference temperature, T_R. Most power semiconductor manufacture's use the devices' case, however, the lead, ambient, or all three can be used as reference locations.

Key elements to insure accurate reference temperature measurement are:

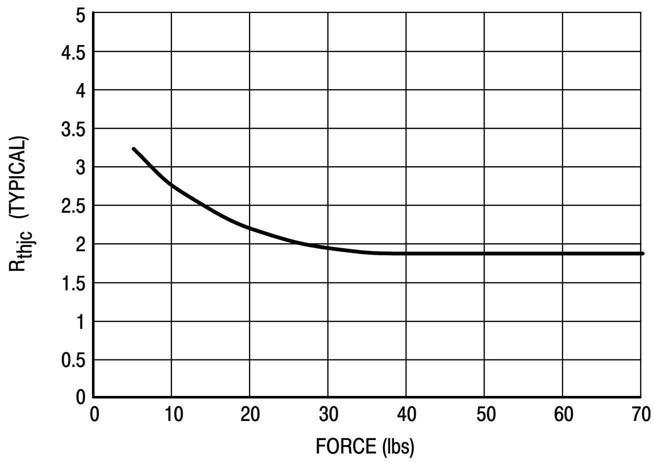
- Good thermocouple to reference contact
- Consistent thermocouple placement location

The reference thermocouple needs to make a good thermal contact to its reference location. This applies to reference locations other than ambient. Without a good thermal contact, measurement error will occur. To improve this contact, use both thermal grease and device clamping pressure as suggested.

Use thermal grease to insure good thermal conductivity and to eliminate air gaps. Applying thermal grease between the device and the heat sink used to keep the case temperature near 25°C will help in two ways. First, it will help keep the case temperature down during measurement by improving the thermal contact to the heat sink. Second, it will also improve the thermocouple to case contact as well. As stated earlier, the case is usually used as the reference location for thermal measurements. Thermal grease helps to maintain good thermal contact and insure measurement accuracy.

Applying about 40 lb of force (85 to 90 PSI) between the thermocouple and the reference location (i.e., device's case) also improves the thermal contact as shown in Figure 4. The application of pressure to the device seems to smooth out thermal grease thickness variations and eliminate air gaps at the contact interface.

Taking these precautions into consideration will help insure a good thermal contact to the reference location surface (i.e., device case).



The value of measured thermal resistance drops and becomes consistent at about 40 lb. of clamp force (85−90 PSI) insuring good thermal contact between the thermal couple and the devices case. [1]

Figure 4. R_{thjc} vs. Clamp Force for a ON Semiconductor MJF10012 TO−218 Fullpak device with uncontrolled thermal grease thickness.

The reference thermocouple needs to be placed at the same location for every device. Any change in the placement of this thermocouple will result in error or at the very least inconsistencies between measurements. A different thermal resistance exists between the junction and the location of each thermocouple placement. Usually for the best readings, the reference thermocouple should be placed at the hottest location on the package (i.e. for TO−220 devices, at the center of the die on the back side of the devices metal case). In any event, to be accurate and consistent, always place the reference thermocouple in the same location for each device measured.

4. Calculating Thermal Resistance, $R_{thj(r)}$, and Maximum Power, P_D

We can use equations (1) and (2) presented earlier, along with our measurements, to calculate the devices thermal resistance and maximum power capability.

Assuming we measured the following; T_J = 100°C, applied test power = 50 W, T_C = 25°C, and maximum device temperature rating = 150°C, we use equation (1) to calculate R_{thjc}.

$$R_{thjc} = (100 - 25)/50$$
$$= 1.5°C/W \text{ (measured value)}$$

Most manufacturer's will guardband the measured R_{thjr} reading to establish their device limits. This helps take into consideration all of the variables involved which cause inconsistencies in readings. A guardband of 25% for thermal measurements is considered good practice.

Multiplying the measured thermal resistance from above by 1.25 to guardband it by 25%, we get the following specified R_{thjc}.

$$R_{thjc} = 1.5 * 1.25$$
$$= 1.9°C/W \text{ (manufacturer's guaranteed limit)}$$

As shown in the Figure 5, the thermal resistance from junction to case is largely dependent on the die size of the device. This implies that silicon has a much larger thermal resistance, or opposition to heat flow, than that of the copper header to which it is bonded to.

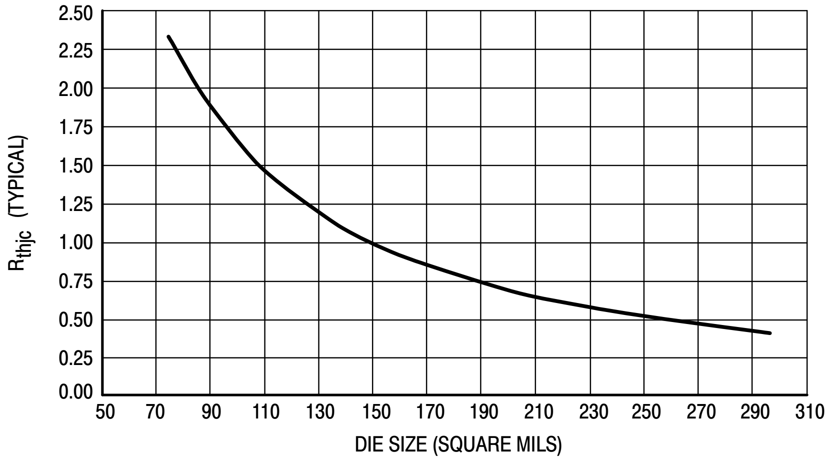


Figure 5. R_{thjc} vs. die size for TMOS® devices in TO−220, D^2PAK, DPAK & TO−247 Packages.

To determine a devices power handling capability, P_D, we use the specified R_{thjc} taken from above along with equation (2).

$$P_D = (150 - 25)/1.9$$
$$= 66 \text{ W (manufacturer's guaranteed limit)}$$

Using Thermal Parameters to Solve Often Asked Thermal Questions

One can use measured or specified thermal parameters to solve many common questions asked about power semiconductor devices. The two examples shown below use thermal parameters to solve frequently asked questions.

Example #1

Calculate the device's junction temperature: Using equation (3) with a known R_{thjc} of 1.25°C/W, case temperature of 85°C, and applied power of 35 W.

$$T_J = 35 * 1.25 + 85$$
$$= 128.8°C$$

Example #2

Calculate the power handling capability : Using equation (2) with a known R_{thjc} of 1.0°C/W, a starting case temperature of 75°C and a maximum rated T_J of 150°C.

$$P_D = (150 - 75)/1.0$$
$$= 75 \text{ W}$$

SUMMARY

This paper presents a description of basic semiconductor thermal measurement as well as the use of thermal data in real world examples. Included are terms, definitions, equations and test equipment required. This provides the reader with information useful in answering many common questions regarding the basic thermal capabilities of power semiconductor devices.

REFERENCES

[1] Billings, Dave, 1992, “Thermal Performance of the TO−218 Fullpak MFJ10012 under Force Loading”, ON Semiconductor.

[2] Gottlieb, Irving M., 1992, *Regulated Power Supplies,* 4th Edition, Blue Ridge Summit, Pennsylvania, TAB BOOKS: (92−105).

[3] Pshaenich, Al, “Basic Thermal Management of Power Semiconductors”, ON Semiconductor Application Note *AN1083.*

[4] Roehr, Bill and Bryce Shiner, “Transient Thermal Resistance — General Data and its Use”, AN569 in ON Semiconductor *Power Applications Manual,* 1990: (23−38), ON Semiconductor Literature Distribution Center, Ph. # 1 (800) 344−3860.

This data was collected using thermal test die in 20-pin PLCC packages on PLCC test boards (2.24″ x 2.24″ x .062″ glass epoxy, type FR-4, with solder coated 1 oz./sq. ft. copper).

Integrated Circuit Package Thermal Management

Circuit performance and long−term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit − from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).

$\overline{\theta}_{JC}$ = average thermal resistance, junction to case

$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient

$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This ON Semiconductor recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL−M−38510(JAN) MECL 10K devices.

Only two terms on the right side of equation (1) can be varied by the user − the ambient temperature, and the device case−to−ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

Table 1. Thermal Resistance Values for Standard MECL I/C Packages

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	EPOXY	1/4″×3/8″	EPOXY	2496	8100	102	133	50	80
8	DIL	ALUMINA	1/4″×3/8″	SILVER/GLASS	2496	N/A	140	182	35	56
14	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	6400	84	109	38	61
14	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
16	DIL	EPOXY	1/4″×3/4″	EPOXY	4096	12100	70	91	34	54
16	DIL	ALUMINA	1/4″×3/4″	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.35″×0.35″	EPOXY	4096	14,400	74	82	N/A (6)	N/A (6)
24	DIL (4)	EPOXY	1/2″×1−1/4″	EPOXY	8192	22500	67	87	31	50
24	DIL (5)	ALUMINA	1/2″×1−1/4″	SILVER/GLASS	8192	N/A	50	65	10	16
28	PLCC	EPOXY	0.45″×0.45″	EPOXY	7134	28,900	65	68	N/A (6)	N/A (6)

NOTES:

1. All plastic packages use copper lead frames − ceramic packages use alloy 42 frames.
2. Body style DIL is "Dual−In−Line."
3. Standard Mounting Methods:
   a. Dual−In−Line In Socket or P/C board with no contact between bottom of package and socket or P/C board.
   b. PLCC packages solder attached to traces on 2.24″ × 2.24″ × 0.062″ FR4 type glass epoxy board with 1 oz./S.F. copper (solder coated) mounted to tester with 3 leads of 24 gauge copper wire.
4. Case Outline 649
5. Case Outline 623
6. $\theta_{JC} = \theta_{JA} - \left(\frac{T_C - T_A}{P_D}\right)$

T_C = Case Temperature (determined by thermocouple)

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature−controlled heatsink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D\,(\overline{\theta}_{JC}) \qquad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Table 1. In , this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life ($\geqslant$ 100,000 hours for ceramic packages).

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) is illustrated in the graphs of Figure 6 through Figure 8. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual−in−line packaged MECL 10K quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 9, $\overline{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D\,(\overline{\theta}_{JA}) + T_A$$

$$T_J = (0.195\text{ W})\,(50°\text{C/W}) + 25°\text{C} = 34.8°\text{C}$$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

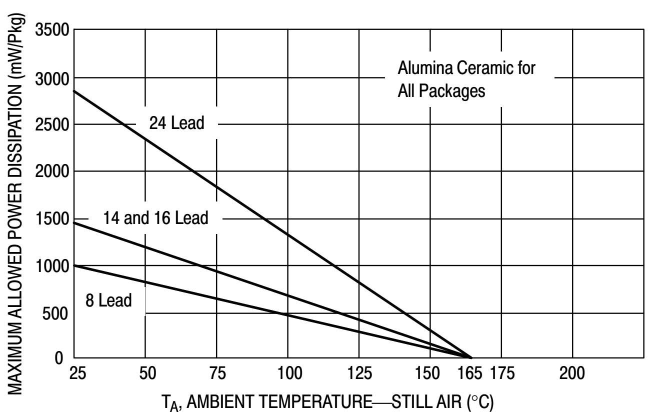


Figure 6. Ambient Temperature Derating Curves (Ceramic Dual−In−Line Pkg)

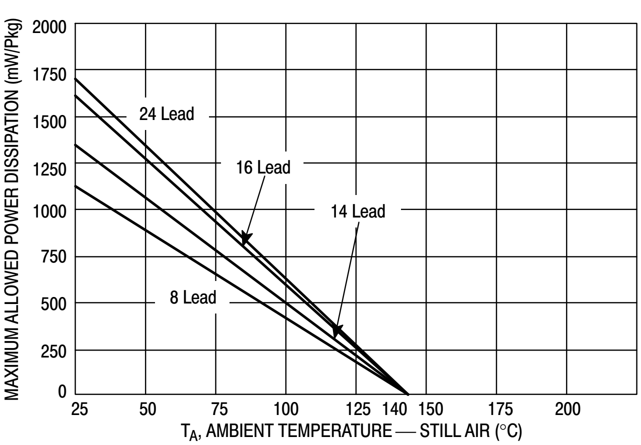


Figure 7. Ambient Temperature Derating Curves (Plastic Dual−In−Line Pkg)

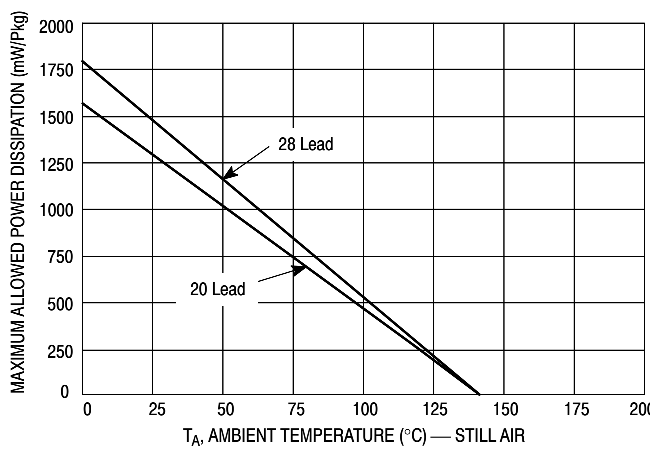


Figure 8. Ambient Temperature Derating Curves (PLCC Pkg)

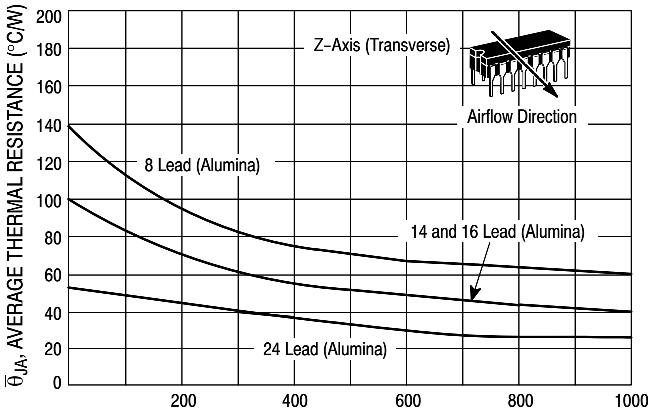


Figure 9. Airflow versus Thermal Resistance (Ceramic Dual-In-Line Pkg)

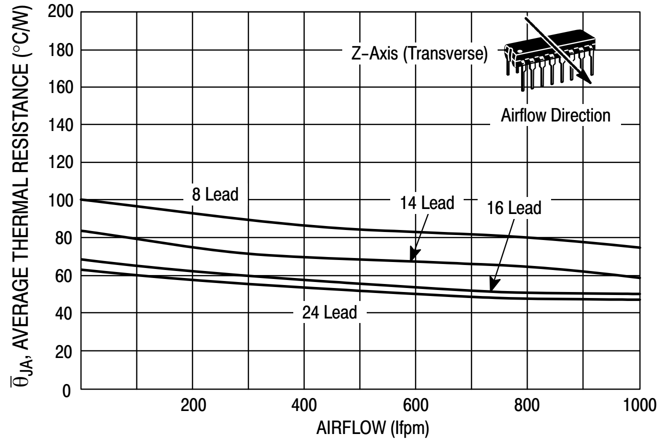


Figure 10. Airflow versus Thermal Resistance (Plastic Dual-In-Line Pkg)

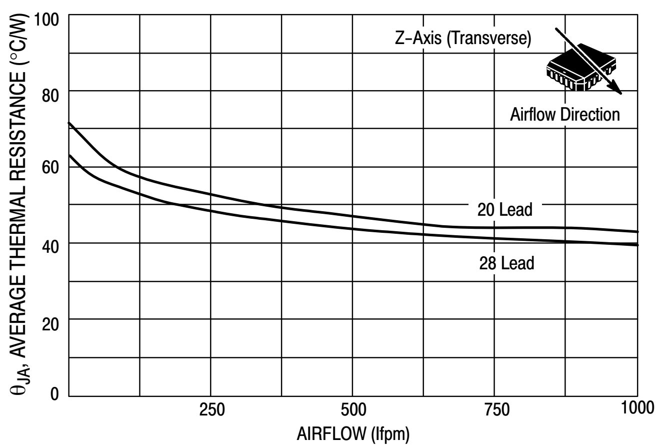


Figure 11. Airflow versus Thermal Resistance (PLCC Pkg)

Table 2. Thermal Gradient of Junction Temperature (16-Pin MECL Dual-In-Line Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062″ PC board with Z axis spacing 0.5″. Air flow is 500 lfpm along the Z axis.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipations. Table 2 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual-in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$\text{(1) } T = (6.376 \times 10^{\boxed{2}})\, e\left[\frac{11554.267}{273.15 + T_J}\right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

(2) $T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on−chip power dissipation.

Table 3 shows the relationship between junction temperature, and continuous operating time to 0.1% bond failure, (1 failure per 1,000 bonds).

Table 3. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temp °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 3 is graphically illustrated in Figure 12 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid−life failure rates of plastic devices are not effected by this intermetallic mechanism.

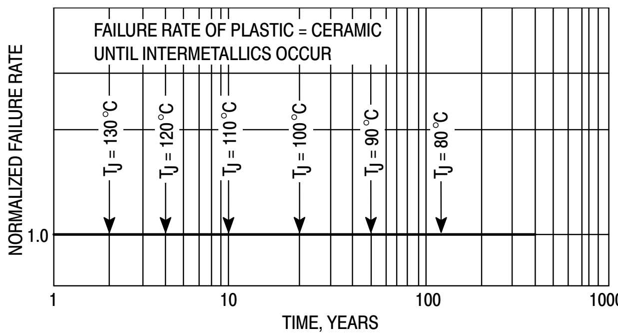


Figure 12. Failure Rate versus Time Junction Temperature

MECL Junction Temperatures:

Power levels have been calculated for a number of MECL 10K and MECL 10H devices in 20 pin plastic leaded chip carriers and translated to the resulting increase of junction temperature (ΔT_J) for still air and moving air at 500 LFPM using equation 2 and are shown in Table 4.

Table 4. Increase in Junction Temperature Due to I/C Power Dissipation.
20 Pin Plastic Leaded Chip Carrier

MECL 10K Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air	MECL 10H Device Type	ΔT_J, °C Still Air	ΔT_J, °C 500 LFPM Air
MC10101	21.8	14.1	MC10H016	48.0	30.0
MC10102	17.6	11.4	MC10H100	16.6	10.8
MC10103	17.6	11.4	MC10H101	22.1	14.5
MC10104	20.8	13.4	MC10H102	18.0	11.8
MC10105	17.2	11.2	MC10H103	18.0	11.8
MC10106	13.0	8.4	MC10H104	21.0	13.5
MC10107	19.8	12.8	MC10H105	17.8	11.7
MC10109	11.7	7.7	MC10H106	13.2	8.7
MC10110	24.7	16.1	MC10H107	20.0	12.9
MC10111	24.7	16.1	MC10H109	11.9	7.8
MC10113	22.2	14.3	MC10H113	22.8	14.8
MC10114	22.6	14.6	MC10H115	16.7	10.9
MC10115	16.7	10.9	MC10H116	17.8	11.7
MC10116	17.2	11.1	MC10H117	16.7	11.0
MC10117	16.2	10.5	MC10H121	13.9	9.1
MC10121	13.5	8.5	MC10H123	23.1	15.0
MC10123	37.6	24.0	MC10H124	44.2	28.4
MC10124	42.9	27.3	MC10H125	–	–
MC10125	–	–	MC10H130	28.2	18.2
MC10131	26.9	17.1	MC10H135	33.2	21.4
MC10133	34.4	21.9	MC10H136	61.7	38.5
MC10134	27.0	17.2	MC10H141	44.3	28.0
MC10135	31.9	20.3	MC10H158	25.3	16.4
MC10136	52.3	32.6	MC10H159	27.3	17.7
MC10138	37.0	23.2	MC10H160	32.1	20.5
MC10141	42.7	26.7	MC10H161	41.5	26.7
MC10153	34.4	21.9	MC10H162	41.5	26.7
MC10158	23.9	15.2	MC10H164	31.9	20.6
MC10159	25.8	16.4	MC10H165	56.3	35.8
MC10160	32.0	20.4	MC10H166	44.4	28.3
MC10161	40.7	26.0	MC10H171	41.9	26.9
MC10162	40.7	26.0	MC10H172	41.9	26.9
MC10164	31.3	20.1	MC10H173	32.6	21.1
MC10165	53.7	33.6	MC10H174	32.5	21.0
MC10166	43.5	27.6	MC10H175	45.9	29.6
MC10168	34.4	21.9	MC10H176	50.9	32.3
MC10170	29.9	18.9	MC10H179	35.0	22.6
MC10171	41.1	26.2	MC10H180	42.4	27.2
MC10172	41.1	26.2	MC10H181[4]	64.4	38.6
MC10173	30.5	19.3	MC10H186	50.2	31.8
MC10174	31.9	20.5	MC10H188	25.8	16.7
MC10175	43.7	27.6	MC10H189	25.8	16.7
MC10176	49.6	31.3	MC10H209	18.9	12.5
MC10178	38.1	23.9	MC10H210	25.0	16.4
MC10186	49.6	31.1	MC10H211	25.0	16.4
MC10188	25.4	16.4	MC10H330[4]	65.8	36.1
MC10189	24.6	15.9	MC10H332	52.2	33.5
MC10192	67.0	43.0	MC10H334	77.8	49.3
MC10195	46.7	29.9	MC10H350	–	–
MC10197	27.7	17.7	MC10H351	27.2	18.1
MC10198	21.2	13.4	MC10H352	27.2	18.1
MC10210	24.5	16.0	MC10H424	37.7	24.3
MC10211	24.6	16.0			
MC10212	24.3	15.8			
MC10216	24.1	15.6			
MC10231	30.6	19.5			

NOTES:
(1) All ECL outputs are loaded with a 50 Ω resistor and assumed operating at 50% duty cycle.
(2) ΔT_J for ECL to TTL translators are excluded since the supply current to the TTL section is dependent on frequency, duty cycle and loading.
(3) Thermal Resistance (θ_{JA}) measured with PLCC packages solder attached to traces on 2.24″ x 2.24″ x 0.062″ FR4 type glass epoxy board with 1 oz./sq. ft. copper (solder−coated) mounted to tester with 3 leads of 24 gauge copper wire.
(4) 28 lead PLCC.

Case Example:

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each plastic device in the system should be evaluated for maximum junction temperature using Table 4. Knowing the maximum junction temperature refer to Table 3 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 12.

To illustrate, assume that system ambient air temperature is 55°C (an accepted industry standard for evaluating system failure rates). Reference is made to Table 4 to determine the maximum junction temperature for each device for still air and transverse air flow of 500 LFPM.

Adding the 55°C ambient to the highest, ΔT_J listed, 77.8°C (for the MC10H334 with no air flow), gives a maximum junction temperature of 132.8°C. Reference to Table 3 indicates a departure from the desired failure rate after about 2 years of constant exposure to this junction temperature. If 500 LFPM of air flow is utilized, maximum junction temperature for this device is reduced to 104.3°C for which Table 3 indicates an increased failure rate in about 15 years.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K and MECL III devices are given for an operating temperature range from −30°C to +85°C (0° to +75°C for MECL 10H and memories). These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heatsinking (i.e., dual−in−line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non−metalized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low−power device types may be used without air and with higher $\overline{\theta}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\theta}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual−in−line ceramic device operated at $\overline{\theta}_{JA}$ = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\overline{\theta}_{JA}$ = 50°C/W. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heatsinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEATSINK SUGGESTIONS

With large high−speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two−sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two−ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 13, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug−in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

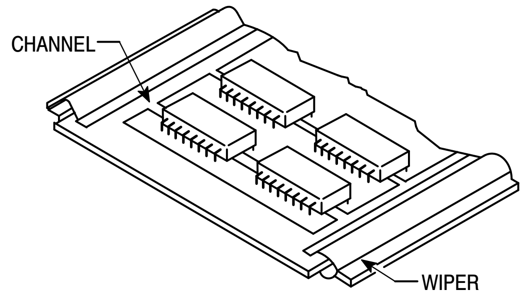


Figure 13. Channel/Wiper Heatsinking on Double Layer Board

For operating some of the higher power device types* in 16 lead dual−in−line packages in still air, requiring $\overline{\theta}_{JA}$ <100°C/W, a suitable heatsink is the IERC LIC−214A2WCB shown in Figure 14. This sink reduces the still air $\overline{\theta}_{JA}$ to around 55°C/W. By mounting this heatsink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for MECL 10H memories) or in lowering T_J for improved reliability.

It should be noted that the use of a heatsink on the top surface of the dual−in−line package is not very effective in lowering the $\overline{\theta}_{JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

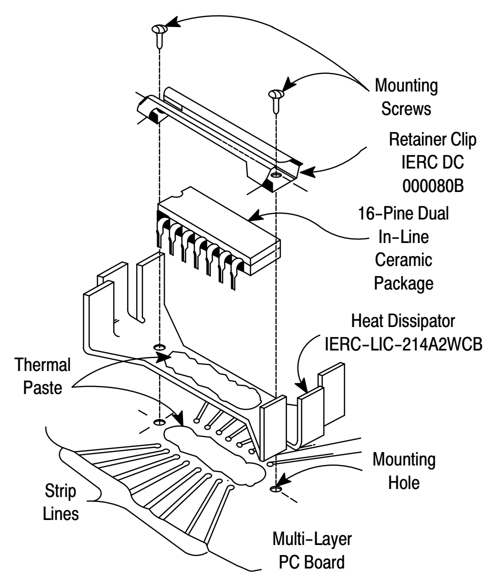


Figure 14. MECL High−Power Dual−in−Line Package Mounting Method

Thermal Characterization of the SO-8 Package for Power Semiconductor Applications

Kent Kime, Mike Lissy, Dave Shumate and Larry Walker
ON Semiconductor

ABSTRACT — A very up–and–coming package for power semiconductor applications is the SO–8 (also known in the IC world as the SOIC8) package. The purpose of this work is to present the thermal characterization (with emphasis on R_{thja}), both measured and modeled, of this package configured with a power transistor. The paper presents in detail results of characterizing three different package configurations: a) dual die, b) single large die, and c) single small die. The dual die and single large die configurations were used to establish the finite element model accuracy. The model was then used to predict the thermal performance in the untested single small die configuration. The model predictions matched the measured results thus validating the modeling effort. Factors such as solder voiding, die attach technique, junction depth, convective heat transfer coefficient and die thickness that could affect the modeling results were examined and their criticality assessed. As a verification to the modeling and measurements, infrared images were also made of the devices while under test.

INTRODUCTION

Actual measured thermal characterizations of semiconductor devices and packages can be very time consuming. If it is desired to evaluate multiple silicon and package configurations, the experimentation can take weeks. This is not acceptable in today's 10x, "first–to–market" product environment. One answer to this dilemma is thermal modeling. The goal here was to establish a verified model from which the major geometric, material and process variables affecting thermal performance can be determined.

Historically, the focus in power devices was the case–mounted part where the thermal model considered a series of resistances from junction (heat source) through the die, from die to the case and from the case to ambient. Traditional methods of viewing thermal resistance need to be expanded or at least viewed with greater understanding for surface mount packages. DPak and other case–mounted packages have been thermally characterized using R_{thjc} since a large portion of the case is attached to the board. For lead–mounted packages, SO–8, SOT–223, et al., however, the primary heat transfer is not through a board attached case but through the leads, and convection from the package surface becomes a significant factor. This can be seen in the simple parallel resistor analogy for heat dissipation shown in Figure 1, where R1 is the convection from the package surface and R2 is the conduction through the mounting surface. R1 is much greater than R2 for case–mounted packages. R1 is roughly the same order of magnitude as R2 for lead–mounted packages. Because of this, even small changes in the configuration of lead–mounted packages can drastically influence their thermal performance. Modeling makes determining this influence a manageable task.

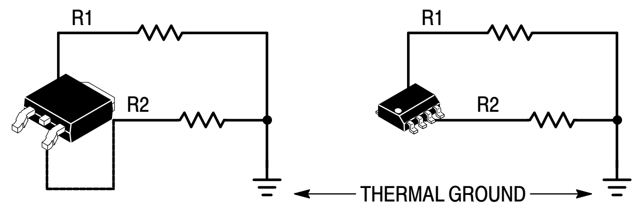


Figure 15. Parallel Resistor Analogy for Case–Mounted and Lead–Mounted Configurations

Definition of terms

DOE = Design of Experiments

DUT = Device–Under–Test

FEA = Finite–Element Analysis

FEM = Finite–Element Model

HTC = Heat Transfer Coefficient

PCB = Printed Circuit Board

P_D = Power Dissipation

R_{thja} = Thermal resistance, junction–to–ambient

R_{thjc} = Thermal resistance, junction–to–case

T_J = Junction Temperature

T_R = Reference Temperature

T_A = Ambient Temperature

TSEP = Temperature Sensitive Electrical Parameter

Device Thermal Measurements

In this section, thermal measurement techniques and the results of three experiments are discussed. Thermal characterization techniques are well established and have been standardized under such organizations as JEDEC and SEMI [1, 2]. Hence, there exists a certain level of confidence in the measured results. However, due to the nature of these measurements, there are always questions about accuracy; large percentage variations are not uncommon. The effort described in this paper establishes two key points: 1) accurate thermal modeling of power semiconductors can be accomplished with minimal experimental validation and 2) effective modeling can be used to illuminate the existence and sources of experimental error prevalent in this type of evaluation.

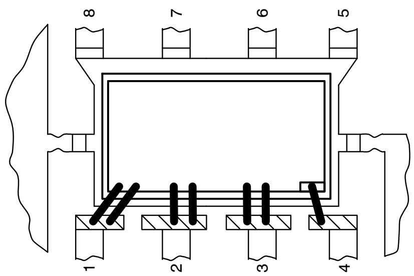


Figure 16. Device 1 − ON Semiconductor's MMSF5N03HD SO−8 package, 98 x 120 mil die, 1 die per package

In order to provide data for thermal finite−element model correlation efforts, two power semiconductor devices, shown in Figures 2 and 3, were characterized by the characterization laboratory.

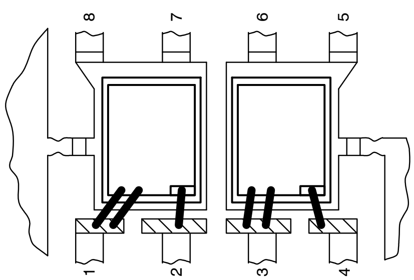


Figure 17. Device 2 − ON Semiconductor's MMDF3N03HD SO−8 package, 57 x 99 mil die, 2 die per package

Once the modeling technique was established with these two platforms, a double−blind experiment was conducted on a similar device with a slightly different configuration to demonstrate the modeling viability. The device used for this phase is shown in Figure 4.

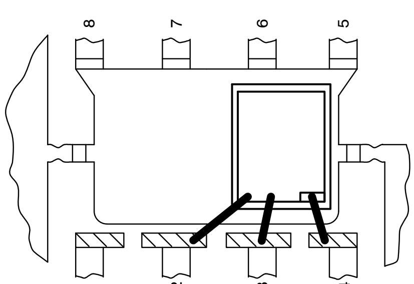


Figure 18. Device 3 − ON Semiconductor's MMSF2P02E SO−8 package, 57 x 99 mil die, 1 die per package

Since the modeling effort was launched from laboratory measured data, a verification of the laboratory results was warranted. Validation of the thermal characterization was achieved by utilizing thermal imaging techniques performed in an independent laboratory. What is fortunate about this method is that a correct temperature correlation can be established for the laboratory measurements and simultaneously thermal topographical mapping of the test coupon is provided, which can also be directly compared to the finite−element model's thermal profiles.

A. Thermal Characterization Techniques

Non−invasive, thermal resistance measurements are well established and quite mature. The general approach to thermal characterization of a semiconductor device is straightforward; many papers have been written on this topic [3]. First, the basic equation for thermal resistance used in the semiconductor industry is

$$R_{thjr} = \frac{T_J - T_R}{P_D} \quad (1)$$

Generally, T_J is measured utilizing an electrical characteristic of the device that is repeatable and an accurate function of temperature. This is usually referred to as the temperature sensitive electrical parameter (TSEP). The parameters most often used for MOSFETs are either $V_{GS(th)}$, $R_{DS(on)}$ or V_{SD} (the body diode forward voltage drop). The values of the parameter are established over the temperatures of interest, thus calibrating the TSEP "thermometer". During thermal characterization the TSEP is sampled to determine T_J. T_R is ordinarily measured with a thermocouple at the point of interest. P_D is simply the power dissipated by the device.

There are many sources for error in these thermal measurements. Also, there are many misunderstandings about the thermal resistance values. Most TSEPs for a given device have small, hard−to−measure changes over temperature. For example, V_{SD} may only change 2 mV per degree Celsius; therefore, sub−millivolt accuracy is needed to measure T_J. T_R accuracy depends on the thermocouple, its mounting techniques and its time response. To minimize heat "wicking" from the DUT small gauge conductors and four−wire measurement techniques are employed for P_D measurements. P_D can also be quite low (< 500 mW) for small surface mount devices which makes it difficult to measure accurately.

A key factor in understanding thermal resistance measurements is that if the application configuration is different from that of the measured device, the thermal results will be different. Thermal data on manufacturers' data sheets is designed for comparison with other manufacturers' devices and to give the user a place to begin their thermal management solution.

Test devices were mounted on 2 x 2 x 0.06 in. FR4/G10 printed circuit boards. The printed circuit pattern is a 1 x 1 in., 2 oz. copper pad with 10 mil separations for the leads. Figure 5 shows the test coupon layout. Due to some tester limitations, test devices were mounted to the PCB with the gate and source leads shorted together, essentially making the device into a rectifier. Since the body diode was the chosen TSEP, this change was thermally insignificant. Once mounted on the PCB and its support structure, the devices were placed for measurement in the center of a standard still−air chamber. The still−air chamber is a 1 ft. x 1 ft. x 1 ft. sealed chamber that prevents external sources of air movement around the DUT from affecting the measurements. Only natural convection is allowed. The test setup is then interfaced to the Analysis Tech™ Semiconductor Thermal Analyzer.

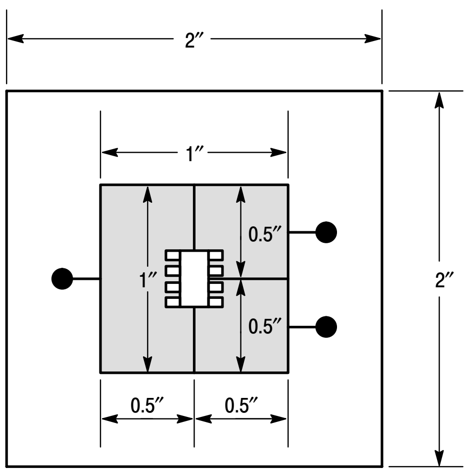


Figure 19. Thermal Test Coupon Layout

Almost all thermal analyzer equipment operates on the same principle. The DUT is powered by the tester for ≈99.9% of the cycle and the TSEP is measured for the other 0.1%. For steady−state thermal resistance, power is applied until T_J statistically stabilizes. T_R and P_D are measured simultaneously with T_J and, thus, thermal resistance is measured. For transient or pulsed power conditions, the pulse is applied and the TSEP is measured before and after it, indicating the ΔT_J during the pulse. For measuring thermal resistance as a function of time, the two methods most commonly used are referred to as cooling−curve and heating−curve techniques.

Briefly, in the cooling−curve scenario, the device is heated by applying P_D until T_J is at the desired value. After stabilization, power is removed from the device, and T_J and T_R are measured at precise time intervals during cool down. Using Equation 1, and the values measured, a thermal resistance versus time relationship is obtained.

For the heating−curve method, successive power pulses of programmed widths which produce the same ΔT_J are applied. The device is allowed to cool between pulses. These pulses are continued until steady−state T_J is reached. ΔT_R and P_D are measured simultaneously with ΔT_J; hence, the thermal resistance versus time characterization is produced. Generally, the heating−curve method is considered the more accurate technique due to the higher resolution created by the consistent ΔT_J, and because this testing technique operates the device in the manner it's most likely to be used.

B. Thermal Test Results

As mentioned before, three devices were characterized in the laboratory: two devices before FEA and one after. Both transient and steady−state thermal resistance values were obtained. The data is shown in Table 1 and Figures 6 through 8.

Figures 6 through 8 show the transient response curves generated for the devices' data sheets. Note the RC thermal networks that can be used in circuit simulator programs to determine T_J under any power input conditions. These thermal resistance versus time curves were generated using the heating–curve method. The curves shown are normalized at 10 seconds.

Table 5. Thermal Characterization Data for Three Devices mounted on 1 in. sq. Cu area PCB.

Device	Measured Steady−State R_{thja}	FEM Predicted Steady−State R_{thja}
MMSF5N03HD	70.3°C/W	70.1°C/W
MMDF3N03HD	87.0°C/W	84.5°C/W
MMSF2P02E	74.6°C/W	72.2°C/W

C. Device Infrared Thermal Imaging

As mentioned before, to help "triangulate" on the correct results for this characterization, thermal imaging was employed. The point here is to provide an independent "sanity check" for both the modeling and the laboratory measurements.

The thermal imaging procedure is fairly straightforward. First, as with standard thermal characterizations, power must be applied which raises the junction temperature to a known value. Again, this requires device TSEP calibration. Fortunately, in the case of a rectifier, the only parameter needed by the imaging laboratory is the current required (to the exact mA) to produce the desired T_J. Only steady–state correlation was obtainable with the thermal imaging equipment available at the Mechanical Engineering Laboratory.

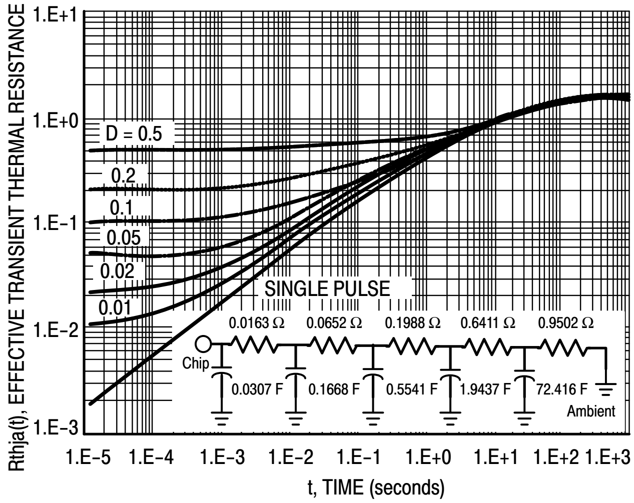


Figure 20. Transient Thermal response for MMSF5N03HD mounted on 1 in. sq. Cu area PCB.

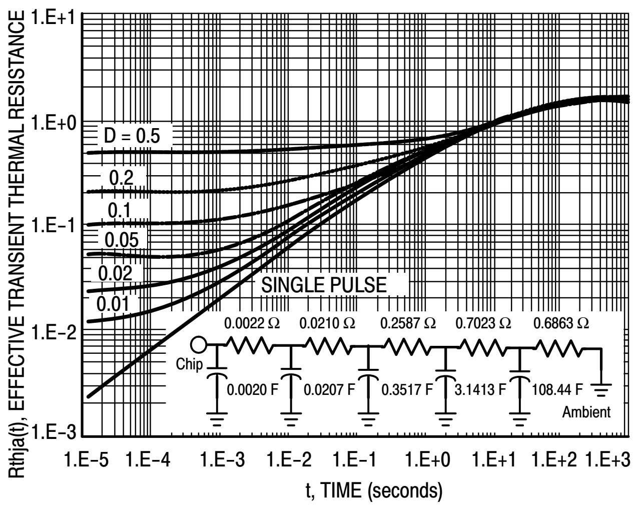


Figure 21. Transient Thermal response for MMSF2P02E mounted on 1 in. sq. Cu area PCB.

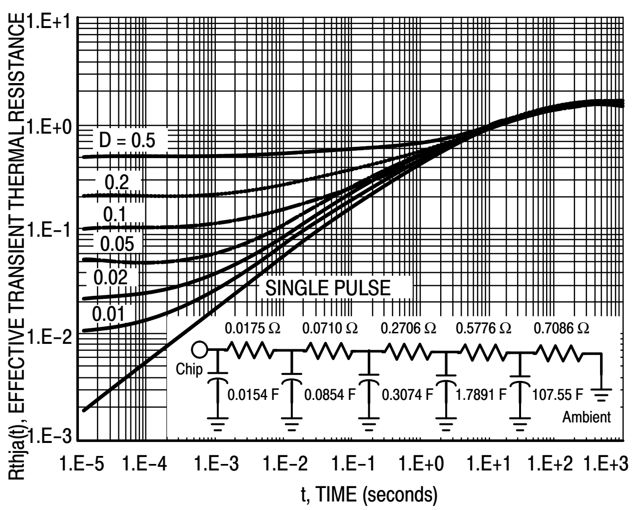


Figure 22. Transient Thermal response for MMDF3N03HD mounted on 1 in. sq. Cu area PCB.

Once a sample is prepared for emmissivity differences and mounted in the IR camera setup, the current is applied and the device temperature is allowed to stabilize. Thermal image photographs are then taken in which distinct temperature points are identified and the thermal profile is mapped. An IR image of the steady−state thermal profile of Device 1 is compared to FEA predictions in Figure 9 and Figure 10.

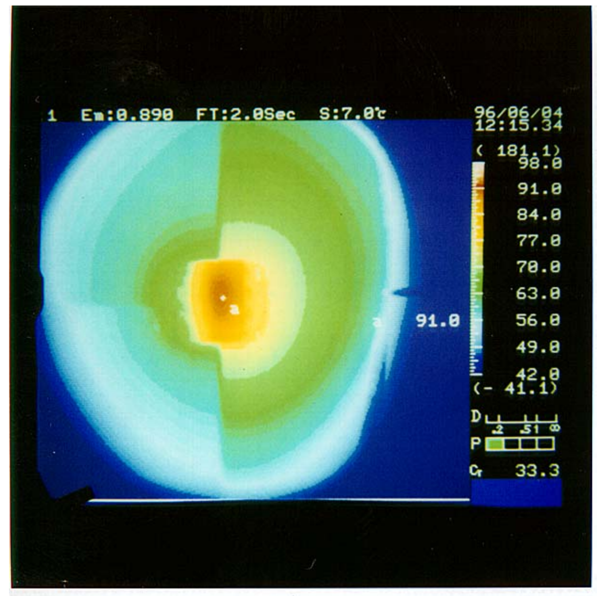


Figure 23. Thermal image of SO−8 package mounted on test coupon with power applied of 0.96 W.

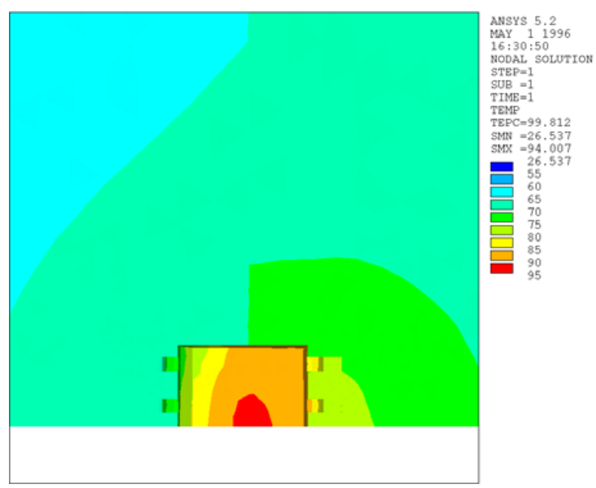


Figure 24. FEA steady−state temperature distribution on Device 1, half symmetry model at 0.96 W.

The maximum measured device surface temperature of 91°C compares well with the 93°C predicted by FEA. The measured and modeled steady−state thermal contours agree to within two to three degrees Celsius.

Finite Element Modeling

The finite−element analysis presented in this paper was performed in three stages. First, following DOE methodology, finite−element modeling was used to determine the relative importance of key variable factors related to the thermal performance of the SO−8 package. Next, the results of the DOE were used to provide direction to achieve correlation between the finite−element model predictions and thermal test results for Devices 1 and 2. Finally, the correlated SO−8 model was used to predict the thermal performance of Device 3.

A. Finite−ElementModel Description

1. MODEL GEOMETRY

Three−dimensional solid models of the three different SO−8 configurations were made using IDEAS™ solid modeling software. The solid models were meshed with linear tetrahedral elements using the free−meshing capability in IDEAS. IDEAS was then used to translate the resulting meshes into ANSYS™ format. Boundary conditions were applied and the solutions run and post−processed using ANSYS.

2. BOUNDARY CONDITIONS

The boundary conditions consist of power applied to the die and heat transfer coefficients (HTCs) applied to external surfaces of the model. Power is applied to each model by specifying a heat flux over the active area of the die surface. The total power applied depends on the configuration: 2 watts to Device 1, 1.5 watts to Device 2, and 2.25 watts to Device 3.

Convective heat transfer to the air surrounding the part and test board is included by applying HTCs to the package top and both the upper and lower surfaces of the test coupon. The HTCs were calculated based on the approach used for free convection from horizontal flat plates outlined in [4, 5]. The interested reader will find the calculations for the HTCs used in this analysis in Appendix A. All surfaces without HTCs are assumed to be adiabatic.

B. Analytical DOE using FEA

1. EXPERIMENTAL DESIGN

The first phase of the analysis process involved using finite−element modeling to determine which parameters have the greatest influence on the thermal performance of the SO−8 package. The authors selected 6 parameters (listed in Table 2) believed to be of primary importance in determining package thermal performance. A designed experiment was generated in which each of these factors was varied from a selected minimum to maximum value. This was a factorial class 2^{6-2} with 16 runs plus 2 centerpoints (18 runs total) experiment. The range of variation of each factor is listed in Table 2. These ranges were selected by the authors to bracket what is commonly observed. The response variable was R_{thja} on the 1 inch copper pad. The general result of this first experiment was used to design a second experiment to investigate package design factors.

2. EXPERIMENTAL PROCEDURE

The experiment was conducted analytically using the ANSYS model of Device 1. In order to eliminate any effects that mesh density might have on the solutions, the same number of nodes and elements was used in each of the runs.

The procedure was to first use IDEAS to generate a mesh with the proper die and epoxy thicknesses. The mesh was transferred to ANSYS where the appropriate material properties were defined (silver epoxy and solder conductivities) and boundary conditions (power and HTCs) applied. A steady−state thermal solution was then performed and post−processed using ANSYS. The ANSYS results were then used to calculate a steady−state R_{thja} for each run using Equation 1 with T_R equal to T_A.

3. RESULTS OF DOE

The first experiment indicated that HTC was the only statistically significant variable. Device suppliers generally have no control over HTC and thus the impact of the other variables was desired. To see the significance of the other variables, a new factorial experiment (2^{5-1} with 16 runs) in which the HTC was kept constant was designed and conducted. Table 3 shows the inputs and responses. The analysis indicated that several input variables were significant such as die thickness, die attach thickness, solder board voiding and device junction depth. No interactions were statistically significant. An “F” value of 159 and a “p” value of less than 0.01% indicated the significance of this experiment. The analysis of the residuals indicates no non−linear dispersion and all of the assumptions of the analysis of variance were met (see Montgomery [6]).

Table 3 shows the relative strength of each of the pooled model variables. Die thickness has the strongest effect on the model. Tables 2 and 3 illustrate the predicted responses. The overall response variation from the experiment was only 3°C /Watt. Another main point of this analysis is that no interactions are significant.

Combining the results of the two designed experiments shows that HTC is the most significant variable. In order to get accurate modeling data, it is necessary to know the HTC value for the environmental conditions. The others variables do not play a significant role in the thermal model for <u>steady−state</u> R_{thja}.

C. FEA Correlation with Thermal Measurements

Prior to finite−element modeling of these parts, thermal testing of Devices 1 and 2 was performed. The data from this testing was used for correlation of the FE model. The results of the DOE show that for prediction of steady−state thermal performance the HTC values dominate other factors. The correlation efforts focused on adjusting the HTCs to match the test results. Other factors (die thickness, silver−epoxy thickness, etc.) were set to nominal values and not varied.

Table 6. Summary of DOE #1

DOE #1	Range	Effect	% Effect
Die thickness (mils)	8−15	0.16	1.8
Die attach thick (mils)	.25−.60	0.32	3.6
% silver in die attach	60 − 80	0.06	0.7
% Solder void	0 − 25	0.12	1.3
Junction depth	top − bot	0.11	1.2
HTC from nominal	±20 %	8.19	91.4

Table 7. Summary of DOE #2, with HTC held constant

DOE #2	Range	Effect	% Effect
Die thickness (mils)	8−15	0.34	35.4
Die attach thick (mils)	.25−.60	0.24	25.0
% silver in die attach	60 − 80	0.05	5.2
% Solder void	0 − 25	0.15	15.6
Junction depth	top − bot	0.18	18.8

Using the procedure outlined in Appendix A convective HTCs were calculated for Devices 1 and 2. These calculated values provided a good starting point, but required adjustment in order to obtain agreement between analysis and test. This is a normal practice in modeling to calibrate the work. The adjustment involved simply multiplying the calculated HTCs by a constant pre−factor. The value of the pre−factor was determined by running several steady−state thermal solutions for each configuration. Good correlation was achieved for a pre−factor of 1.2.

The results of the transient thermal analyses are compared to the test data Figures 11 and 12. Plots of R_{thja} vs. Time for both Devices 1 and 2 are presented. Examination of the plots shows very good correlation for time greater than 500 seconds. For time less than 500 seconds, the analysis consistently under predicts the R_{thja} of the parts. An explanation for this is that the overall package R_{thja} can be considered a combination of junction−to−case and case−to−ambient thermal resistances. The correlation technique used here has concentrated on the case−to−ambient heat transfer aspects of the package which, as the DOE showed, dominate the steady−state thermal behavior of these parts. For short times, before the package has experienced much heating, case−to−ambient convective heat transfer plays a smaller role and other parameters, such as the thermal conductivities and enthalpies of the materials used in the package, have a greater influence. A more complete assessment of the important factors in the short time portion of a thermal transient could be obtained by performing a DOE using transient (rather than steady−state) thermal analysis. Such an exercise would require a substantial amount of computation time and is an issue the authors hope to address in the future.

A final note concerning Figures 11 and 12, the analysis curves are based on R_{thja}'s determined using the die average, not maximum, temperature at each time point for T. The authors feel that using the die average temperature more closely matches what is actually measured using the heating−curve test technique described earlier in this paper.

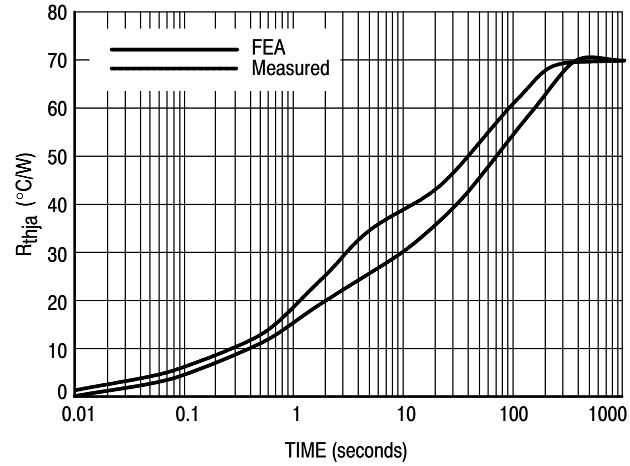


Figure 25. Measured and Modeled R_{thja} for Device 1

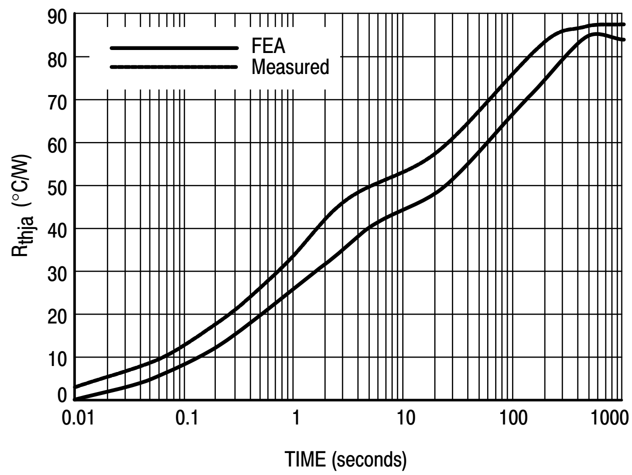


Figure 26. Measured and Modeled R_{thja} for Device 2

D. Device 3 Thermal Performance Prediction

The purpose of the analysis presented to this point has been to determine the proper boundary conditions for our thermal test configuration. The next step was to use that information to verify the capability of the model to predict the thermal performance of a previously untested device.

The results of the thermal FEA of Device 3 are shown in Figure 13. The data labeled “FEA” was generated using convective HTCs calculated with the procedure in Appendix A and a pre−factor of 1.2 as in the previous analyses. It is known from previous efforts that the “FEA” curve probably correlates only for times greater than 500 seconds. It was seen for Devices 1 and 2 that for times less than 500 seconds the analysis consistently under states the R_{thja}. The “Estimate” curve in Figure 13 was generated by assuming for Device 3 the same average percentage difference between measurement and test as observed in Devices 1 and 2.

After completing the above analysis and arriving at an estimate of the transient thermal performance of Device 3, this configuration was built and tested. The data from this testing is labeled “Measured” in Figure 13. The measured data matches the estimated very well across the entire transient, with a maximum deviation of approximately 10% in the 10 to 20 second range.

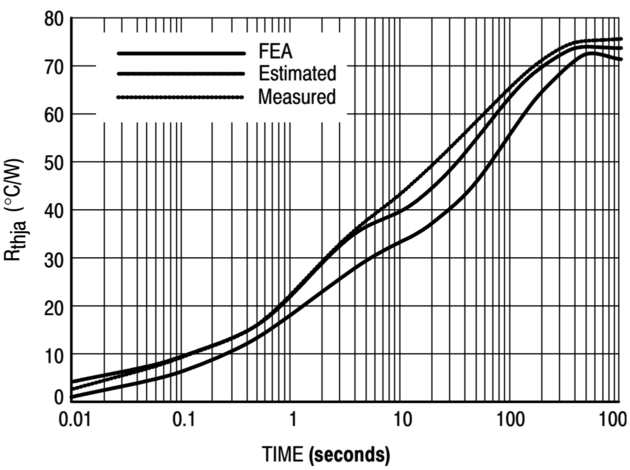


Figure 27. Predicted and Measured R_{thja} for Device 3

CONCLUSIONS

The original intent of this work was to match the modeled predictions with measured thermal data. This was accomplished with a two−phase DOE. During the process, several factors were discovered:

- In predicting steady−state R_{thja} for lead−mounted devices, HTC dominates. Package design and assembly parameters are insignificant.
- Test configuration has a large influence on the measured Rthja, which, for power devices, is quite a paradigm shift from the typical R_{thjc} measurements. In the modeling realm, it is critical to use the exact configuration or R_{thja} can be completely in error.
- Models of this type must be correlated and calibrated to measured values. Otherwise, significant prediction errors may occur.
- Infrared measurements are an excellent way to verify measured and modeled values of R_{thja}.
- Determining HTC for free convection is very complex and critical to model construction. The accuracy of the FEA thermal predictions depends on correct HTC values.

One practical result of this work is that it allowed ON Semiconductor to re−specify the power and drain current capability of ON Semiconductor’s MiniMOS™ (SO−8 MOSFET) portfolio to match or exceed competitors’ claims. This directly resulted in increased sales and allows ON Semiconductor to be considered for design into sockets that were previously unavailable because of inequitable specifications.

REFERENCES

[1] EIA/JEDEC STANDARD, EIA/JESD51, “Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device),” Dec 95.

[2] SEMI Test Method #G38−87, “Still and Forced Air Junction−to−Ambient Thermal Resistance Measurement of Integrated Circuits Packages”, 1993.

[3] NIST Special Publication 400−86, “Semiconductor Measurement Technology: Thermal Resistance Measurements,” July 1990.

[4] Zahn, B., Stout, R., and Billings, D., 1996, “A Thermal Comparative Study of Ceramic Dual In−Line Pressed Microelectronics Package Using Both Computational Fluid Dynamics and Solid Modeling Techniques on the ANSYS Finite Element Analysis System”, *Proc. of the 1996 Winter Motorola AMT Symposium*, pp.1063−1070.

[5] Chambers, B., and Lee, T.Y. Tom, 1995, “A Numerical Study of Local and Average Natural Convection Nusselt Numbers for Simultaneous Convection Above and Below a Uniformly Heated Horizontal Thin Plate,” *Proc. of the 1995 Summer Motorola AMT Symposium*, pp. 579−585.

[6] Montgomery, Douglas C., DESIGN AND ANALYSIS OF EXPERIMENTS, John Wiley & Sons 1991.

Trademarks:

ACKNOWLEDGMENTS

Special THANKS to Bob Buhrman, Ed Clemente, and Tanya Fowler for their support.

APPENDIX A:
Calculation of HTC for Natural Convection to Air

A. Introduction:

As shown in the body of this report, for the devices tested, accurate determination of HTCs is of primary importance to achieve good agreement between FEA and measurements. This is because the primary heat transfer mechanism to the outside environment is convection.

B. Procedure for HTC Calculation:

The authors used an approach outlined by Zahn, Stout, and Billings [4]. In their paper, a procedure for determining HTCs for natural convection from parts mounted on horizontal test boards is defined. The work of Zahn et al. relies heavily on the results of a previous study by Chambers and Lee [5]. The approach here is to use their method to calculate separate HTCs for the top of the SO−8 package, the surface of the copper cladding, the remaining top surface of the test board, and the entire bottom surface of the test board.

This is, perhaps, beyond how Zahn, et al. intended their method be used. The intent here is not to claim that the use of this method is scientifically rigorous, but instead to use it in the hopes that it will give a good starting point for achieving correlation with data measured in the lab.

Equations 10 and 11 of Zahn, et al. states for horizontal flat plates,

$$\bar{h}_{pup} = 0.653k^{0.857}\left(\frac{g\beta}{v^2}\mathrm{Pr}\right)^{0.143}\left(\frac{q}{P^{0.428}}\right)^{0.143} = z_{up}\left(\frac{q}{P^{0.428}}\right)^{0.143} \quad \text{(A1)}$$

and,

$$\bar{h}_{pup} = 0.979k^{0.863}\left(\frac{g\beta}{v^2}\mathrm{Pr}\right)^{0.137}\left(\frac{q}{P^{0.452}}\right)^{0.137} = z_{dn}\left(\frac{q}{P^{0.452}}\right)^{0.137} \quad \text{(A2)}$$

Where $\bar{h}_{pup}$ and $\bar{h}_{pdn}$ are uniform heat transfer coefficients on upward and downward facing horizontal surfaces in units of W/(m$^{2}\cdot$°C). The other parameters are defined as follows:

- k = conductivity of air
- g = acceleration of gravity
- β = volumetric thermal expansion coefficient of air
- v = kinematic viscosity of air
- Pr = Prandtl number for air
- z = composite parameter
- q = heat generation rate per unit area
- P = characteristic length defined as plate area divided by perimeter

The maximum steady−state junction temperature for the devices considered here is 150°C, so we used properties for air at 150°C to calculate z_{up} and z_{dn} for our case. The values used, and the resulting z_{up} and z_{dn} are as follows:

- k = 0.03536 W/m·°C
- g = 9.81 m/sec^2
- β = 1/423K = 0.002364 K^{-1}
- v = 2.88e^{-5} m^2/sec
- Pr = 0.686

Resulting in:

z_{up} = 0.41 and z_{dn} = 0.54

Thus Equations 1 and 2 above are reduced to:

$$\bar{h}_{pup} = 0.41\left(\frac{q}{P^{0.428}}\right)^{0.143} \quad \text{(A3)}$$

and,

$$\bar{h}_{pdn} = 0.54\left(\frac{q}{P^{0.452}}\right)^{0.137} \quad \text{(A4)}$$

For the ANSYS solutions, Equation A3 was used to calculate HTCs for the upper surface of the SO−8 package, the surface of the copper cladding, and the upper surface of the test board. Equation A4 was used to calculate a uniform HTC for the lower surface of the test board. Determination of the values of P for each of the four HTCs calculated is straightforward − divide the region area (m^2) by the perimeter (m) to determine a value for P in meters. Selecting the values of q to use for each surface is not so simple. The authors chose a scheme in which the total power applied to the package is divided among the four surfaces as follows: 10% through the package top, 40% from the surface of the copper cladding, 10% from the remainder of the test board upper surface, and 40% from the bottom of the test board. This seemed reasonable as the area of the package top surface is only 2.5% of the area of the copper cladding thus more of the total power will go through the cladding than the package top, even though the package top reaches a higher temperature.

The HTCs determined for the three SO−8 configurations are summarized in Table A1. Note that the only reason for the differences in HTCs between configurations is that the total power is different. Also note that the best correlation between model and test was achieved by increasing the HTC values listed in Table A1 by a factor of 1.2. Each configuration requires measurement calibration to determine an accurate HTC correction factor.

Surface	Width (m)	Length (m)	Area (m^2)	Perimeter (m)	P (m)	q (% of Total Power)
Package Top	0.00338	0.00475	1.61E−05	0.01626	9.87E−04	10
Copper Cladding	0.0254	0.0254	6.45E−04	0.1016	6.35E−03	40
FR4 Board Top	0.0508	0.0508	1.94E−03	0.2032	9.53E−03	10
FR4 Board Bottom	0.0508	0.0508	2.58E−03	0.2032	1.27E−02	40

Table A1: Calculated HTC Values for Devices 1, 2 and 3

Calculated HTC Values					
Device	Total Power (Watts)	Package Top (W/m^2 C)	Copper Clad (W/m^2 C)	FR4 Top (W/m^2 C)	FR4 Bottom (W/m^2 C)
1	2	30.534	9.898	5.833	8.527
2	1.5	29.304	9.499	5.598	8.197
3	2.25	31.053	10.066	5.932	8.666

New Models and Techniques for Analyzing the Power Transistor and its Thermal Environment

By Kim Gauen
ON Semiconductor

INTRODUCTION

In many electronic systems, power transistors perform critical system functions. They also can account for a significant portion of the total system cost. Better performance can come at a higher price, but balancing this price/performance tradeoff has not been easy for designers. Thermal issues are involved, and the tools for analyzing the electrical/thermal environment have not been available. Recently, new tools have become available and techniques are now appearing for sophisticated analysis of the power transistor and its thermal environment.

This paper describes one set of tools and some techniques for thermal/electrical analysis. Because the power MOSFET is so popular, it is one of the first devices to be characterized for such evaluations and it is the focus of this paper.

Know Your Transistor's Operating Temperature

Probably the two most important parameters for keeping a power MOSFET within its safe operating area are its silicon temperature, often referred to as its "junction temperature (T_J)," and the voltages appearing across its terminals. Steady state current handling capability is certainly important, but it is usually bounded by the maximum rated junction temperature and not by effects such as wirebond limitations, metal migration of the source metal, or insufficient gate voltage.

There are several reasons why it is important to know a power MOSFET's junction temperature. First, junction temperature affects reliability. High temperature and the associated thermal cycling accelerate several failure mechanisms. Second, parameters that affect junction temperature also influence system cost. An overly conservative designer might use a power transistor that is unnecessarily large and expensive for the application. On the other hand, using a transistor that is undersized might result in the designer selecting a heat sink that is larger and more expensive than necessary. Third, knowing T_J will help the designer understand how the system will operate under various loading conditions and temperatures. MOSFET junction temperature affects its breakdown voltage, on−resistance, threshold voltage, switching speed, and transfer characteristics — all of which can cause changes in system level performance. For example, changing a MOSFET's switching speed is likely to affect the system's noise performance, and the MOSFET is certainly less efficient at higher temperatures due to a significant increase in $R_{DS(on)}$. With cost, system performance, and reliability at stake, the designer needs good tools for determining junction temperature and evaluating design tradeoffs.

Traditional Method of System Design

The traditional way to size a power transistor is to estimate the on−resistance requirements and the associated on−state losses and switching losses and then to estimate the size of the heat sink needed for the anticipated load currents and ambient temperature. The system is then assembled and tested and (sometimes) the transistor's case temperature is measured under "worst case" conditions. Heat sink or transistor size is then modified, and the system is retested and refined until the results are acceptable.

The limitations of this approach are well known. First, system complexity and lack of time often limit the engineer's ability to completely analyze the system prior to assembling hardware. Therefore, the first prototype is based on calculations, educated guesses, and intuition. Good analysis tools and techniques can produce a much better first pass implementation in hardware.

Second, determining "worst case" conditions might not be easy. For example, the highest junction temperature usually occurs at the maximum anticipated ambient temperature, but sometimes that is not the case. For some loads, currents are significantly higher at cold temperatures. If a large load such as a motor has a very long thermal time constant, the power transistor could see high currents for a long time relative to the thermal time constant of it and its heat sink. It would be helpful to have a method of quickly evaluating the effects of these and other changing conditions.

The third problem with the traditional approach is that it is cumbersome to evaluate system trade−offs with hardware. Heat sinks must be built and changed, the system must be tested under various conditions, loads must be built, ambient temperatures must be controlled, etc.

Other difficulties are related directly to analyzing the thermal system. The first problem is that junction temperature is not easy to measure. Using an infrared camera to view an unencapsulated die would be ideal, but few designers have this option.

More likely, a designer places a thermocouple on the heat sink next to the MOSFET or directly on the MOSFET's tab. But under transient conditions or at high power, these measurements are probably at least several degrees lower than the actual junction temperature.

The most accurate way to monitor the junction temperature of a plastic encapsulated MOSFET is to use one of its temperature sensitive parameters, or TSPs. The MOSFET's TSPs are its on−resistance, the forward voltage drop of its body diode, its threshold voltage, and its breakdown voltage. All four require that each test device be calibrated over temperature, which is time consuming. The first two TSPs are the ones most commonly used.

In circuits where the MOSFET is on continuously, using $R_{DS(on)}$ as the TSP works fairly well. A low voltage MOSFET, however, may give a signal that is too low for accurate measurement. Therefore, this method works best for high on−resistance (high voltage) devices. Monitoring the forward voltage drop of the body diode gives very good results, but it is difficult to build the circuitry that interrupts the normal drain to source load current and forces a small source to drain sense current in the body diode. The technique of using the body diode is discussed in detail in References [1] and [2].

Even if the system is characterized perfectly, there are remaining roadblocks to accurately predicting junction temperature. Power waveforms are often complex, making analysis very difficult. The graphical methods described in Reference [3] can help, but they are unwieldy with complex waveforms. Next, there is the issue of how to monitor junction temperature to verify simulation results. Finally, it is important to provide power inputs to the thermal network and thermal inputs to the electrical system. Until recently, the only way to provide thermal feedback was to do it iteratively with successive simulation runs, one for each new junction temperature estimate. That approach suffices for steady state conditions, but it is not accurate for transient analysis since it cannot track junction temperature variations throughout the simulation.

Requirements for Accurate Models

To accurately model the electrical/thermal system a designer needs:

1. an accurate model of the MOSFET that is temperature dependent
2. a model of the MOSFET that supports passing information between the electrical and thermal environments during the simulation (these models are "dynamically" temperature dependent)
3. an accurate model of the MOSFET's thermal environment
4. tools that support the above models for easy simulation and analysis

Each of the above requirements can now be met, and the pieces have been assembled into a very effective analysis tool.

The first requirement is an accurate and robust model of the power MOSFET that is also temperature dependent. This model should accurately predict the I−V characteristics for the forward range of operation, as well as leakage, reverse recovery and breakdown characteristics of the drain−source body diode. The electrical model must also describe the nonlinear gate drain (and gate source for negative V_{GS}) capacitances that are key to accurate transient simulations.

In the language of simulation a "robust" model is one that does not cause convergence problems, which are most commonly the result of discontinuities in the model. Many SPICE based subcircuit models have been introduced over the years in an attempt to describe the non linear power MOSFET capacitances; however, the macro modeling approach introduces discontinuities. Although such discontinuities may be acceptable in a purely electrical simulation environment, the complexity of the dynamic electro−thermal system requires models with superior convergence qualities.

So far, the model we have discussed is a "static" thermal model. This means that the designer can assign any reasonable temperature to the model prior to simulation. However, device temperature will remain constant throughout the simulation, regardless of power dissipation. Instead of this static model, we require a "dynamic" thermal model that allows the device temperature to change as electrical energy is converted to heat, as it does in a real device. To accomplish this, the temperature parameter, used inside the MOSFET model to adjust the electrical parameters for thermal effects, must now become an independent variable solved by the simulator. When temperature is an independent variable, the simulator must solve a set of simultaneous nonlinear differential equations for temperature and heat flow as well as for voltage and current for each node and each time step.

The third requirement, having accurate models of the thermal environment, is a bit tricky to meet because there is no standard methodology for obtaining such models. The system designer has difficulty obtaining thermal models of heat sinks and extracting thermal models of the MOSFET from the information provided on the MOSFET data sheets. Neither the power transistor user nor the semiconductor manufacturer has a very good handle on characterizing the thermal interface between the case and the heat sink. However, techniques are available to get such models. The best technique depends on the pulse width of interest.

Transient thermal response curves for power transistors have been around for a couple of decades. A curve like the one shown in Figure 28 is generated by observing the response of the transistor's junction temperature to a step function of power dissipation. One can develop a thermal R−C network from a transient thermal response curve.

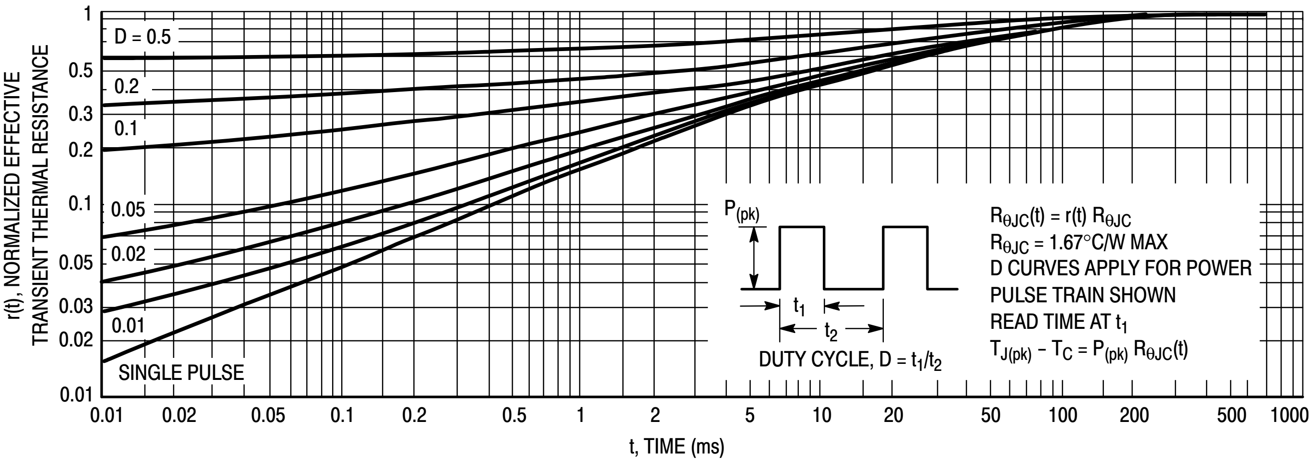


Figure 28. It is possible to generate thermal models from transient thermal response curves such as this one for a 4 A, 500 V MOSFET in a TO−220 package.

These curves are perfectly adequate for analysis — if the power transistor's case temperature is known and the power dissipation waveform is relatively simple. The accepted definition of "case temperature" is the temperature of the hottest part of the transistor's tab, which is the spot on the tab just behind the power transistor die, as shown in Figure 29. Unfortunately, monitoring this temperature is not easy and a tab or heat sink temperature is often measured instead. So, the situation that is easiest to analyze is one where the case temperature doesn't change, as would happen under brief transient conditions or when the tab is attached to a known and constant temperature — an "infinite heat sink."

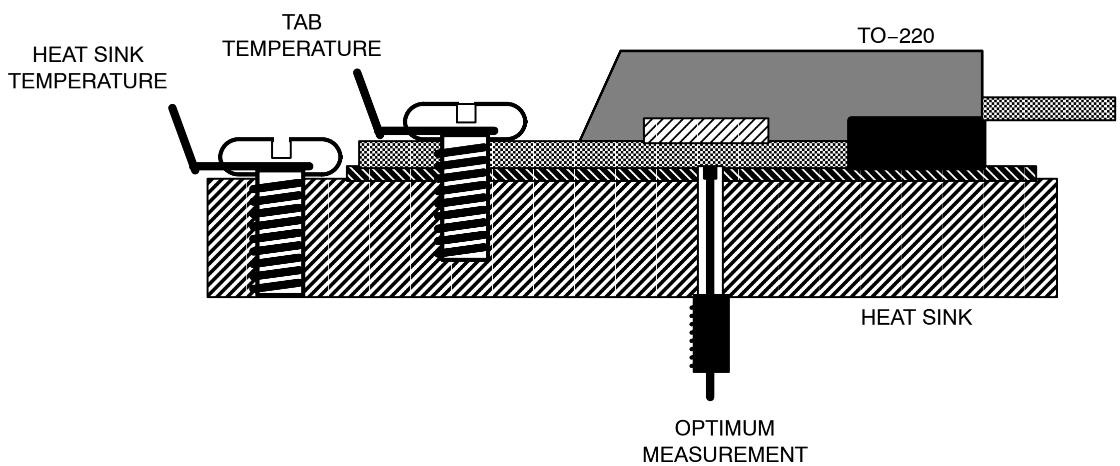


Figure 29. The standard way to measure the heat sink of a power transistor is to place a thermocouple through the heat sink and against the back of the transistor's tab, just opposite the center of the die.

Steady state conditions are also fairly easy to characterize and then model. One could characterize the system's thermal resistances (junction to tab, tab to heat sink, heat sink to ambient), put the steady state models into the simulator, and again the modeling should go smoothly. But for many cases, i.e., for power pulses more than a few milliseconds yet not DC, an approach that defines the entire thermal system is needed.

An effective method is to treat the power transistor and its heat sink as a unit and characterize the assembly just as one would characterize a power transistor — in effect, developing a transient thermal response curve for the entire thermal system. This method inherently addresses the thorny problem of trying to define the thermal interface if the power transistor and the heat sink are characterized separately. The interface is simply one part of the network, and the empirical tests automatically include its effects. The last circuit example in this paper shows how to use this technique.

The fourth and final requirement is for a simulator that can support thermal as well as electrical models, allowing the electrical system to affect the thermal and visa versa. In system simulators such as SPICE the system variables are constrained to voltage and current. In order to simulate non−electrical systems in these types of simulators, the non electrical system must be written in terms of equivalent electrical elements, or macro−models. Macro modeling techniques of electro−thermal systems suffer from their inability to directly adjust the internal electrical model parameters for the non−electrical changes in the system. To circumvent this limitation, the user is forced to make gross adjustments to the external nodes of the circuit through controlled sources or other elements.

Simulators such as Analogy's SABER provide a modeling language which separates the simulation "engine" from the models. (Analogy's hardware description language is MASTTM.) This allows the user to develop models as a system of through and across variables that are not constrained to voltage and current. Thus, the relationship between electrical and thermal energy can be described directly in the model. The SABER simulator uses a dynamic thermal version of the MPV3 MOSFET model (MPV3X), which is the basis of the library of ON Semiconductor MOSFET models provided with the 4.0 release of SABER.

A Simple Example

A simple example illustrates the basic modeling concepts and some of the analysis possibilities. Assume that the desired load current conducted by a pair of MTP75N05HDs is 35 A and that the load current lasts for an indefinite time. Also assume that the heat sink is a 40 mm by 20 mm by 12 mm piece of aluminum with no fins. Such a heat sink has a large thermal capacity and low cost, but poor thermal resistance. So, the question might be, "In a 25°C environment, how hot do the power transistors get and how long does it take to reach steady state conditions?" Without good evaluation tools or actual hardware, it is difficult to tell if the transistors will slip into a thermal runaway condition.

The first step is to characterize the heat sink. A single MOSFET was mounted to the heat sink and was controlled to step its power dissipation from 0 to a constant and continuous 7.87 W. The MOSFET's tab was monitored until the system became stable. From the power dissipation and the difference between the tab and ambient temperatures, the thermal resistance is easily calculated. For this heat sink in a 30°C environment:

Ttab−Tamb = P_D * Rth_hs

152°C− 30°C = 7.87 * Rth_hs

Therefore, Rth_hs = 15.5°C/W

Like all others, this heat sink consists of a network of distributed thermal resistances and capacitances. The construction and complexity of a heat sink determines how to select the lumped elements that model its thermal network. In cases like this, a single thermal resistance and capacitance model the heat sink well enough for purposes here.

With the assumption that a single R−C network is adequate, the task is now to determine the heat sink's thermal capacitance. Figure 30 shows how the transistor's tab temperature varies with time, and the data suggest a tau of about 420 seconds. That sets the thermal capacitance to 27 J/°C. Simulating with an Rth_hs of 15.5°C/W, a Cth of 27 J/°C and a power dissipation of 7.87 W yields a response that is within measurement error of the actual system response. This system is relatively easy to model since the power dissipation in the MOSFET is held constant by gate drive circuitry and the thermal network is quite simple.

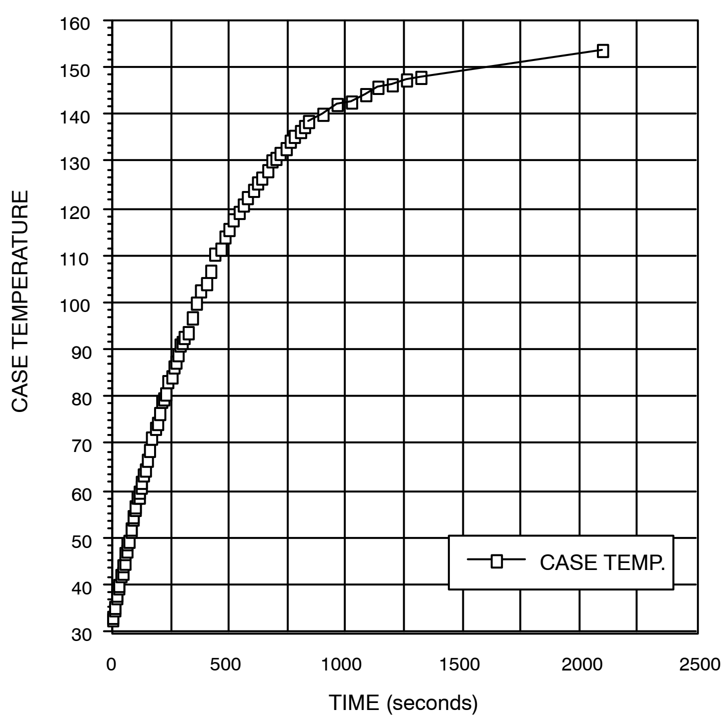


Figure 30. Thermal response of 40 x 20 x 12 mm Al heat sink

A more difficult test of the models and the simulation methodology is to revisit the conditions and requirements of the initial application. In this case, two MOSFETs were mounted to the same heat sink and they were forced to conduct 17.5 A continuously at an ambient and initial heatsink temperatures of 20.7°C. The added difficulty of this simulation is that the power dissipation of the MOSFET causes the heat sink and junction temperatures to increase, which increases on−resistance and further increases power dissipation. The change in $R_{DS(on)}$ cannot be ignored because it increases by about 70% for a 100°C rise in junction temperature. The first simulation was simpler because the power dissipation was held constant since the MOSFET was forced by gate drive circuitry to operate as a constant current source.

The results of the simulated $V_{DS(on)}$ and the actual tab temperature data are shown in Figure 31. Again, the empirical and simulated curves are the same within a couple of degrees and about 10 mV. For this example, the tab temperature is very close to the junction temperature since the MOSFET's power dissipation is less than 3.5 W. The results track nicely only because SABER's MOSFET model is dynamically temperature dependent. The model correctly predicted the final junction temperature and that the system would not go into thermal runaway. Additionally, the MOSFET's $V_{DS(on)}$ in simulation matched the empirical results even as junction temperature changed, further validating the model.

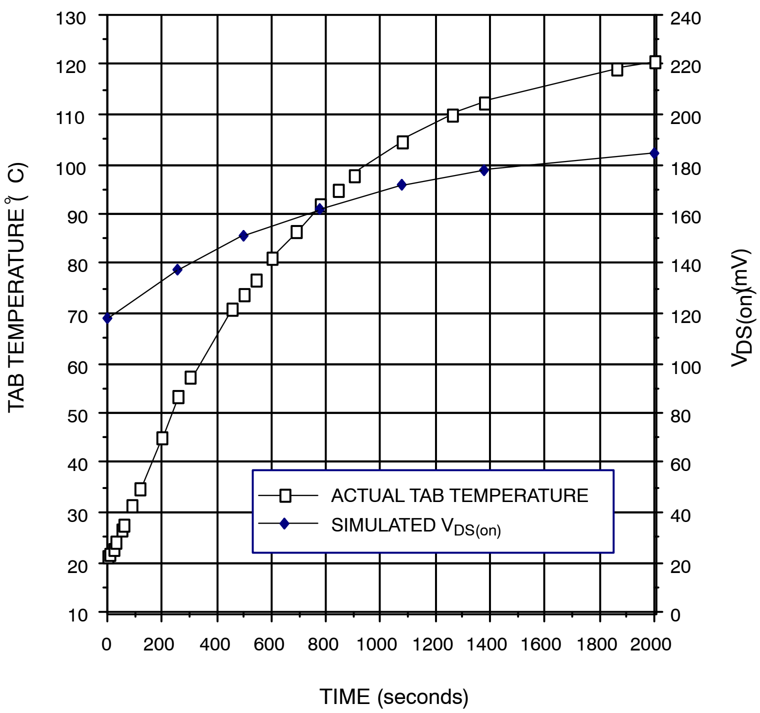


Figure 31. One of two MTP75N06HDs conducting a total continuous current of 35 A. Simulation results closely matched empirical results.

A More Complex Example

The above example validates the general concept for a relatively simple circuit. Adding pulse width modulation to the circuit further illustrates the technique's strengths, but it also uncovers some limitations. This final example also validates the technique of developing and using a transient thermal response curve for a MOSFET attached to a heat sink.

Like the other examples, the first step in this analysis is to determine the system's thermal model. But this time we are interested in the system's thermal response to very narrow power pulses that occur during switching transitions as well as the comparatively very long response of the heat sink. In fact, we are interested in responses to pulse widths varying about nine orders of magnitude; so it's likely that there are new measurement challenges.

Until recently, thermal response test equipment had maximum pulse width capability of at most a few seconds. The advent of surface mount power devices and the much longer thermal response time of the transistor/circuit board combination bought about the need for equipment that can apply a power pulse and measure the response for several minutes. One vendor of this new equipment is Analysis Tech, and their Phase 9 automatic transient thermal response tester was used in this study.

The Analysis Tech Phase 9 can be used to measure the thermal response of the system of interest here, i.e., a power transistor mounted to moderate size heat sink. For this exercise an MTP15N06V (a 15 A, 60 V MOSFET) was mounted to a Wakefield 667−10ABPP heat sink. The Wakefield heat sink is finned and is 1″ tall, 1.35″ wide, and 0.5″ deep.

For MOSFET data sheet characterization, the transient thermal response is normally taken with the device mounted to an infinite (water cooled) heat sink. The infinite heat sink fixes the MOSFET's case temperature to a known value which serves as the reference temperature for the characterization. Instead of a water cooled heat sink, the Wakefield heat sink was used, and the reference temperature was the ambient temperature.

The thermal response of the MOSFET on the water cooled heat sink and the response on the Wakefield 667−10ABPP heat sink are shown in Figure 32. Note that at narrow pulse widths the two curves are very similar, as there is insufficient time to transfer enough power into the heat sink to raise its temperature. At about 0.3 seconds, the two curves begin to diverge as the temperature of the Wakefield heat sink begins to rise while the water cooled heat sink maintains a steady case temperature.

RC networks for both thermal circuits are included in Figure 32. They were automatically generated by the Analysis Tech Phase 9. Off the shelf programs such as Sauna™ can extract the thermal Rs and Cs from transient thermal response curves. The dashed lines, which are for the most part hidden by the empirical data points, indicate the response of the suggested RC equivalent networks.

Note that the final data point is taken around 600 s, before the MOSFET/Wakefield heat sink system is completely stable. At the time of the test this was thought to be the pulse width limitation of the tester. (The actual limitation is 10,000 seconds.) An alternate test using simple equipment that is only good for steady state produced a reading of 18.1°C/W for the total thermal resistance from junction to ambient. Therefore, in the final model of the MOSFET/ Wakefield heat sink, Rth_3 was changed from 11.44 to 15.66°C/W. (The Wakefield 667−10ABPP is specified to be 12.66°C/W in still air at 6 W.)

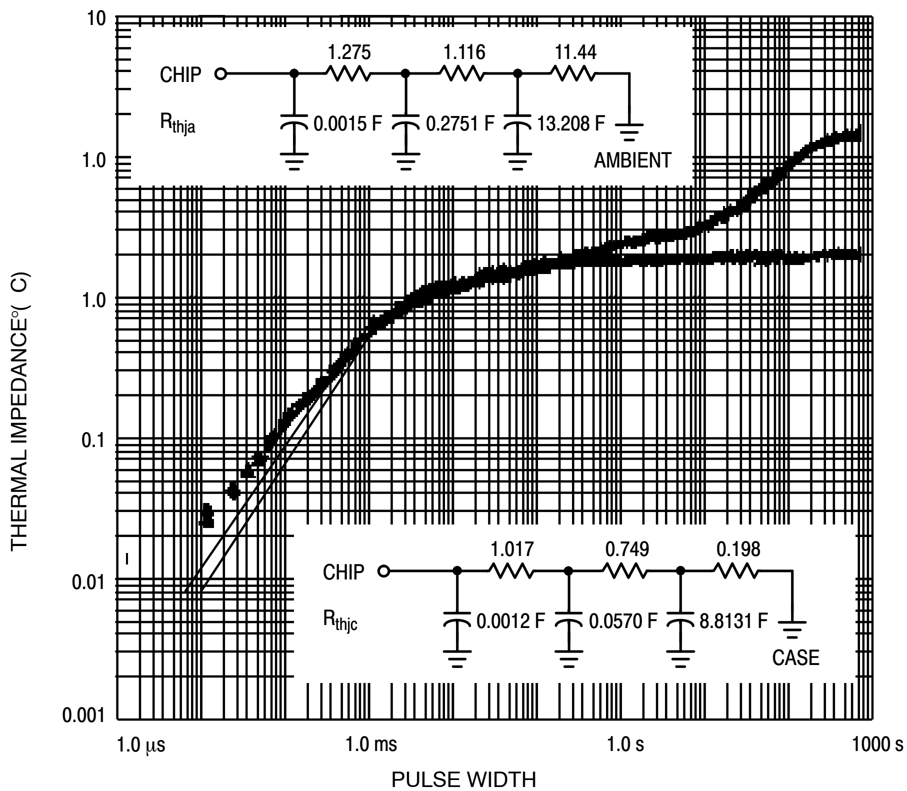


Figure 32. Thermal response of the MOSFET on a water cooled heatsink and on a Wakefield heatsink.

Figure 33 shows the entire thermal/electrical system. The MOSFET's gate was driven by a 10 V, 100 Hz, 50% duty cycle voltage source. A brute force attempt at simulating hundreds of seconds of operation unveils a limitation of the tools and this methodology. The simulation proceeds rapidly as long as the MOSFET is on or off, but during switching, the simulator slows down to accurately model the transitions. Even though the circuit is very simple and the switching frequency is low by most standards, it took several minutes on an HP 9000 Model 735 to simulate each second of operation. To get useful data without excessive simulation times, the simulation was conducted in two runs, one to obtain the circuit's response during the first fourteen seconds and the other to determine its steady state response.

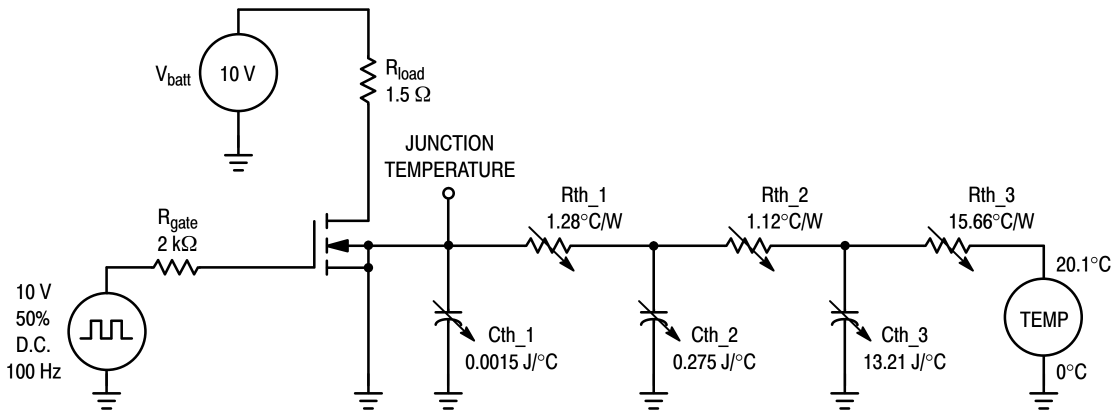


Figure 33. Schematic of electrical/thermal system. The values of the discrete thermal Rs and Cs shown are chosen to give a response most similar to that of the system's distributed elements.

Figure 34 shows the junction temperature variation during the first 1.1 s of operation. Two features are clear: the junction temperature swings about five degrees each period and the average temperature within a cycle begins to increase more slowly at around 300 ms as the heat sink's large thermal capacitance comes into play. The junction temperature during the first 14 seconds of simulation is shown in Figure 35. The junction temperature swing within a cycle, the rise in the average temperature during the first second, and the gradual rise thereafter are controlled by the three thermal capacitances.

Figure 36 shows the temperature appearing at Cth_2 and Cth_3. This graph clearly illustrates the initial charging of the heat sink's large thermal capacity. It also shows that temperature ripple on Cth_2 is in the 0.1°C range and that there is essentially no ripple on Cth_3. Heat flow from the heat sink and into the environment is shown in Figure 37. As would be excepted, no heat flows initially and heat flow steadily increases as the heat sink's temperature rises.

A test lasting 14 seconds lends itself to methods of verification. A thermocouple placed on the MOSFET's tab read 25.0°C at 14 seconds. The model's discrete thermal capacitances and resistances are chosen to provide a response similar to the actual response of the distributed Rs and Cs of the heat sink. They do not represent physically discrete capacitances associated with specific elements of the circuit. Therefore, the tab temperature should not be expected to be equal to the temperature appearing at any of the three thermal capacitances. However, the change in the tab temperature can be tracked, and it should follow the temperature rise of the body of the MOSFET and the heat sink. That indeed proves to be the case, because between 5 and 14 seconds the simulated tab temperature increases at the same rate as the temperature of Cth_2 and Cth_3.

A second simulation and an alternate method is needed to get results at steady state without very long simulation times. The trick is to decrease the size of the thermal capacitances so that they are more easily charged to their final temperatures. Keeping some thermal capacity in the system keeps the junction temperature from swinging wildly with variations in power dissipation. Without any capacitance, variations in power dissipation generate unrealistically large swings about the steady state value. These swings might be high enough to cause problems in the simulation. The waveforms in Figure 38 represent the system's performance with Cth_2 set to 0.03°J/C and Cth_3 set to zero. The steady state value of the empirical test was 63.4 degrees, which matches very well with the simulation.

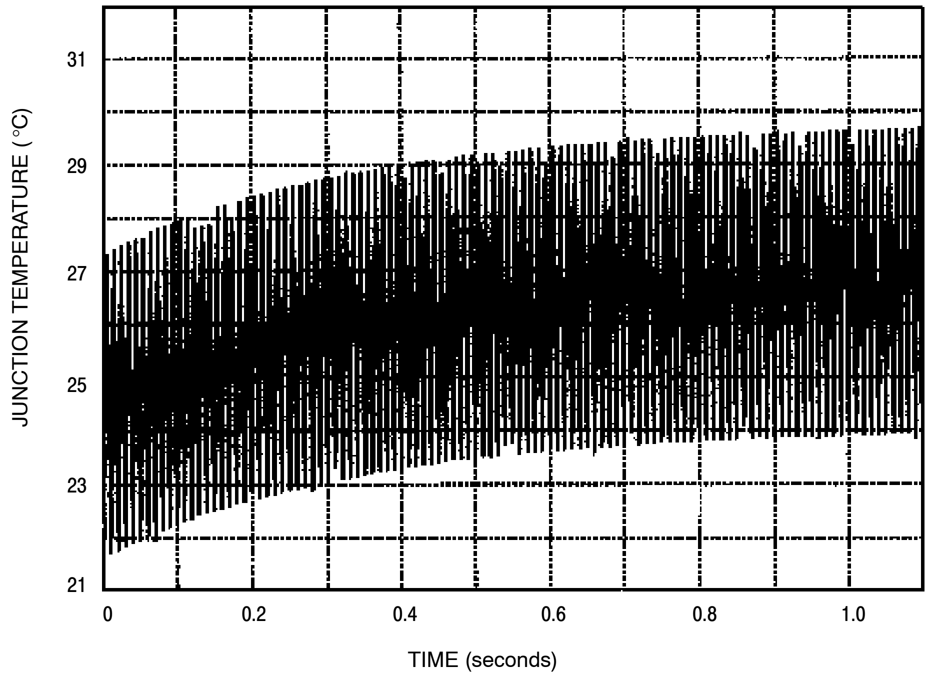


Figure 34. Junction temperature during the first 1.1 seconds of operation

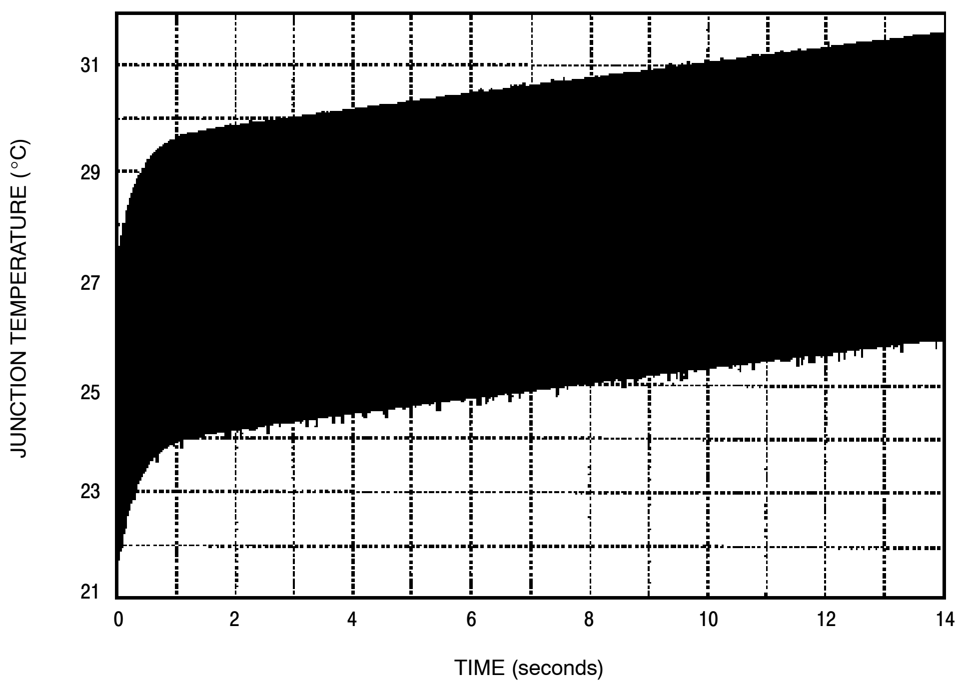


Figure 35. Junction temperature during the first 14 seconds of operation

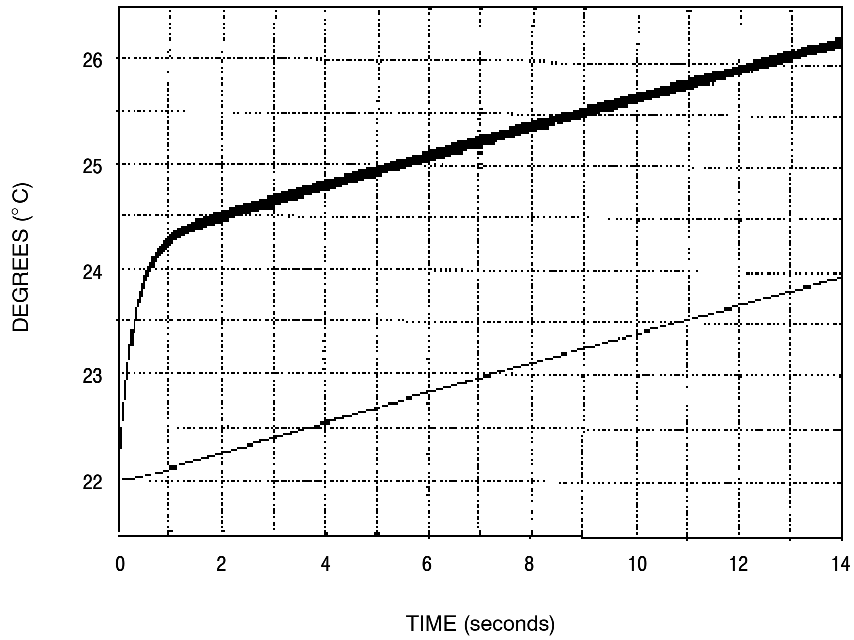


Figure 36. Temperature rise at Cth_2 and Cth_3 clearly show the different thermal time constants that make up the thermal response

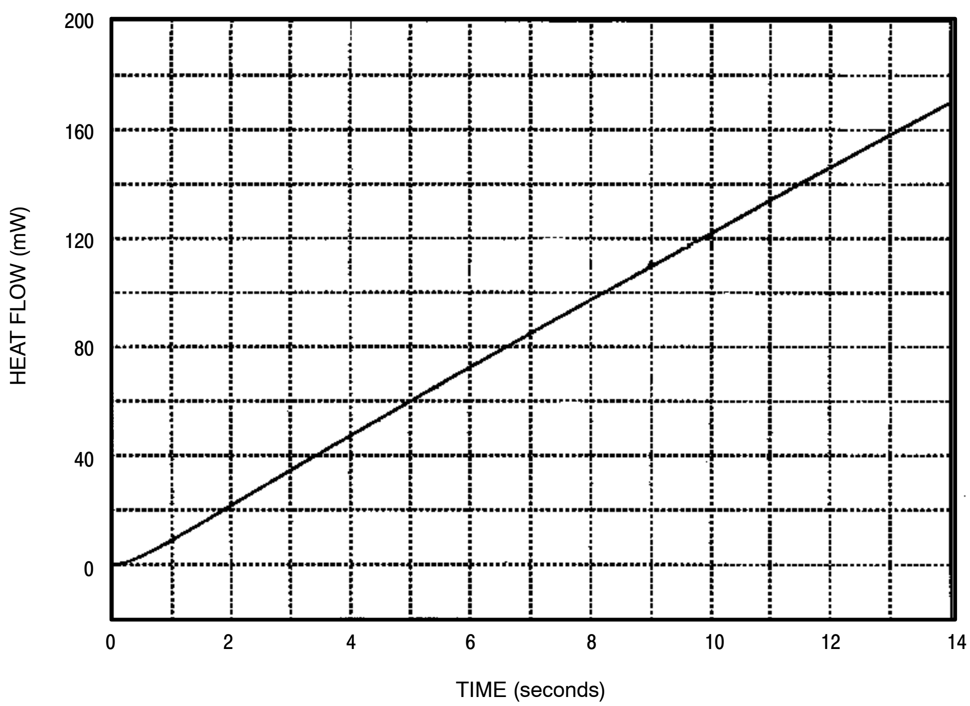


Figure 37. Simulation shows that little heat flows into the environment during the first 14 seconds of operation.

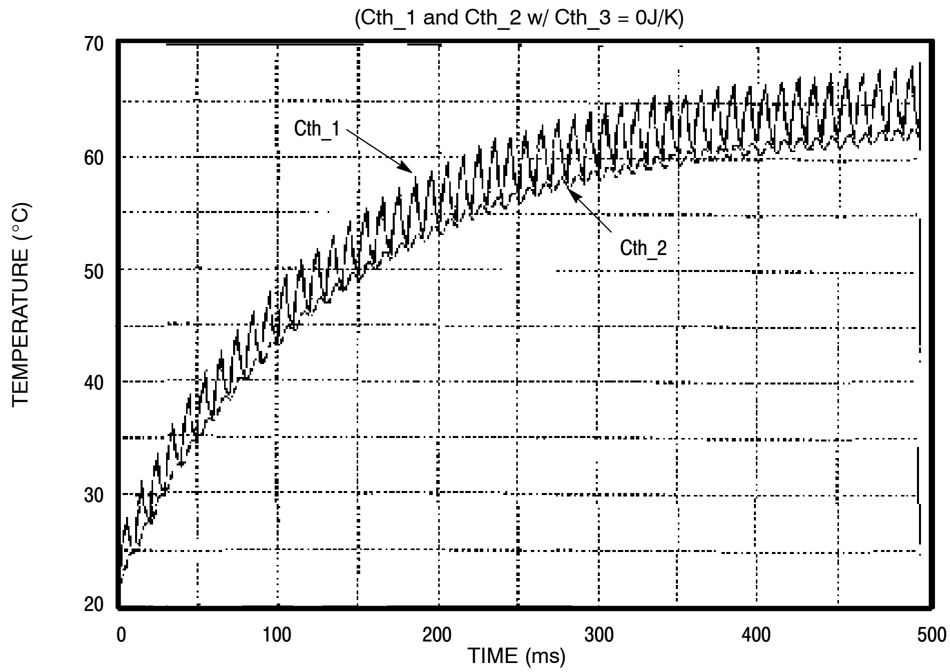


Figure 38. Dramatically reducing the size of the largest thermal capacitances allows the simulator to quickly find solutions for steady state conditions.

Other Tips

When using Analogy's SABER program, it is good to know how the program assigns default values of thermal resistance. The program looks to see if the user specifies Rth_hs or Rth_jc. If the user defines Rth_hs, SABER uses that value and the value of Rth_jc specified on the manufacturer's data sheet. If Rth_hs is not specified, SABER uses the value of Rth_ja specified on the manufacturer's data sheet in place of Rth_jc and Rth_hs. Rth_ja is the device's junction to ambient thermal resistance without a heat sink, and its value for a TO−220, for example, is quite large, 62.5°C/W. Defaulting to such a large thermal resistance might cause unrealistic junction temperatures and invalid results or even convergence problems.

In release 4.0 of SABER, Analogy's thermal models do not contain thermal capacitance. To add your own thermal network, including thermal capacitance, set the MOSFET's Rth_hs and Rth_jc to very small values (0.001 °C/W was used in these simulations) and then add your own thermal network, including thermal capacitances and thermal resistances.

SUMMARY

The tools and techniques described here proved to be an effective means of predicting power transistor junction temperature of two different MOSFETs operating in three types of circuits with two different heat sinks. This methodology is also useful for understanding how circuit performance varies with changes in the power transistor, the thermal interface between it and the heat sink, and the heatsink itself. The uniqueness of the approach is the use of a combination of newly developed tools, all of which are readily available to the power electronics community.

ACKNOWLEDGMENTS

Special thanks to Gary Dashney, Tanya Fowler, and Larry Walker of ON Semiconductor for developing the technique of measuring transient thermal response of systems with very long thermal response times and for characterizing the MOSFET/heatsink assembly used in this study.

REFERENCES

[1] G. Dashney, "Basic Semiconductor Thermal Measurement," ON Semiconductor (602−244 3471).

[2] A. Pshaenich, "Basic Thermal Management of Power Semiconductors," ON Semiconductor Application Note AN1083.

[3] Brice Shiner, Bill Roehr, "Transient Thermal Resistance — General Data and Its Use," ON Semiconductor Application Note AN569.

[4] A. Hefner, D Blackburn, "Thermal Component Models for Electrothermal Network Simulation," IEEE Transactions on Components, Packaging, and Manufacturing Technology — Part A, Vol. 17, No. 3, September 1994.

[5] "Modeling Thermal Networks in Electrical Circuits," Engineering Note No. 110, Analogy, Inc., Beaverton, OR.

[6] Dr. J. Sophia, "Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices," Analysis Tech, Wakefield, MA 01880.

Transient Thermal Resistance of Semiconductor Packages

Edited and Updated

USING TRANSIENT THERMAL RESISTANCE DATA IN HIGH POWER PULSED THYRISTOR APPLICATIONS

INTRODUCTION

For a certain amount of dc power dissipated in a semiconductor, the junction temperature reaches a value which is determined by the thermal conductivity from the junction (where the power is dissipated) to the air or heat sink. When the amount of heat generated in the junction equals the heat conducted away, a steady−state condition is reached and the junction temperature can be calculated by the simple equation:

$$T_J = P_D R_{\theta JR} + T_R \qquad (1a)$$

where T_J = junction temperature
T_R = temperature at reference point
P_D = power dissipated in the junction
$R_{\theta JR}$ = steady−state thermal resistance from junction to the temperature reference point.

Power ratings of semiconductors are based upon steady−state conditions, and are determined from equation (1a) under worst case conditions, i.e.:

$$P_{D(max)} = \frac{T_{J(max)} - T_R}{R_{\theta JR(max)}} \qquad (1b)$$

$T_{J(max)}$ is normally based upon results of an operating life test or serious degradation with temperature of an important device characteristic. T_R is usually taken as 25°C, and $R_{\theta JR}$ can be measured using various techniques. The reference point may be the semiconductor case, a lead, or the ambient air, whichever is most appropriate. Should the reference temperature in a given application exceed the reference temperature of the specification, P_D must be correspondingly reduced.

Thermal resistance allows the designer to determine power dissipation under steady state conditions. Steady state conditions between junction and case are generally achieved in one to ten seconds while minutes may be required for junction to ambient temperature to become stable. However, for pulses in the microsecond and millisecond region, the use of steady−state values will not yield true power capability because the thermal response of the system has not been taken into account.

Note, however, that semiconductors also have pulse power limitations which may be considerably lower − or even greater − than the allowable power as deduced from thermal response information. For transistors, the second breakdown portion of the pulsed safe operating area defines power limits while surge current or power ratings are given for diodes and thyristors. These additional ratings must be used in conjunction with the thermal response to determine power handling capability.

To account for thermal capacity, a time dependent factor r(t) is applied to the steady−state thermal resistance. Thermal resistance, at a given time, is called transient thermal resistance and is given by:

$$R_{\theta JR(t)} = r(t) \cdot R_{\theta JR} \qquad (2)$$

The mathematical expression for the transient thermal resistance has been determined to be extremely complex. The response is, therefore, plotted from empirical data. Curves, typical of the results obtained, are shown in Figure 1. These curves show the relative thermal response of the junction, referenced to the case, resulting from a step function change in power. Observe that the total percentage difference is about 10:1 in the short pulse ($\sqrt{t}$) region. However, the values of thermal resistance vary over 20:1.

Many ON Semiconductor data sheets have a graph similar to that of Figure 2. It shows not only the thermal response to a step change in power (the D = 0, or single pulse curve) but also has other curves which may be used to obtain an effective r(t) value for a train of repetitive pulses with different duty cycles. The mechanics of using the curves to find T_J at the end of the first pulse in the train, or to find $T_{J(pk)}$ once steady state conditions have been achieved, are quite simple and require no background in the subject. However, problems where the applied power pulses are either not identical in amplitude or width, or the duty cycle is not constant, require a more thorough understanding of the principles illustrated in the body of this report.

USE OF TRANSIENT THERMAL RESISTANCE DATA

Part of the problem in applying thermal response data stems from the fact that power pulses are seldom rectangular, therefore to use the r(t) curves, an equivalent rectangular model of the actual power pulse must be determined. Methods of doing this are described near the end of this note.

Before considering the subject matter in detail, an example will be given to show the use of the thermal response data sheet curves. Figure 2 is a representative graph which applies to a 2N5886 transistor.

Pulse power P_D = 50 Watts
Duration t = 5 milliseconds
Period τ_p = 20 milliseconds
Case temperature, T_C = 75°C
Junction to case thermal resistance, $R_{\theta JC}$ = 1.17°C/W

The temperature is desired, a) at the end of the first pulse b) at the end of a pulse under steady state conditions.

For part (a) use:

$$T_J = r(5\ ms)\ R_{\theta JC} P_D + T_C$$

The term r(5 ms) is read directly from the graph of Figure 2 using the D = 0 curve,

$$\therefore T_J = 0.49 \times 1.17 \times 50 + 75 = 28.5 + 75 = 103.5$$

The peak junction temperature rise under steady conditions is found by:

$$T_J = r(t, D)\ R_{\theta JC}\ P_D + T_C$$

$D = t/\tau_p = 5/20 - 0.25$. A curve for D= 0.25 is not on the graph; however, values for this duty cycle can be interpolated between the D = 0.2 and D = 0.5 curves. At 5 ms, read $r(t) \approx 0.59$.

$$T_J = 0.59 \times 1.17 \times 50 + 75 = 34.5 + 75 = 109.5°C$$

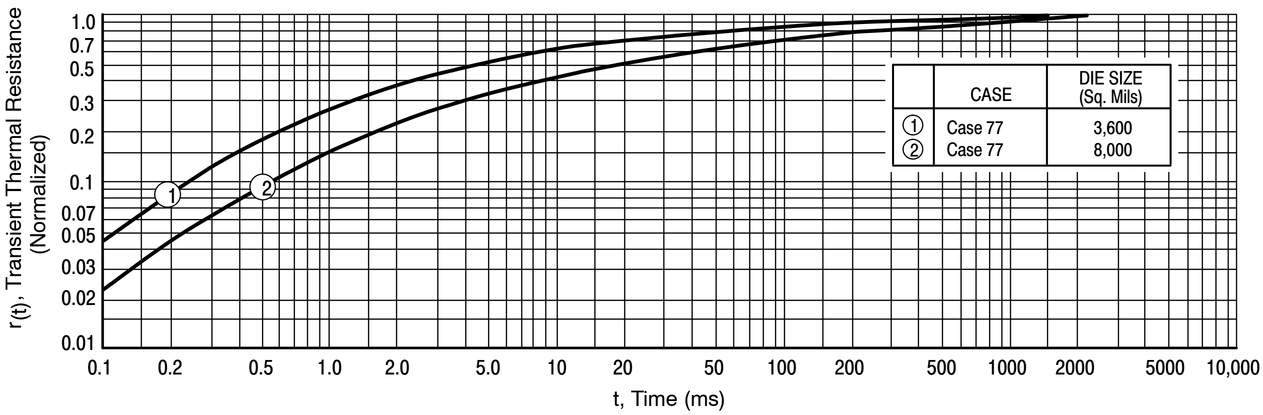


Figure 39. Thermal Response, Junction to Case, of Case 77 Types For a Step of Input Power

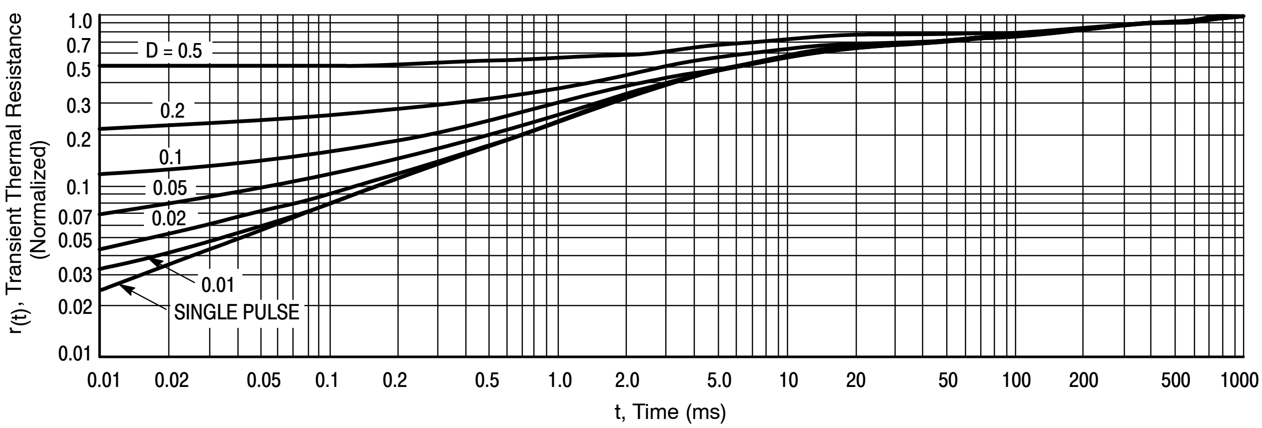


Figure 40. Thermal Response Showing the Duty Cycle Family of Curves

The average junction temperature increase above ambient is:

$$T_{J(average)} - T_C = R_{\theta JC} P_D D = (1.17)(50)(0.25) = 14.62°C \quad (3)$$

Note that T_J at the end of any power pulse does not equal the sum of the average temperature rise (14.62°C in the example) and that due to one pulse (28.5°C in example), because cooling occurs between the power pulses.

While junction temperature can be easily calculated for a steady pulse train where all pulses are of the same amplitude and pulse duration as shown in the previous example, a simple equation for arbitrary pulse trains with random variations is impossible to derive. However, since the heating and cooling response of a semiconductor is essentially the same, the superposition principle may be used to solve problems which otherwise defy solution.

Using the principle of superposition each power interval is considered positive in value, and each cooling interval negative, lasting from time of application to infinity. By multiplying the thermal resistance at a particular time by the magnitude of the power pulse applied, the magnitude of the junction temperature change at a particular time can be obtained. The net junction temperature is the algebraic sum of the terms.

The application of the superposition principle is most easily seen by studying Figure 3.

Figure 3(a) illustrates the applied power pulses. Figure 3(b) shows these pulses transformed into pulses lasting from time of application and extending to infinity; at t_o, P_1 starts and extends to infinity; at t_1, a pulse ($-P_1$) is considered to be present and thereby cancels P_1 from time t_1, and so forth with the other pulses. The junction temperature changes due to these imagined positive and negative pulses are shown in Figure 3(c). The actual junction temperature is the algebraic sum as shown in Figure 3(d).

Problems may be solved by applying the superposition principle exactly as described; the technique is referred to as Method 1, the pulse−by−pulse method. It yields satisfactory results when the total time of interest is much less than the time required to achieve steady state conditions, and must be used when an uncertainty exists in a random pulse train as to which pulse will cause the highest temperature. Examples using this method are given in Appendix A under Method 1.

For uniform trains of repetitive pulses, better answers result and less work is required by averaging the power pulses to achieve an average power pulse; the temperature is calculated at the end of one or two pulses following the average power pulse. The essence of this method is shown in Figure 6. The duty cycle family of curves shown in Figure 2 and used to solve the example problem is based on this method; however, the curves may only be used for a uniform train after steady state conditions are achieved. Method 2 in Appendix A shows equations for calculating the temperature at the end of the n_{th} or n + 1 pulse in a uniform train. Where a duty cycle family of curves is available, of course, there is no need to use this method.

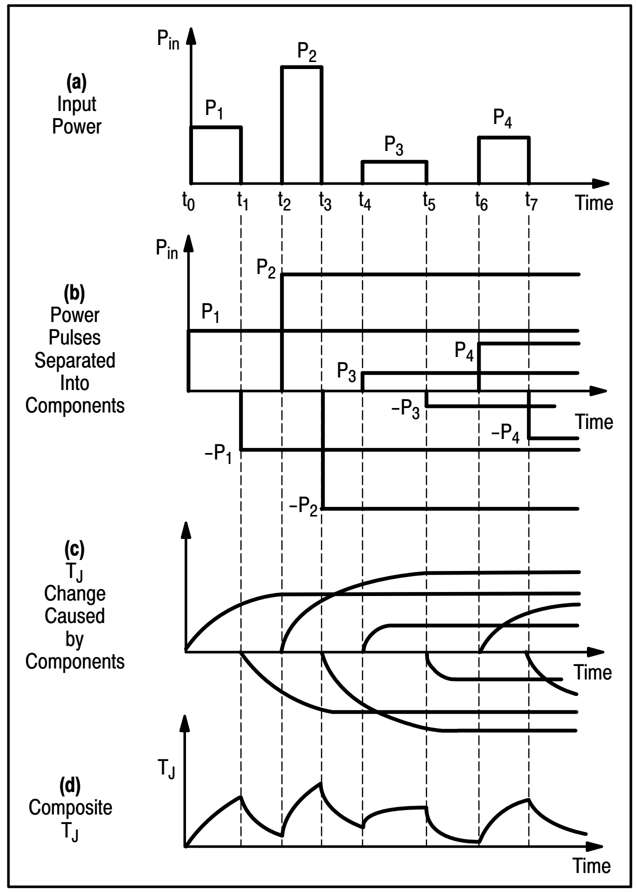


Figure 41. Application of Superposition Principle

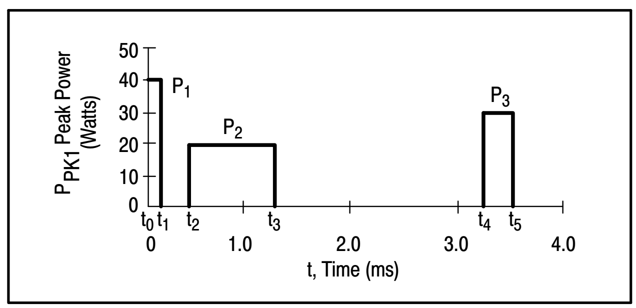


Figure 42. Non−Repetitive Pulse Train (Values Shown Apply to Example in Appendix)

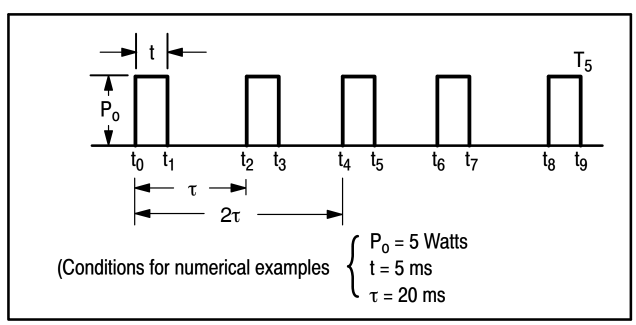


Figure 43. A Train of Equal Repetitive Pulses

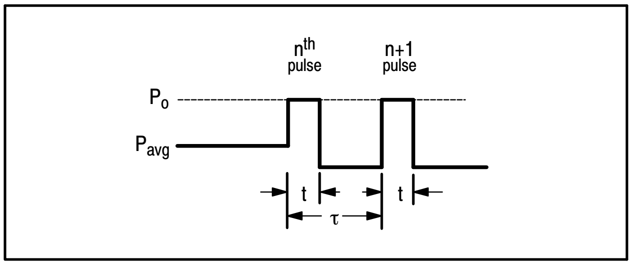


Figure 44. Model For a Repetitive Equal Pulse Train

Temperature rise at the end of a pulse in a uniform train before steady state conditions are achieved is handled by Method 3 (a or b) in the Appendix. The method is basically the same as for Method 2, except the average power is modified by the transient thermal resistance factor at the time when the average power pulse ends.

A random pulse train is handled by averaging the pulses applied prior to situations suspected of causing high peak temperatures and then calculating junction temperature at the end of the n_{th} or n + 1 pulse. Part c of Method 3 shows an example of solving for temperature at the end of the 3rd pulse in a three pulse burst.

HANDLING NON−RECTANGULAR PULSES

The thermal response curves, Figure 1, are based on a step change of power; the response will not be the same for other waveforms. Thus far in this treatment we have assumed a rectangular shaped pulse. It would be desirable to be able to obtain the response for any arbitrary waveform, but the mathematical solution is extremely unwieldy. The simplest approach is to make a suitable equivalent rectangular model of the actual power pulse and use the given thermal response curves; the primary rule to observe is that the energy of the actual power pulse and the model are equal.

Experience with various modeling techniques has lead to the following guidelines:

For a pulse that is nearly rectangular, a pulse model having an amplitude equal to the peak of the actual pulse, with the width adjusted so the energies are equal, is a conservative model. (See Figure 7(a)).

Sine wave and triangular power pulses model well with the amplitude set at 70% of the peak and the width adjusted to 91% and 71%, respectively, of the baseline width (as shown on Figure 7(b)).

A power pulse having a $\sin^2$ shape models as a triangular waveform.

Power pulses having more complex waveforms could be modeled by using two or more pulses as shown in Figure 7(c).

A point to remember is that a high amplitude pulse of a given amount of energy will produce a higher rise in junction temperature than will a lower amplitude pulse of longer duration having the same energy.

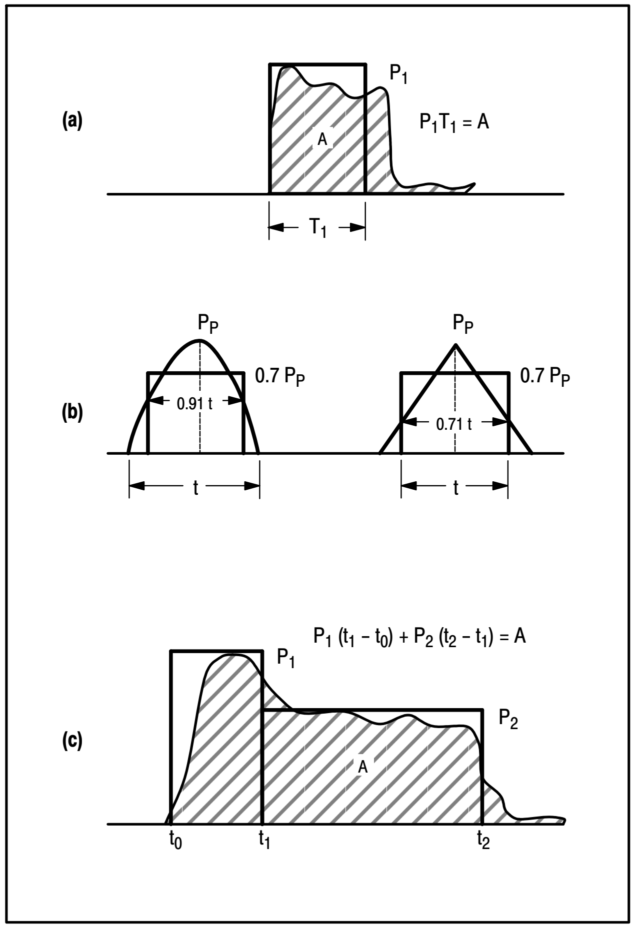


Figure 45. Modeling of Power Pulses

As an example, the case of a transistor used in a dc to ac power converter will be analyzed. The idealized waveforms of collector current, I_C, collector to emitter voltage, V_{CE}, and power dissipation P_D, are shown in Figure

A model of the power dissipation is shown in Figure 8(d). This switching transient of the model is made, as was suggested, for a triangular pulse.

For example, T_J at the end of the rise, on, and fall times, T_1, T_2 and T_3 respectively, will be found.

Conditions:

TO−3 package,

$R_{\theta JC}$ = 0.5°C/W, I_C = 60A, $V_{CE(off)}$ = 60 V
T_A = 50°C
t_f = 80 μs, t_r = 20 μs
$V_{CE(sat)}$ = 0.3 V @ 60 A
Frequency = 2 kHz∴τ = 500 μs
P_{on} = (60) (0.3) = 18 W
$P_f = 30 \times 30 = 900$ W = P_r

Assume that the response curve in Figure 1 for a die area of 58,000 square mils applies. Also, that the device is mounted on an MS−15 heat sink using Dow Corning DC340 silicone compound with an air flow of 1.0 lb/min flowing across the heat−sink. (From MS−15 Data Sheet, $R_{\theta CS}$ = 0.1°C/W and $R_{\theta SA}$ = 0.55°C/W).

Procedure: Average each pulse over the period using equation 1−3 (Appendix A, Method 2), i.e.,

$$
\begin{aligned}
P_{avg} &= 0.7\ P_r\ 0.71\ \frac{t_r}{\tau} + Pon\ \frac{ton}{\tau} + 0.7\ P_f\ 0.71\ \frac{t_f}{\tau} \\
&= (0.7)\ (900)\ (0.71)\ \frac{(20)}{500} + (18)\ \frac{(150)}{500} \\
&\quad + (0.7)\ (900)\ (0.71)\ \frac{80}{500} \\
&= 17.9 + 5.4 + 71.5 \\
&= 94.8\ W
\end{aligned}
$$

From equation 1−4, Method 2A:

$$T_1 = [P_{avg} + (0.7\ P_r - P_{avg}) \cdot r(t_1 - t_o)]\ R_{\theta JC}$$

At this point it is observed that the thermal response curves of Figure 1 do not extend below 100 μs. Heat transfer theory for one dimensional heat flow indicates that the response curve should follow the $\sqrt{t}$ law at small times. Using this as a basis for extending the curve, the response at 14.2 μs is found to be 0.023.

We then have:

$$
\begin{aligned}
T_1 &= [94.8 + (630 - 94.8).023]\ (0.5) \\
&= (107.11)(0.5) = 53.55°C
\end{aligned}
$$

For T_2 we have, by using superposition:

$$
\begin{aligned}
T_2 &= [P_{avg} - P_{avg} \cdot r(t_2 - t_o) + 0.7\ P_r \cdot \\
&\quad r(t_2 - t_o) - 0.7\ P_r \cdot r(t_2 - t_1) + Pon \cdot \\
&\quad r(t_2 - t_1)]\ R_{\theta JC} \\
&= [P_{avg} + (0.7\ P_r - P_{avg}) \cdot r(t_2 - t_o) + \\
&\quad (Pon - 0.7\ P_r) \cdot r(t_2 - t_1)]\ R_{\theta JC} \\
&= [94.8 + (630 - 94.8) \cdot r(164\ \mu s) + (18 - 630) \\
&\quad \cdot r(150\ \mu s)]\ (0.5) \\
&= [94.8 + (535.2)(.079) - (612)(.075)]\ (0.5) \\
&= [94.8 + 42.3 - 45.9]\ (0.5) \\
&= (91.2)(0.5) = 45.6°C
\end{aligned}
$$

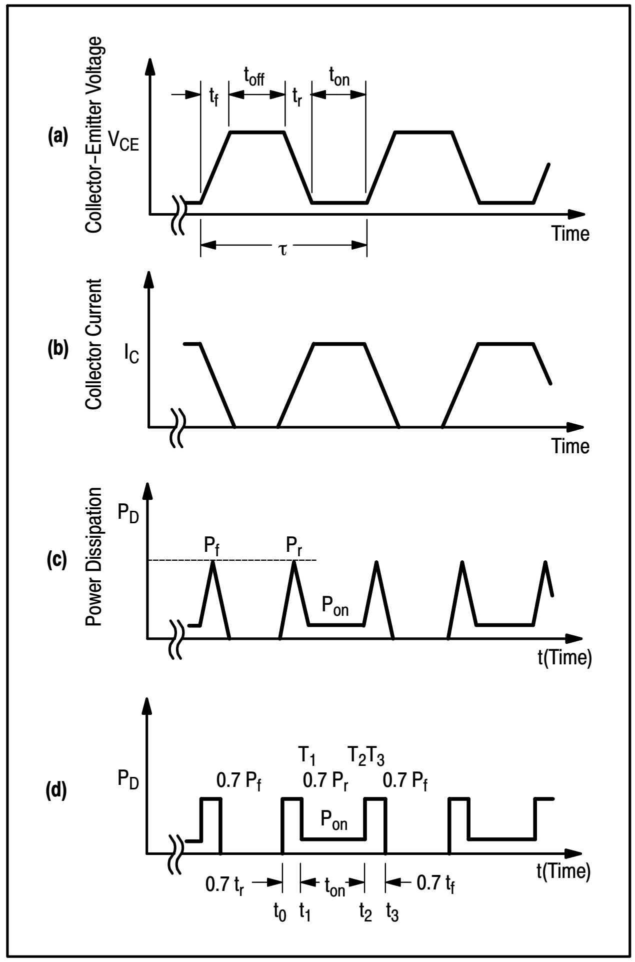


Figure 46. Idealized Waveforms of I_C, V_{CE} and P_D in a DC to AC Inverter

For the final point T_3 we have:

$$
\begin{aligned}
T_3 &= [P_{avg} - P_{avg} \cdot r(t_3 - t_o) + 0.7\ P_r \cdot \\
&\quad r(t_3 - t_o) - 0.7\ P_r \cdot r(t_3 - t_1) + Pon \cdot \\
&\quad r(t_3 - t_1) - Pon \cdot r(t_3 - t_2) \\
&\quad + 0.7\ P_f \cdot r(t_3 - t_2)]\ R_{\theta JC} \\
&\quad [P_{avg} + (0.7\ P_r - Pavg) \cdot r(t_3 - t_o) + \\
&\quad (Pon - 0.7\ P_r) \cdot r(t_3 - t_1) + (0.7\ P_f - Pon) \\
&\quad \cdot\ r(t_3 - t_2)]\ R_{\theta JC} \\
&= [94.8 + (535.2) \cdot r(221\ \mu s) + (-612) \cdot r(206.8\ \mu s) \\
&\quad + (612) \cdot r(56.8 \mu s)]\ (0.5) \\
&= [94.8 + (535.2)(0.09) - (612)\ (0.086) + \\
&\quad (612)(0.045)]\ (0.5) \\
&= [94.8 + 481.7 - 52.63 + 27.54]\ (0.5) \\
&= (117.88)(0.5) = 58.94°C
\end{aligned}
$$

The junction temperature at the end of the rise, on, and fall times, T_{J1}, T_{J2}, and T_{J3}, is as follows:

$$T_{J1} = T_1 + T_A + R_{\theta CA} \cdot P_{avg}$$
$$R_{\theta CA} = R_{\theta CS} = R_{\theta SA} = 0.1 + 0.55$$
$$T_{J1} = 53.55 + 50 + (0.65)(94.8) = 165.17°C$$
$$T_{J2} = T_2 + T_A + R_{\theta CA} \cdot P_{avg}$$
$$= 45.6 + 50 + (0.65)(94.8)$$
$$= 157.22°C$$
$$T_{J3} = T_3 + T_A + R_{\theta CA} \cdot P_{avg}$$
$$= 58.94 + 50 + (0.65)(94.8)$$
$$= 170.56°C$$
$$T_{J(avg)} = P_{avg}\,(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A$$
$$= (94.8)(0.5 + 0.1 + 0.55) + 50$$
$$= (94.8)(1.15) + 50 = 159.02°C$$

Inspection of the results of the calculations T_1, T_2, and T_3 reveal that the term of significance in the equations is the average power. Even with the poor switching times there was a peak junction temperature of 11.5°C above the average value. This is a 7% increase which for most applications could be ignored, especially when switching times are considerably less. Thus the product of average power and steady state thermal resistance is the determining factor for junction temperature rise in this application.

SUMMARY

This report has explained the concept of transient thermal resistance and its use. Methods using various degrees of approximations have been presented to determine the junction temperature rise of a device. Since the thermal response data shown is a step function response, modeling of different wave shapes to an equivalent rectangular pulse of pulses has been discussed.

The concept of a duty cycle family of curves has also been covered; a concept that can be used to simplify calculation of the junction temperature rise under a repetitive pulse train.

APPENDIX A METHODS OF SOLUTION

In the examples, a type 2N3647 transistor will be used; its steady state thermal resistance, $R_{\theta JC}$, is 35°C/W and its value for r(t) is shown in Figure A1.

Definitions:

$P_1, P_2, P_3 \ldots P_n$ = power pulses (Watts)

$T_1, T_2, T_3 \ldots T_n$ = junction to case temperature at end of $P_1, P_2, P_3 \ldots P_n$

$t_0, t_1, t_2, \ldots t_n$ = times at which a power pulse begins or ends

$r(t_n - t_k)$ = transient thermal resistance factor at end of time interval $(t_n - t_k)$.

Table 1. Several Possible Methods of Solutions

1. Junction Temperature Rise Using Pulse−By−Pulse Method
   - A. Temperature rise at the end of the n_{th} pulse for pulses with unequal amplitude, spacing, and duration.
   - B. Temperature rise at the end of the n_{th} pulse for pulses with equal amplitude, spacing, and duration.
2. Temperature Rise Using Average Power Concept Under Steady State Conditions For Pulses Of Equal Amplitude, Spacing, And Duration
   - A. At the end of the n_{th} pulse.
   - B. At the end of the (n + 1) pulse.
3. Temperature Rise Using Average Power Concept Under Transient Conditions.
   - A. At the end of the n_{th} pulse for pulses of equal amplitude, spacing and duration.
   - B. At the end of the n + 1 pulse for pulses of equal amplitude, spacing and duration.
   - C. At the end of the n_{th} pulse for pulses of unequal amplitude, spacing and duration.
   - D. At the end of the n + 1 pulse for pulses of unequal
   - J amplitude, spacing and duration.

METHOD 1A − FINDING T_J AT THE END OF THE Nth PULSE IN A TRAIN OF UNEQUAL AMPLITUDE, SPACING, AND DURATION

General Equation:

$$T_n = \sum_{i=1}^{n} P_i\,[r(t_{2n-1} - t_{2i-2}) - r(t_{n-1} - t_{2i-1})]R_{\theta JC} \qquad (1-1)$$

where n is the number of pulses and P_i is the peak value of the i^{th} pulse.

To find temperature at the end of the first three pulses, Equation 1−1 becomes:

$$T_1 = P_1\,r(t_1)\,R_{\theta JC} \qquad (1-1A)$$
$$T_2 = [P_1\,r(t_3) - P_1\,r(t_3 - t_1) + P_2\,r(t_3 - t_2)]\,R_{\theta JC} \qquad (1-1B)$$
$$T_3 = [P_1\,r(t_5) - P_1\,r(t_5 - t_1) + P_2\,r(t_5 - t_2) - P_2\,r(t_5 - t_3) + P_3\,r(t_5 - t_4)]\,R_{\theta JC} \qquad (1-1C)$$

Example:

Conditions are shown on Figure 4 as:

P_1 = 40 W	t_0 = 0	t_3 = 1.3 ms
P_2 = 20 W	t_1 = 0.1 ms	t_4 = 3.3 ms
P_3 = 30 W	t_2 = 0.3 ms	t_5 = 3.5 ms

Therefore,

$t_1 - t_0 = 0.1$ ms $\quad t_3 - t_1 = 1.2$ ms
$t_2 - t_1 = 0.2$ ms $\quad t_5 - t_1 = 3.4$ ms
$t_3 - t_2 = 1$ ms $\quad t_5 - t_2 = 3.2$ ms
$t_4 - t_3 = 2$ ms $\quad t_5 - t_3 = 2.2$ ms
$t_5 - t_4 = 0.2$ ms

Procedure:

Find $r(t_n - t_k)$ for preceding time intervals from Figure 2, then substitute into Equations 1−1A, B, and C.

$$T_1 = P_1\, r(t_1)\, R_{\theta JC} = 40 \cdot 0.05 \cdot 35 = 70°C$$

$$\begin{aligned} T_2 &= [P_1\, r(t_3) - P_1\, r(t_3 - t_1) + P_2\, r(t_3 - t_2)]\, R_{\theta JC} \\ &= [40\,(0.175) - 40\,(0.170) + 20\,(0.155)]\, 35 \\ &= [40\,(0.175 - 0.170) + 20\,(0.155)]\, 35 \\ &= [0.2 + 3.1]\, 35 = 115.5°C \end{aligned}$$

$$\begin{aligned} T_3 &= [P_1\, r(t_5) - P_1\, r(t_5 - t_1) + P_2\, r(t_5 - t_2) \\ &\quad - P_2\, r(t_5 - t_3) + P_3\, r(t_5 - t_4)]\, \theta_{JC} \end{aligned}$$

$$\begin{aligned} T_3 &= [40\,(0.28) - 40\,(0.277) + 20\,(0.275) - 20\,(0.227) \\ &\quad + 30\,(0.07)]\, 35 \\ &= [40\,(0.28 - 0.277) + 20\,(0.275 - 0.227) \\ &\quad + 30\,(0.07)]\, 35 \\ &= [0.12 + 0.96 + 2.1]^{\dagger}\, 35 = 3.18 \cdot 35 = 111.3°C \end{aligned}$$

Note, by inspecting the last bracketed term in the equations above that very little residual temperature is left from the first pulse at the end of the second and third pulse. Also note that the second pulse gave the highest value of junction temperature, a fact not so obvious from inspection of the figure. However, considerable residual temperature from the second pulse was present at the end of the third pulse.

METHOD 1B – FINDING T_J AT THE END OF THE Nth PULSE IN A TRAIN OF EQUAL AMPLITUDE, SPACING, AND DURATION

The general equation for a train of equal repetitive pulses can be derived from Equation 1−1. $P_i = P_D$, $t_i = t$, and the spacing between leading edges or trailing edges of adjacent pulses is τ.

General Equation:

$$T_n = P_D R_{\theta JC} \sum_{i=1}^{n} r[(n - i)\,\tau + t] - r[(n - i)\,\tau] \qquad (1–2)$$

Expanding:

$$\begin{aligned} T_n &= P_D\, R_{\theta JC}\, r[(n - 1)\,\tau + t] - r[(n - 1)\,\tau] \\ &\quad + r[(n - 2)\,\tau + t) - r[(n - 2)\,\tau] + r[(n - 3) \\ &\quad \tau + t] - r[(n - 3)\,\tau] + \ldots + r[(n - i)\,\tau + t] \\ &\quad - r[(n - i)\,\tau] \ldots\ldots + r(t)] \end{aligned} \qquad (1–2A)$$

---

† Relative amounts of temperature residual from P_1, P_2, and P_3 respectively are indicated by the terms in brackets.

For 5 pulses, equation 1−2A is written:

$$\begin{aligned} T_5 &= P_D\, R_{\theta JC}\, [r(4\,\tau + t) - r(4\tau) + r(3\tau + t)] \\ &\quad - r(3\tau) + r(2\tau + t) - r(2\tau) + r(\tau + t) \\ &\quad - r(\tau) + r(t)] \end{aligned}$$

Example:

Conditions are shown on Figure 5 substituting values into the preceding expression:

$$\begin{aligned} T_5 &= (5)\,(35)\,[r(4.20 + 5) - r(4.20) + r(3.20 + 5) \\ &\quad + r(3.20) + r(2.20 + 5) - r(2.20) + r(20 + 5) \\ &\quad - r(20) + r(5)] \\ T_5 &= (5)\,(35)\,[0.6 - 0.76 + 0.73 - 0.72 + 0.68 \\ &\quad - 0.66 + 0.59 - 0.55 + 0.33] - (5)(35)(0.40) \\ T_5 &= 70.0°C \end{aligned}$$

Note that the solution involves the difference between terms nearly identical in value. Greater accuracy will be obtained with long or repetitive pulse trains using the technique of an average power pulse as used in Methods 2 and 3.

METHOD 2 – AVERAGE POWER METHOD, STEADY STATE CONDITION

The essence of this method is shown in Figure 6. Pulses previous to the n_{th} pulse are averaged. Temperature due to the n_{th} or n + 1 pulse is then calculated and combined properly with the average temperature.

Assuming the pulse train has been applied for a period of time (long enough for steady state conditions to be established), we can average the power applied as:

$$P_{avg} = P_D\, \frac{t}{\tau} \qquad (1–3)$$

METHOD 2A – FINDING TEMPERATURE AT THE END OF THE N_{th} PULSE

Applicable Equation:

$$T_n = [P_{avg} + (P_D - P_{avg})\, r(t)]\, R_{\theta JC} \qquad (1–4)$$

or, by substituting Equation 1−3 into 1−4,

$$Tn = \left[\frac{t}{\tau} + \left(1 - \frac{t}{\tau}\right) r(t)\right] P_D\, R\theta JC \qquad (1–5)$$

The result of this equation will be conservative as it adds a temperature increase due to the pulse ($P_D - P_{avg}$) to the average temperature. The cooling between pulses has not been accurately accounted for; i.e., T_J must actually be less than $T_{J(avg)}$ when the n^{th} pulse is applied.

Example: Find T_n for conditions of Figure 5.
Procedure: Find P_{avg} from equation (1−3) and substitute values in equation (1−4) or (1−5).

$$\begin{aligned} T_n &= [(1.25) + (5.0 - 1.25)(0.33)]\,(35) \\ &= 43.7 + 43.2 = 86.9°C \end{aligned}$$

METHOD 2B – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE

Applicable Equation:

$$T_{n+1} = [P_{avg} + (P_D - P_{avg})\, r(t+\tau) + P_D\, r(t) - P_D\, r(\tau)]\, R_{\theta JC} \quad (1-6)$$

or, by substituting equation 1−3 into 1−6,

$$T_{n+1} = \left[\frac{t}{\tau} + \left(1 - \frac{t}{\tau}\right) r(t+\tau) + r(t) - r(\tau)\right] P_D R_{\theta JC} \quad (1-7)$$

Example: Find T_n for conditions of Figure 5.
Procedure: Find P_{avg} from equation (1−3) and substitute into equation (1−6) or (1−7).

$$T_{n+1} = [(1.25) + (5 - 1.25)(0.59) + (5)(0.33) - (5)(0.56)]\,(35) = 80.9°C$$

Equation (1−6) gives a lower and more accurate value for temperature than equation (1−4). However, it too gives a higher value than the true T_J at the end of the n + 1th pulse. The error occurs because the implied value for T_J at the end of the nth pulse, as was pointed out, is somewhat high. Adding additional pulses will improve the accuracy of the calculation up to the point where terms of nearly equal value are being subtracted, as shown in the examples using the pulse by pulse method. In practice, however, use of this method has been found to yield reasonable design values and is the method used to determine the duty cycle of family of curves − e.g., Figure 2.

Note that the calculated temperature of 80.9°C is 10.9°C higher than the result of example 1B, where the temperature was found at the end of the 5th pulse. Since the thermal response curve indicates thermal equilibrium in 1 second, 50 pulses occurring 20 milliseconds apart will be required to achieve stable average and peak temperatures; therefore, steady state conditions were not achieved at the end of the 5th pulse.

METHOD 3 – AVERAGE POWER METHOD, TRANSIENT CONDITIONS

The idea of using average power can also be used in the transient condition for a train of repetitive pulses. The previously developed equations are used but P_{avg} must be modified by the thermal response factor at time $t_{(2n-1)}$.

METHOD 3A – FINDING TEMPERATURE AT THE END OF THE N_{th} PULSE FOR PULSES OF EQUAL AMPLITUDE, SPACING AND DURATION

Applicable Equation:

$$T_n = \left[\frac{t}{\tau}\, r\, t_{(2n-1)} + \left(1 - \frac{t}{\tau}\right) r(t)\right] P_D R_{\theta JC} \quad (1-8)$$

Conditions: (See Figure 5)
Procedure: At the end of the 5th pulse (See Figure 7) . . .

$$T_5 = [5/20 \cdot r(85) + (1 - 5/20) r(5)]\,(5)(35)$$
$$= [(0.25)(0765) + (0.75)(0.33)]\,(175)$$
$$= 77°C$$

This value is a little higher than the one calculated by summing the results of all pulses; indeed it should be, because no cooling time was allowed between P_{avg} and the nth pulse. The method whereby temperature was calculated at the n + 1 pulse could be used for greater accuracy.

METHOD 3B – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE FOR PULSES OF EQUAL AMPLITUDE, SPACING AND DURATION

Applicable Equation:

$$T_{n+1} = \left[\frac{t}{\tau}\, r(t_{2n-1}) + \left(1 - \frac{t}{\tau}\right) r(t+\tau) + r(t) - r(\tau)\right] P_D R_{\theta JC} \quad (1-9)$$

Example: Conditions as shown on Figure 5. Find temperature at the end of the 5th pulse.

For n + 1 = 5, n = 4, $t_{2n-1} = t_7 = 65$ ms,

$$T_5 = \left[\frac{5}{20}\, r(65\text{ ms}) + \left(1 - \frac{5}{20}\right) r(25\text{ ms}) + r(5\text{ ms}) - r(20\text{ ms})\right] (5)(35)$$

$$T_5 = [(0.25)(0.73) + (0.75)(0.59) + 0.33 - 0.55](5)(35)$$

$$T_5 = 70.8°C$$

The answer agrees quite well with the answer of Method 1B where the pulse−by−pulse method was used for a repetitive train.

METHOD 3C – FINDING T_J AT THE END OF THE N_{th} PULSE IN A RANDOM TRAIN

The technique of using average power does not limit itself to a train of repetitive pulses. It can be used also where the pulses are of unequal magnitude and duration. Since the method yields a conservative value of junction temperature rise it is a relatively simple way to achieve a first approximation. For random pulses, equations 1−4 through 1−7 can be modified. It is necessary to multiply P_{avg} by the thermal response factor at time $t_{(2n-1)}$. P_{avg} is determined by averaging the power pulses from time of application to the time when the last pulse starts.

Applicable Equations:

$$\text{General: } P_{avg} = \sum_{i=1}^{n} P_i \frac{t_{(2i-1)} - t_{(2i-2)}}{t_{(2n)} - t_{(2i-2)}} \qquad (1-10)$$

For 3 Pulses:

$$P_{avg} = P_1 \frac{t_1 - t_0}{t_4 - t_0} + P_2 \frac{t_3 - t_2}{t_4 - t_2} \qquad (1-11)$$

Example: Conditions are shown on Figure 4 (refer to Method 1A).

Procedure: Find P_{avg} from equation 1−3 and the junction temperature rise from equation 1−4.

Conditions: Figure 4

$$P_{avg} = 40 \cdot \frac{0.1}{3.3} + 20 \frac{1}{3} = 1.21 + 6.67$$
$$= 7.88 \text{ Watts}$$
$$T_3 = [P_{avg}\, r(t_5) + (P_3 - P_{avg})\, r(t_5 - t_4)]\, R_{\theta JC}$$
$$= [7.88\,(0.28) + (30 - 7.88) \cdot 0.07]\, 35$$
$$= [2.21 + 1.56]\, 35 = 132°C$$

This result is high because in the actual case considerable cooling time occurred between P_2 and P_3 which allowed T_J to become very close to T_C. Better accuracy is obtained when several pulses are present by using equation 1−10 in order to calculate $T_J - t_C$ at the end of the $n^{th} + 1$ pulse. This technique provides a conservative quick answer if it is easy to determine which pulse in the train will cause maximum junction temperature.

METHOD 3D – FINDING TEMPERATURE AT THE END OF THE N + 1 PULSE IN A RANDOM TRAIN

The method is similar to 3C and the procedure is identical. P_{avg} is calculated from Equation 1−10 modified by $r(t_{2n-1})$ and substituted into equation 1−6, i.e.,

$$T_{n+1} = [P_{avg}\, r(t_{2n-1}) + (P_D - P_{ave})\, r(t_{2n-1} - t_{2n-2}) + P_D\, r(t_{2n+1} - t_{2n}) - P_D\, r(t_{2n+1} - t_{2n-1})]\, R_{\theta JC}$$

The previous example cannot be worked out for the n + 1 pulse because only 3 pulses are present.

Table 2. Summary Of Numerical Solution For The Repetitive Pulse Train Of Figure 5

Temperature Desired	Temperature Obtained, °C		
	Pulse by Pulse	Average Power Nth Pulse	Average Power N + 1 Pulse
At End of 5th Pulse	70.0 (1B)	77 (3A)	70.8 (3B)
Steady State Peak	–	86.9 (2A)	80.9 (2B)

Note: Number in parenthesis is method used.

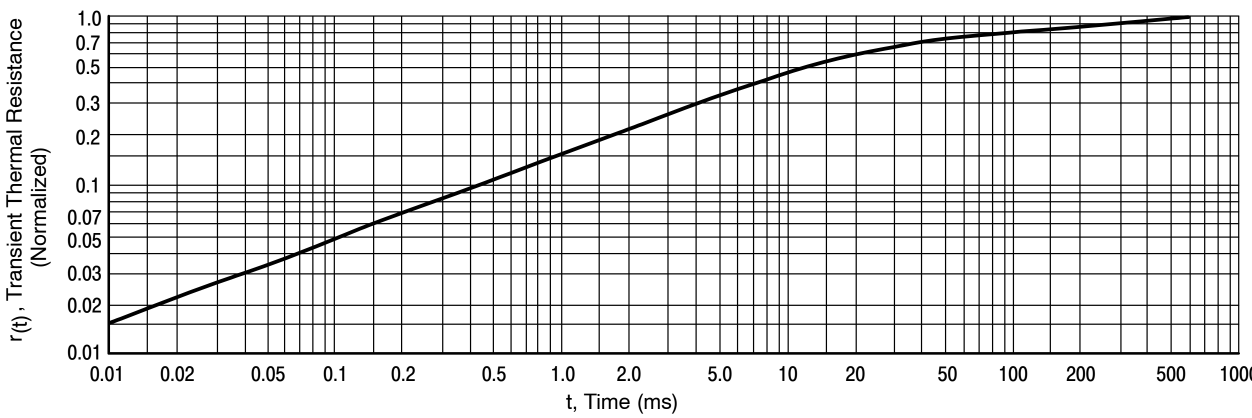


Figure 47. 2N3467 Transient Thermal Response

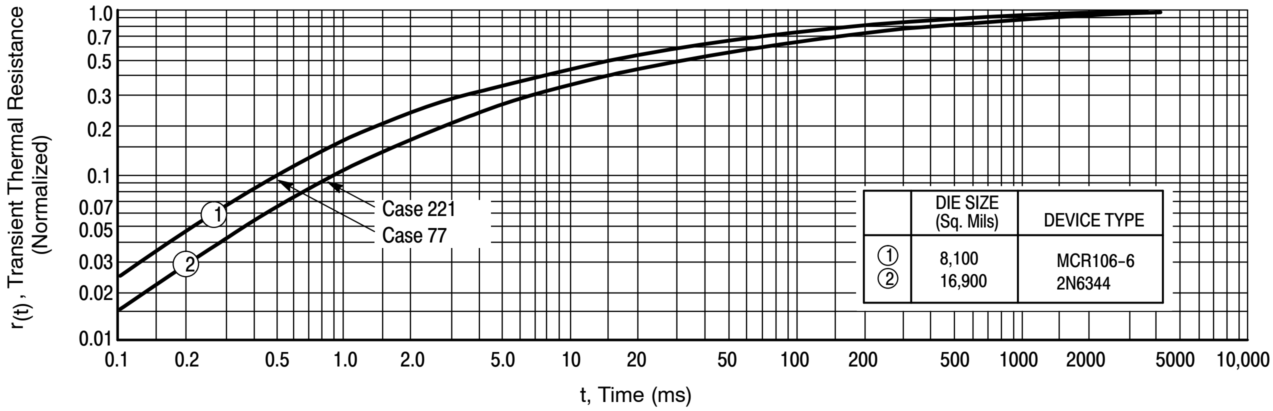


Figure 48. Case 77 and TO−220 Thermal Response

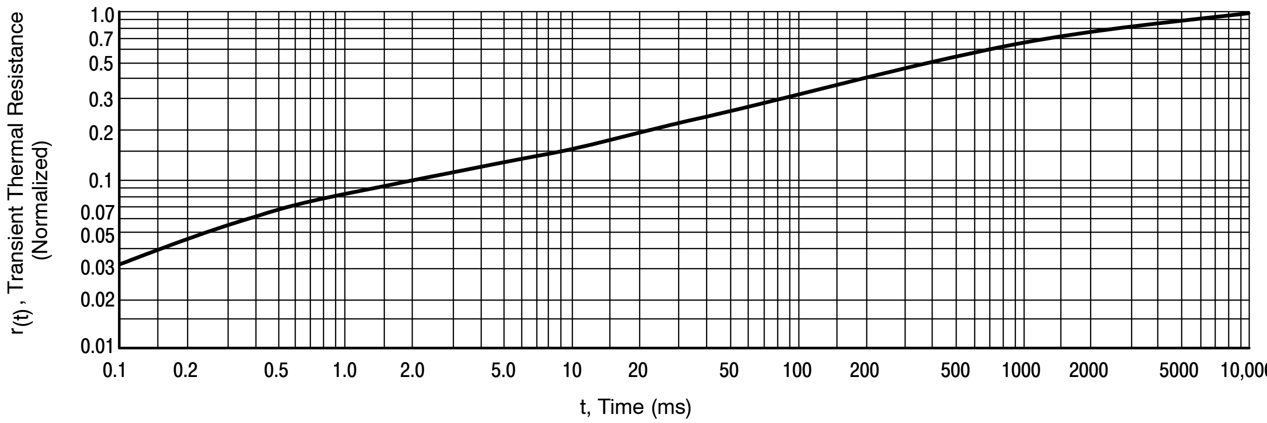


Figure 49. TO−92 Thermal Response, Applies to All Commonly Used Die

SPICE Generates the Thermal Response Models of a Power Semiconductor

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INTRODUCTION

An equivalent electric circuit consisting of a resistor−capacitor network can be used to describe both the steady−state and transient thermal response of a power semiconductor device. Combined with SPICE, this network is extremely useful in determining a device's junction temperature for any input power condition or waveform that can be modeled in SPICE.

This paper will cover the following topics:

- Understanding basic transient thermal response of power semiconductors
- Basic transient thermal response test methods
- The thermal equivalent SPICE model
- Examples of using SPICE to model transient thermal response of power devices

Understanding Basic Transient Thermal Response of Power Semiconductors

Having already described the basic thermal parameters of power semiconductors in "**Basic Semiconductor Thermal Measurement**", [1] this paper will focus primarily on the thermal equivalent circuit and how it applies to transient and steady−state thermal analysis.

The thermal behavior of a power semiconductor device can be described by a resistor−capacitor network as shown in Figure 50. This network shows the most commonly used thermal equivalent model for a power semiconductor. More elements (RC sections) can be added to increase the model detail as required. The third order model shown in Figure 50 is relatively simple yet accurately describes the thermal performance of a power semiconductor device.

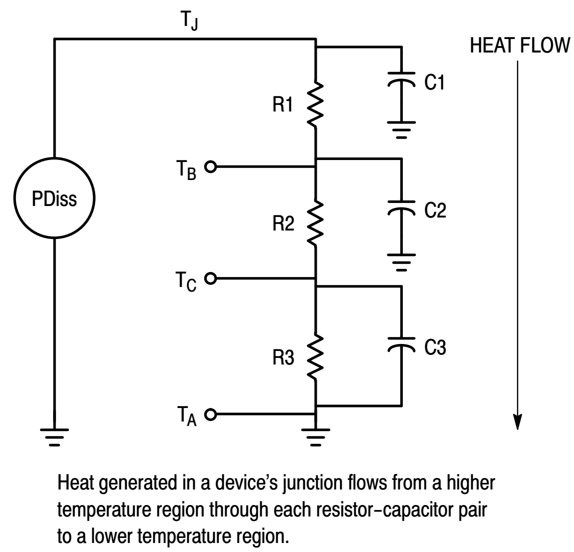


Figure 50. Thermal Electrical Equivalent Circuit

The thermal circuit shown in Figure 50 is governed by three basic equations which are similar to the three forms of Ohm's law.

Thermal Equation	**Electrical Equivalent**	
$R_{th} = \Delta T/P_D$	$R = V/I$	(1)
$\Delta T = P_D{*}R_{th}$	$V = I{*}R$	(2)
$P_D = \Delta T/R_{th}$	$I = V/R$	(3)

Where:

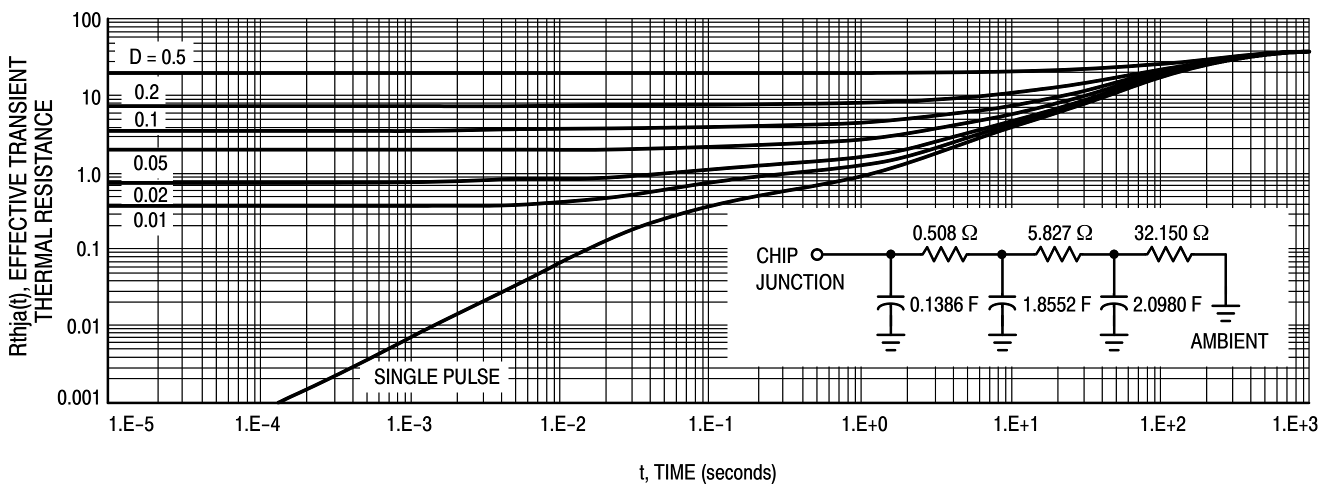
- R_{th}, thermal resistance, is analogous to resistance
- ΔT is analogous to a voltage drop
- P_D, power dissipation, is analogous to current flow
- a *voltmeter* is analogous to a thermometer

Resistors R1, R2, and R3 in Figure 50 are all analogous to individual thermal resistances, or quantities that impede heat flow. Resistor R1 represents the thermal resistance from the device's junction to its die−bond. The "junction" of a power semiconductor, whether it be a pn interface or a schottky barrier, is the location where heat is generated within the device. Resistor R2 represents the thermal resistance from the die−bond to the device's case. Resistor

R3 represents the thermal resistance from the device's case−to−ambient. The steady−state thermal resistance from the junction to some reference point is equal to the sum of the individual resistors between the two points. For instance, the thermal resistance, R_{thjc}, from junction−to−case is equal to the sum of resistors R1 and R2. The thermal resistance, R_{thja}, from junction−to−ambient, therefore, is equal to the sum of resistors R1, R2, and R3.

The capacitors shown in Figure 50 help model the transient−thermal−response of the device. When heat is instantaneously applied and or generated, a thermal charging takes place as heat passes from one point to another with−in the device. This charging effect and/or transient thermal response, as it is traditionally called, follows an RC time constant determined by the resistors and capacitors in the thermal network.

The thermal resistance at any given point in time is equivalent to the total impedance of the circuit under applied power at that time. The total impedance of the network would initially be small and increase over time as the capacitors charge (see Figure 51). As time progresses and the capacitors fully charge, a steady−state condition is reached. When a steady−state condition is reached, the total impedance is simply the sum of the resistors R1, R2, and R3. The total impedance as a function of time is called transient thermal resistance, $R_{thjr(t)}$.



The device shown is mounted on a standard 2 inch square FR4 board with minimum recommended pads. The initial transient thermal resistance starts out very low and increases over time until it reaches its steady−state value.

Figure 51. Transient thermal response curve for an MTV32N20E D3Pak surface mounted power MOSFET device with RC values shown.

Basic Transient Thermal Response Test Methods

The old traditional method of measuring transient thermal response is as follows:

1. Heat the device by applying power until it reaches steady−state
2. Remove the power from the device and begin sampling the TSP (**T**emperature **S**ensitive **P**arameter)
3. Reduce the collected TSP data and normalize it for graphing

This is known as the cooling curve method because the thermal response is measured while the device is cooling. Theory states that the cooling curve is identical to the heating curve, but it is the heating not the cooling of the device that the circuit designer is really interested in. The collected data, therefore, would have to be re−arranged and presented as a heating−curve similar to that shown in Figure 51.

Generally, the best approach to quantify the transient thermal behavior of a device is to generate a heating characterization curve. This is usually done by applying constant power pulses for varying lengths of time and measuring the thermal impedance for this time period. Unfortunately, the applied pulses, for all practicality, are usually rectangular. The data obtained, therefore, represents only rectangular pulses. With this type of transient data (i.e.. rectangular heating pulse) the user must apply his own design conditions by adjusting for non−rectangular pulses. This is usually done with some sort of equivalent and/or superposition technique. [3]

One big advantage that some of the latest test equipment provides is the generation of the RC network values shown in Figures 50 and 51. The RC network values are derived by using error−minimization routines to solve the differential equations that describe the thermal circuit behavior. Actual versus simulated thermal response data for the MTV32N20E device is shown in Figure 53. The RC network derived by these testers provides both the designer and the device manufacturer with a tremendous tool. Thermal circuit RC networks can also be extracted from the collected data by using such software as Sauna™ from Thermal Solutions (313−761−1956).

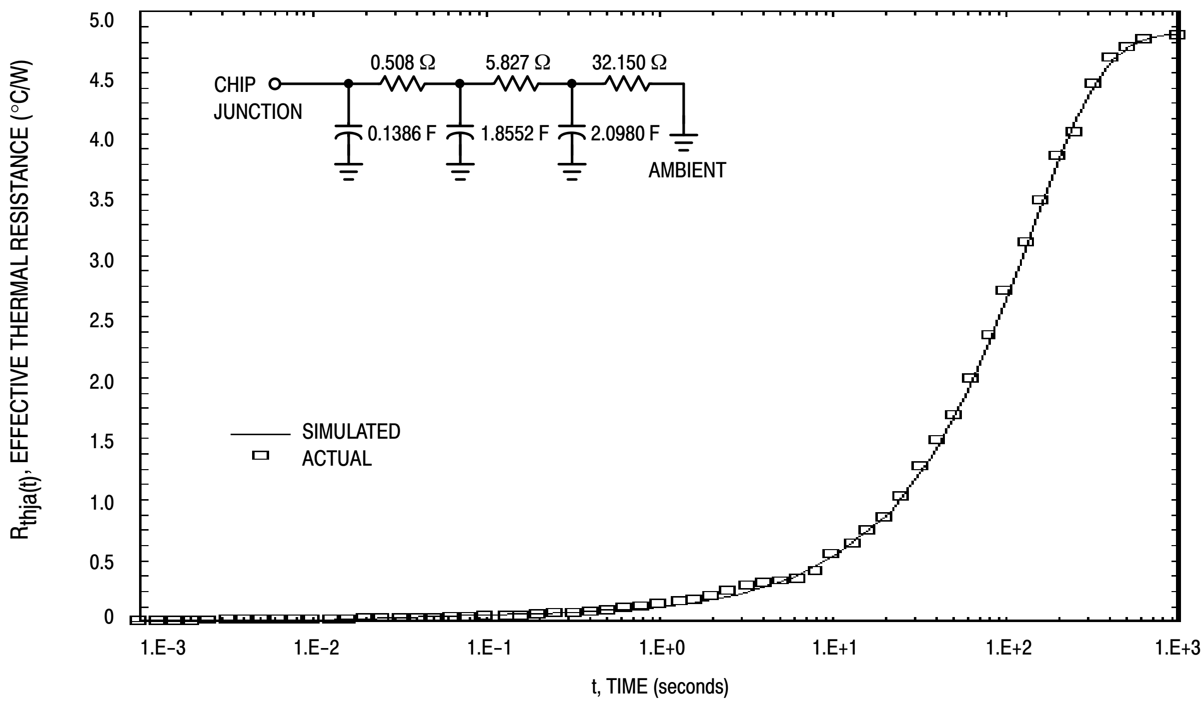


Figure 52. Simulated and actual transient thermal response curves and the thermal equivalent circuit for the MTV32N20E power MOSFET device mounted on a 2 in. x 2 in., 2 oz. Cu, FR4 board with the minimum recommended footprint.

The main advantages of using an RC network for thermal modeling are:

- Individual thermal resistances and time constants of the device's internal package can be shown
- Provides the opportunity to determine where package enhancements can be made to improve thermal performance
- The ability to simulate the device's thermal behavior using SPICE under any power pulse condition

The Thermal Equivalent SPICE Model

Using SPICE, equations (1), (2), and (3), and the RC network derived from the transient thermal response measurements, a model of the thermal behavior for a device under various power conditions can be generated. This provides the designer with a direct way to determine a device's operating junction temperature under the unique electrical conditions of the application circuit, thus insuring circuit reliability.

The p–channel MOSFET, MMSF4P01Z, packaged in an SOIC8 platform will be used to demonstrate the application of this thermal modeling technique. Shown in Figure 53 is the transient thermal response for the MMSF4P01Z along with its synthesized or derived equivalent thermal RC network. A sample SPICE input deck for the thermal circuit is illustrated in Figure 54. It should be recalled that current in the electrical circuit is analogous to power dissipation in the thermal circuit (equation 3), hence, the reason for the current sources in the circuit program. Figure 54 represents the SPICE input deck which produces the input and output waveforms of Figure 55. As can be seen, multiple power inputs can be used to create fairly complex power dissipation waveforms. Keep in mind that the input stimulus to the thermal circuit is power, which is the product of the voltage and current applied to the device of interest.

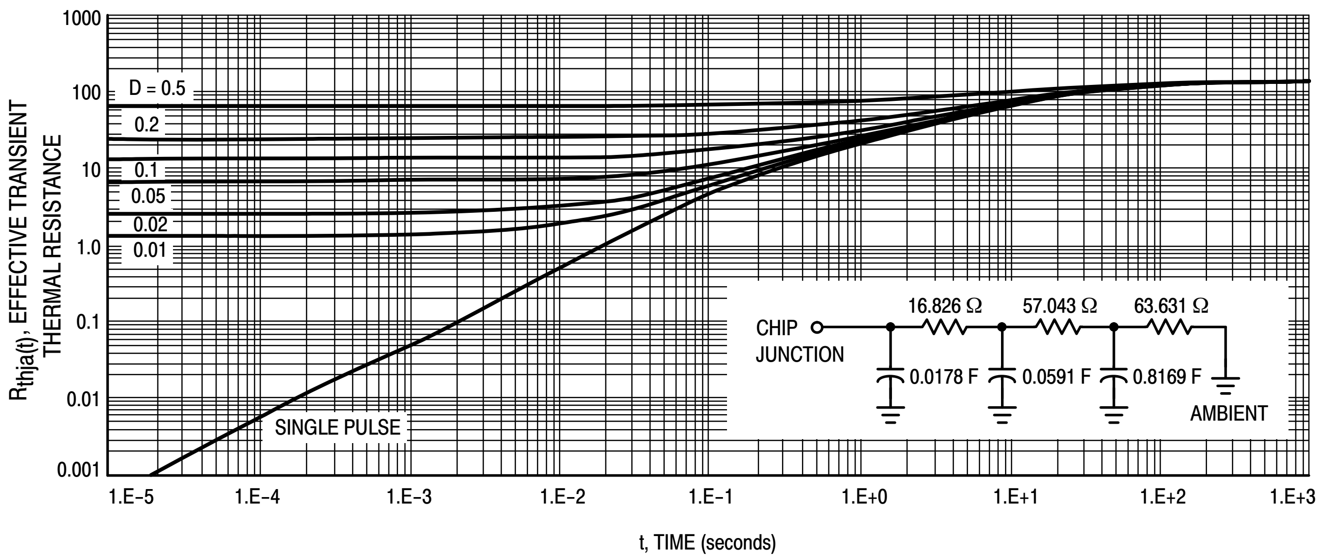


Figure 53. Transient thermal response curve and thermal equivalent circuit for the MMSF4P01Z power MOSFET device mounted on a 2 in. x 2 in., 2 oz. Cu, FR4 board with the minimum recommended footprint.

```
THERMAL RESPONSE SIMULATION − MMSF4P01Z
*
IPDISS1  0  1   PULSE(0A 1A 0S 10MS 1US 1US 20MS)
IPDISS2  0  1   PULSE(0A 20A 0S 10MS 1US 1US 20MS)
CT1      1  0   17.8296M
RT1      1  2   16.8620Ω
CT2      2  0   59.0954M
RT2      2  3   57.0433Ω
CT3      3  0   816.901M
RT3      3  0   63.6307Ω
*
.TRAN 1MS 0.2S
*
.OPTIONS LIMPTS=20000 RELTOL=0.002
.PROBE
.END
```

Figure 54. SPICE input deck used to simulate the thermal circuit of MMSF4P01Z and generate the input and outpu waveforms seen in Figure 55. Concerning the units in the SPICE deck, "M" means 10^{-3} and "U" means 10^{-6}.

Many courses, books and other forms of instruction are available concerning programming and operating SPICE software.[5] These subjects are not the intended scope of this paper. As stated before, Figure 55 represents the input and output waveforms of the SPICE input deck of Figures 52 and 53. Figures 55, 56, and 57 demonstrate the use of the same thermal circuit with other input patterns applied. The solid waveform in these figures is the input power to the thermal circuit. The dashed line represents the junction temperature of the device with this input power applied. As one can probably tell from Figures 52 and 57, it takes several hundred seconds for the MMSF4P01Z to reach a stable thermal condition, i.e. steady−state. What is pleasantly apparent, is that with a given RC network, which leads to a simple SPICE input deck, and the power input waveform information, the junction temperature condition can be easily ascertained. Of course, everything has a limit. If very complex input power waveforms which have short time intervals with respect to steady−state stabilization time are applied for extremely long time periods, one may run out of simulation capability. Figure 58, for example, represents approximately 4000 data points. The simulation for that particular example produced around 9000 data points all the way out to 1000 s.

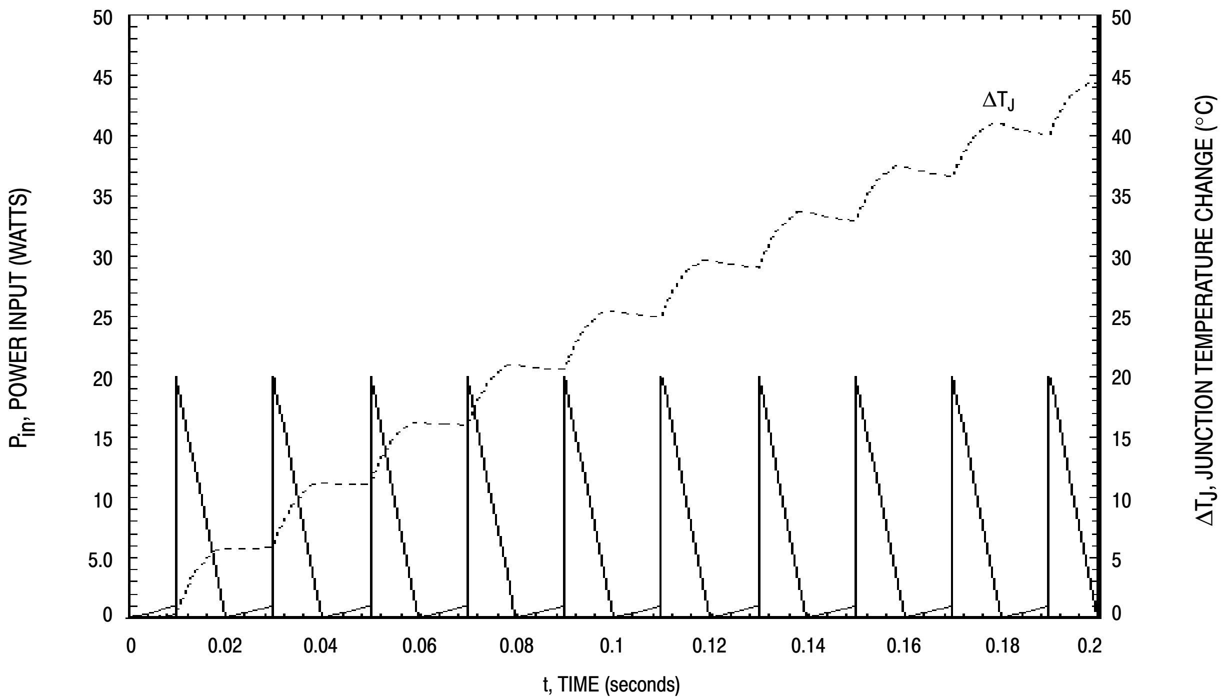


Figure 55. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 52 and 53 with a complex waveform as input.

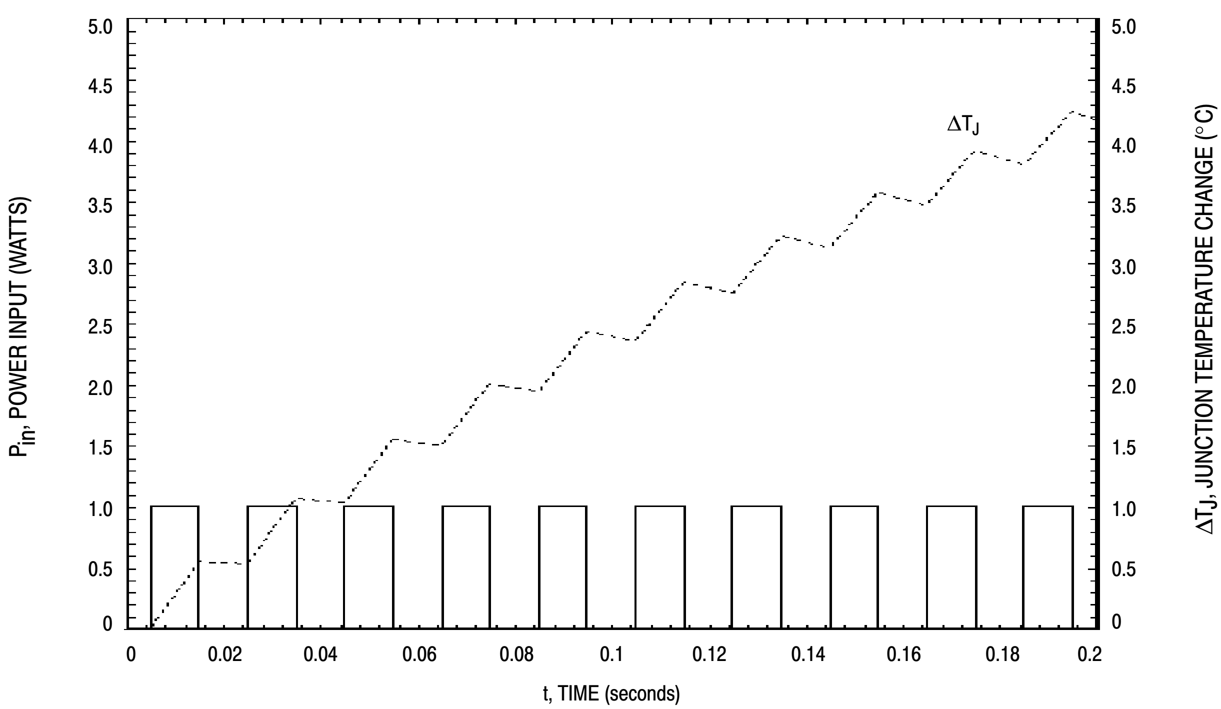


Figure 56. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 52 and 53 with a simple square waveform as input.

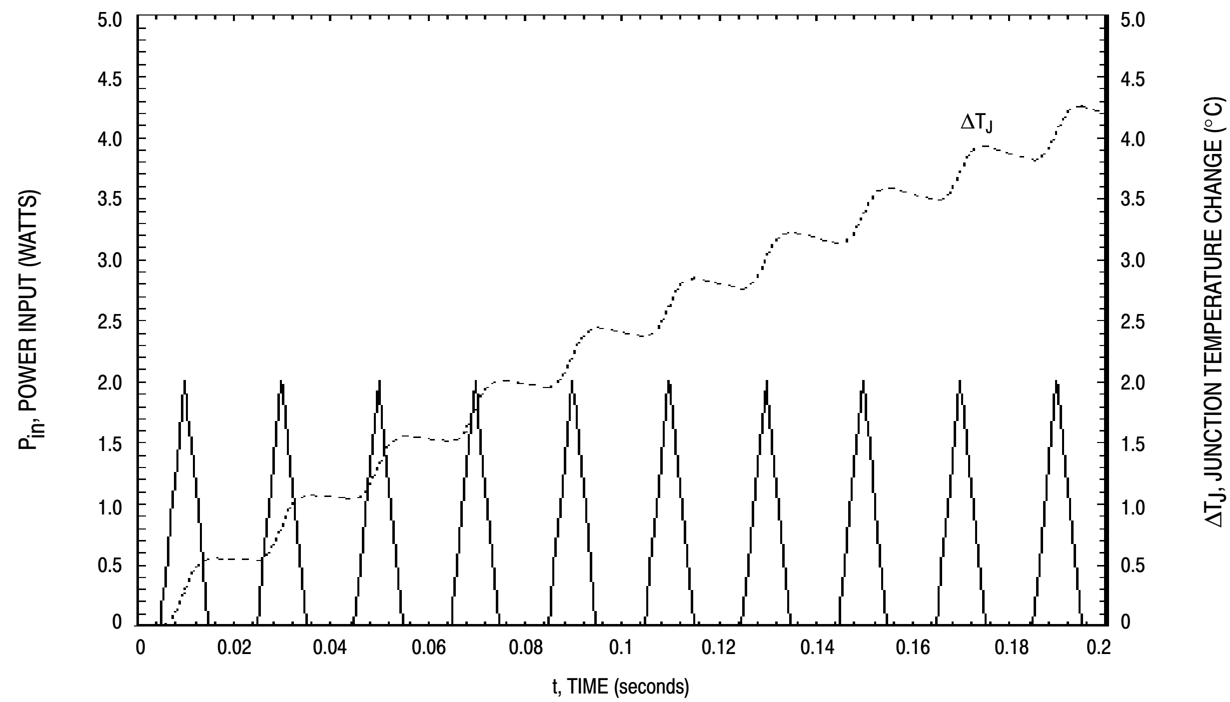


Figure 57. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 52 and 53 with a simple triangular waveform as input.

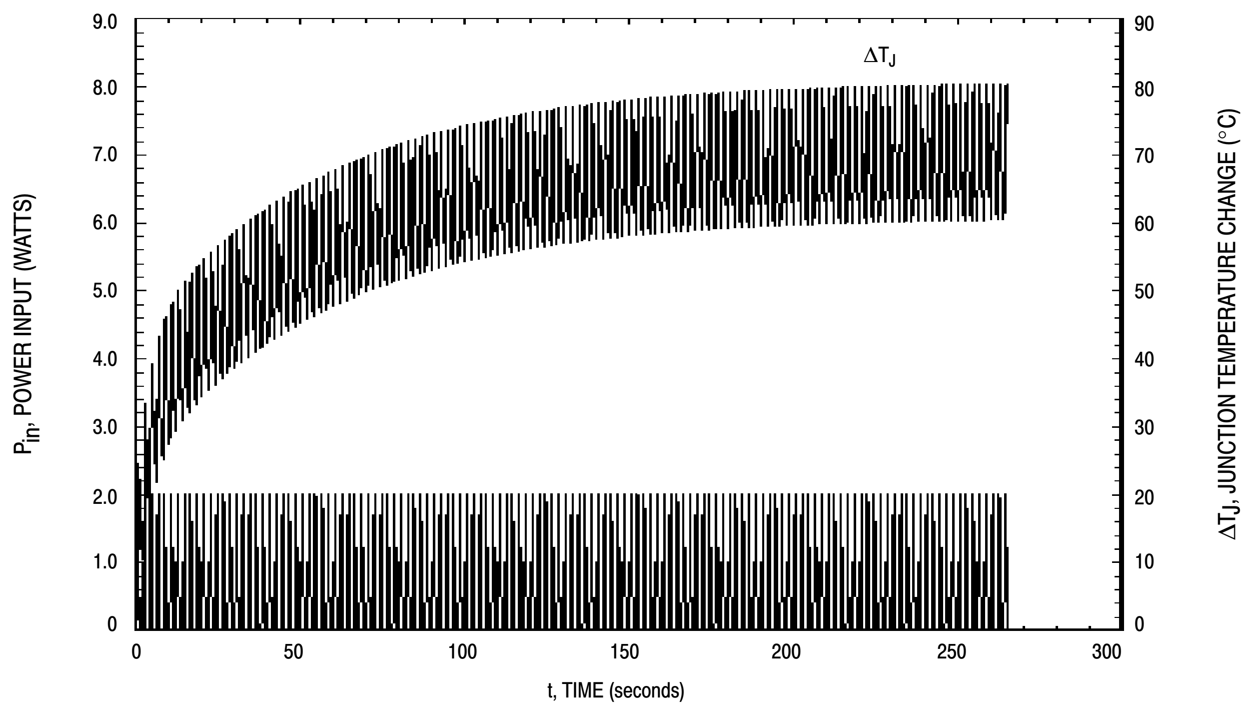


Figure 58. Input (power) and output (temperature) waveforms for the SPICE simulation of the thermal circuit given in Figures 52 and 53 with a low frequency triangular waveform as input. The analysis was carried out until the junction temperature had practically reached steady−state.

SUMMARY

In many situations, the design engineer is faced with the challenge of taking the manufacturers' specifications and characterization data and applying them to their unique application. For power semiconductor thermal performance, the hurtle is taking a thermal characterization for a device based on rectangular power pulse waveforms and transforming this information into useful results for a completely different power application. The attempt of this paper was to present a technique that can greatly reduce this obstacle. Given the RC thermal equivalent network for a device, the known input power waveforms and a circuit simulator, it is a fairly straight forward process to ascertain exactly the junction operating condition of the device. Realizing the power of this tool, some manufacturers, such as ON Semiconductor, are beginning to include this thermal circuit information in their data sheets.

REFERENCES

[1] Dashney, Gary E., "Basic Semiconductor Thermal Measurement", 1995, ON Semiconductor.

[2] Gottlieb, Irving M., 1992, *Regulated Power Supplies,* 4th Edition, Blue Ridge Summit, Pennsylvania, TAB BOOKS: (92−105).

[3] Roehr, Bill and Bryce Shiner, "Transient Thermal resistance — General Data and its Use", AN569 in ON Semiconductor *Power Applications Manual,* 1990, DL140/D: (23−38), Ph. (800−441−2447).

[4] Sofia, Dr. John W., "Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices", Analysis Tech, Wakefield, MA 01880, Ph. (617) 245−7825.

[5] Tuinenga, Paul W., SPICE: A Guide to Circuit Simulation and Analysis Using PSpice®, Second Edition, © 1992 Prentice−Hall, Inc.

Appendix A

Thermal Data on Power Surface Mount Packages

Appendix A Thermal Data on Power Surface Mount Packages

Device Type	Technology	Package	Die Size (mils)	Die Size (mm)	$R_{\theta JA}$ (°C/W)	Notes	$R_{\theta JA}$ (°C/W)
Rectifier	GaAs	D^2PAK	112 x 112	2.84 x 2.84	77.8	Air	3.3
Rectifier	Silicon/Schottky	D^2PAK	114 x 114	2.89 x 2.89	91.38	min	2.19
Rectifier	Silicon/Schottky	D^2PAK	114 x 114	2.89 x 2.89	52.29	1”, SS	
MOSFET	Silicon	D^2PAK	115 x 102	2.92 x 2.59	50	min	1.86
Rectifier	Silicon/Schottky	D^2PAK	128 x 128	3.25 x 3.25	90.19	min	4
Rectifier	Silicon/Schottky	D^2PAK	128 x 128	3.25 x 3.25	59.74	1”, SS	
MOSFET	Silicon	D^2PAK	145 x 145	3.68 x 3.68	50	min	1.29
Rectifier	Silicon/Schottky	D^2PAK	170 x 170	4.31 x 4.31	88.02	min	1.26
Rectifier	Silicon/Schottky	D^2PAK	170 x 170	4.31 x 4.31	54.46	1”, SS	
MOSFET	Silicon	D^2PAK	171 x 227	4.34 x 5.77	76.73	min	0.61
MOSFET	Silicon	D^2PAK	171 x 227	4.34 x 5.77	53.04	1”, SS	
MOSFET	Silicon	D^2PAK	180 x 175	4.57 x 4.44	50	min	1
Rectifier	Silicon/Schottky	D^2PAK	180 x 180	4.57 x 4.57	88.26	min	1.02
Rectifier	Silicon/Schottky	D^2PAK	180 x 180	4.57 x 4.57	56.67	1”, SS	
MOSFET	Silicon	D^2PAK	186 x 190	4.72 x 4.82	50	min	0.93
Rectifier	GaAs	D^2PAK	80 x 80	2.03 x 2.03	76.8	Air	3.77
Rectifier	Silicon/Schottky	DPAK	100 x 100	2.54 x 2.54	134.17	min	112.21
Rectifier	Silicon/Schottky	DPAK	100 x 100	2.54 x 2.54	67.53	1”, SS	2.43
MOSFET	Silicon	DPAK	102 x 102	2.59 x 2.59	118.12	min	1.72
MOSFET	Silicon	DPAK	115 x 102	2.92 x 2.59	71.4	min	1.86
Rectifier	Silicon/Schottky	DPAK	62 x 62	1.57 x 1.57	131.67	min	3.22
Rectifier	Silicon/Schottky	DPAK	62 x 62	1.57 x 1.57	63.95	1”, SS	
MOSFET	Silicon	DPAK	75 x 75	1.91 x 1.91			3.43
Rectifier	Silicon/Schottky	DPAK	80 x 80	2.03 x 2.03	123.34	min	2.5
Rectifier	Silicon/Schottky	DPAK	80 x 80	2.03 x 2.03	62.09	1”, SS	
MOSFET	Silicon	DPAK	89 x 89	2.26 x 2.26	71.4	min	2.38
MOSFET	Silicon	DPAK	89 x 89	2.26 x 2.26	92.29		2.61
MOSFET	Silicon	Micro8™	35 x 70	0.89 x 1.78	239.36	min	21.37
MOSFET	Silicon	Micro8™	35 x 70	0.89 x 1.78	121	1”, SS	26.66
MOSFET	Silicon	Micro8™	70 x 85	1.78 x 2.16	199.24	min	
MOSFET	Silicon	Micro8™	70 x 85	1.78 x 2.16	94.67	1”, SS	
MOSFET	Silicon	Micro8™	70 x 85	1.78 x 2.16	107.67	0.5”, min	
Rectifier	Silicon	Powermite™	40 x 40	1.01 x 1.01	247.2	min	19.5
Rectifier	Silicon/Schottky	Powermite™	40 x 40	1.01 x 1.01	254.9	min	
Rectifier	Silicon/Schottky	Powermite™	40 x 40	1.01 x 1.01	83.1	1”, SS	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	243.95	min	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	85.74	1”, SS	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	250.57	min	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	104.47	0.7”, SS	
Rectifier	Silicon/Schottky	SMA	39 x 39	0.99 x 0.99	87.53	1”, SS	

NOTES:
1. Derating applied to all numbers
   $R_{\theta JX} < 20$: #*1.25
   $20 < R_{\theta JX} < 100$ #*(1+)0.25−0.15*((#−20)/80)))
   $R_{\theta JX} > 100$ #*1.1
2. $R_{\theta JA}$ is on min pad unless noted
3. DXPAK $R_{\theta JA}$ is on min pad unless noted

Appendix A Thermal Data on Power Surface Mount Packages

Device Type	Technology	Package	Die Size (mils)	Die Size (mm)	$R_{\theta JA}$ (°C/W)	Notes	$R_{\theta JA}$ (°C/W)
Rectifier	Silicon/Schottky	SMA	45 x 45	1.14 x 1.14	253.76	min	
Rectifier	Silicon/Schottky	SMA	45 x 45	1.14 x 1.14	101.53	0.7”, SS	
Rectifier	Silicon/Schottky	SMA	45 x 45	1.14 x 1.14	86.4	1”, SS	
Rectifier	Silicon/Schottky	SMA	49 x 49	1.24 x 1.24	251.1	min	
Rectifier	Silicon/Schottky	SMA	49 x 49	1.24 x 1.24	86.7	1”, SS	
Rectifier	Silicon	SMA	52 x 52	1.32 x 1.32	88.3	1”, SS	
Rectifier	Silicon	SMA	52 x 52	1.32 x 1.32	240.7	min	
Rectifier	Silicon	SMA	52 x 52	1.32 x 1.32	247.5	min	
Rectifier	Silicon/Schottky	SMA	52 x 52	1.32 x 1.32	250.01	min	
Rectifier	Silicon/Schottky	SMA	52 x 52	1.32 x 1.32	103.97	0.7”, SS	
Rectifier	Silicon/Schottky	SMA	52 x 52	1.32 x 1.32	85.57	1”, SS	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	219.07	min	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	80.82	1”, SS	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	208.1	min	
Rectifier	Silicon/Schottky	SMB	39 x 39	0.99 x 0.99	78.1	1”, SS	
Rectifier	Silicon	SMB	46 x 46	1.16 x 1.16	79.26	1”, SS	
Rectifier	Silicon	SMB	46 x 46	1.16 x 1.16	234.41	min	
Rectifier	Silicon	SMB	60 x 60	1.52 x 1.52	75.44	1”, SS	
Rectifier	Silicon	SMB	60 x 60	1.52 x 1.52	231.63	min	
Rectifier	Silicon/Schottky	SMB	62 x 62	1.57 x 1.57	225.65	min	
Rectifier	Silicon/Schottky	SMB	62 x 62	1.57 x 1.57	77.38	1”, SS	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	164	min	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	70.7	1”, SS	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	71.6	1”, SS	
Rectifier	Silicon/Schottky	SMC	62 x 62	1.57 x 1.57	164.4	min	
Rectifier	Silicon	SMC	71 x 71	1.80 x 1.80	74.7	1”, SS	
MOSFET	Silicon	SO−8	34 x 68	0.86 x 1.73	176.6	min	
MOSFET	Silicon	SO−8	34 x 68	0.86 x 1.73	105.4	1”, SS	
MOSFET	Silicon	SO−8	34 x 68	0.86 x 1.73	66.33	1”, 10S	
BIPOLAR	Silicon	SO−8	51 x 54	1.3 x 1.37	186.6	min	
BIPOLAR	Silicon	SO−8	51 x 54	1.3 x 1.37	126.3	0.7”, SS	
BIPOLAR	Silicon	SO−8	51 x 54	1.3 x 1.37	108.4	1”, SS	
BIPOLAR	Silicon	SO−8	56 x 84	1.42 x 2.13	185.7	min	
BIPOLAR	Silicon	SO−8	56 x 84	1.42 x 2.13	116.2	0.7”, SS	
BIPOLAR	Silicon	SO−8	56 x 84	1.42 x 2.13	99.6	1”, SS	
MOSFET	Silicon	SO−8	57 x 99	1.45 x 2.51	166.1	min	
MOSFET	Silicon	SO−8	57 x 99	1.45 x 2.51	97.8	1”, SS	
MOSFET	Silicon	SO−8	57 x 99	1.45 x 2.51	61.7	1”, 10S	
MOSFET	Silicon	SO−8	57 x 99	1.45 x 2.51	85.6	1”, SS	
MOSFET	Silicon	SO−8	57 x 99	1.45 x 2.51	49.33	1”, 10S	
MOSFET	Silicon	SO−8	58 x 99	1.47 x 2.51	160.8	min	
MOSFET	Silicon	SO−8	89 x 150	2.26 x 3.81	145.13	min	
Rectifier	Silicon/Schottky	SO−8	90 x 90	2.29 x 2.29	138.5	min	

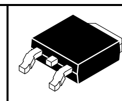
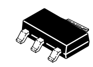
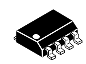
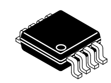
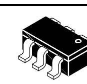
NOTES:
1. Derating applied to all numbers
   $R_{\theta JX} < 20$: #*1.25
   $20 < R_{\theta JX} < 100$ #*(1+)0.25−0.15*((#−20)/80)))
   $R_{\theta JX} > 100$ #*1.1
2. $R_{\theta JA}$ is on min pad unless noted
3. DXPAK $R_{\theta JA}$ is on min pad unless noted

Appendix A Thermal Data on Power Surface Mount Packages

Device Type	Technology	Package	Die Size (mils)	Die Size (mm)	$R_{\theta JA}$ (°C/W)	Notes	$R_{\theta JA}$ (°C/W)
MOSFET	Silicon	SO−8	98 x 120	2.49 x 3.04	133.2	min	
MOSFET	Silicon	SO−8	98 x 120	2.49 x 3.04	81.5	1”, SS	
MOSFET	Silicon	SO−8	98 x 120	2.49 x 3.04	129	min	
MOSFET	Silicon	SO−8	98 x 120	2.49 x 3.04	80.9	1”, SS	
MOSFET	Silicon	SO−8	98 x 120	2.49 x 3.04	44.5	1”, 10S	
Rectifier	Silicon/Schottky	SOD−123	35 x 35	0.89 x 0.89	205.7	1”, SS	
Rectifier	Silicon/Schottky	SOD−123	35 x 35	0.89 x 0.89	429.2	min	
MOSFET	Silicon	SOT−223	35 x 70	0.89 x 1.78	167.49	min	
MOSFET	Silicon	SOT−223	35 x 70	0.89 x 1.78	75.49	1”, SS	
MOSFET	Silicon	SOT−223	55 x 90	1.40 x 2.29	159.8	min	
MOSFET	Silicon	SOT−223	55 x 90	1.40 x 2.29	88.5	0.7”, SS	
MOSFET	Silicon	SOT−223	55 x 90	1.40 x 2.29	71.8	1”, SS	

NOTES:
1. Derating applied to all numbers
   $R_{\theta JX}$ < 20: #*1.25
   20 < $R_{\theta JX}$ < 100 #*(1+)0.25−0.15*((#−20)/80)))
   $R_{\theta JX}$ > 100 #*1.1
2. $R_{\theta JA}$ is on min pad unless noted
3. DXPAK $R_{\theta JA}$ is on min pad unless noted

Thermal Comparison and Summary of Low Voltage Surface Mount Packages

Time in Seconds	Minimum Pad Size (°C/W)	Minimum Pad Size (watts)	0.5" Sq. Pad Size (°C/W)	0.5" Sq. Pad Size (watts)	1" Sq. Pad Size (°C/W)	1" Sq. Pad Size (watts)	Die Size (mils)	Die Size (mm)	Packages
5	24.5	5.10	—	—	15	8.33	100x100	2.54x2.54	 DPAK
10	38.5	3.25	—	—	21	5.95			
SS	134	0.93	—	—	67.5	1.85			
5	55	2.27	—	—	30	4.17	35x70	0.889x1.77	 SOT−223
10	75	1.67	—	—	35	3.57			
SS	167	0.75	—	—	75.94	1.65			
5	50.5	2.48	44	2.84	37.5	3.33	96x120	2.438x3.04	 SO−8
10	64	1.95	51.5	2.43	44	2.84			
SS	128.9	0.97	102	1.23	80.9	1.55			
5	97.5	1.28	52	2.40	46	2.72	70x85	1.77x2.159	 Micro8
10	122	1.02	56	2.23	51	2.45			
SS	199	0.63	107.6	1.16	94.7	1.32			
5	137	0.91	62	2.02	58.3	2.14	40x70	1.016x1.77	 TSOP−6
10	160	0.78	68.3	1.83	61.5	2.03			
SS	241	0.52	125.8	0.99	102.3	1.22			

NOTES: These apply to all of the measurements
SS = Steady State
Thermal measurements are $R_{\theta JA}$ in °C/Watt
Measurements have been derated
All devices are single die

Appendix B

Applicable Standards

APPENDIX B: APPLICABLE STANDARDS

The following list contains applicable Electronic Industries Association (EIA) JEDEC Standards. These may be obtained by accessing the JEDEC website at www.JEDEC.org

JESD30−B Descriptive Designation System for Semiconductor−Device Packages

JESD1 JEDEC Standard 1, Leadless Chip Carrier Pinouts Standardized for Linear's

JESD2 JEDEC Standard 2, Digital Bipolar Pinouts for Chip Carriers

JESD4 JEDEC Standard 4, Definition of External Clearance and Creepage Distances of Discrete Semiconductor Packages for Thyristors and Rectifiers

JESD9−A JEDEC Standard 9−A, Metal Package Specification for Microelectronic Packages

JESD11 JEDEC Standard 11, Chip Carrier Pinouts Standardized for CMOS 4000, HC and HCT Series of Logic Circuits

JESD27 JEDEC Standard 27, Ceramic Package Specification for Microelectronic Packages

JESD51 JEDEC Standard 51, Methodology for the Thermal Measurement of Component Packages

JESD51−1 JEDEC Standard 51, Addendum No. 1, Integrated Circuit Thermal Measurement Method − Electrical Test Method (Single Semiconductor Device)

JESD51−2 JEDEC Standard 51, Addendum No. 2, Integrated Circuits Thermal Test Method Environment Conditions − Natural Convection (Still Air)

JESD51−3 JEDEC Standard 51, Addendum No. 3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

JESD51−4 JEDEC Standard 51, Addendum No. 4, Thermal Test Chip Guideline (Wire Bond Type Chip)

JESD51−5 JEDEC Standard 51, Addendum No. 5, Extension of Thermal Test board Standards for Packages with direct Thermal Attachment Mechanisms

JESD51−6 JEDEC Standard 51, Addendum No. 6, Integrated Circuit Thermal Test Method Environmental Conditions − Forced Convection (Moving Air)

JESD51−7 JEDEC Standard 51, Addendum No. 7, High Effective Thermal Conductivity Test Board for Leaded Surface mount Packages

JESD51−8 JEDEC Standard 51, Addendum No. 8, Integrated Circuit Thermal Test Method Environmental Conditions − Junction−to−Board

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